EECS 240

Analog Integrated Circuits

Topic 9: Operation Transconductance Amplifier (OTA)

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Operational Transconductance Amplifiers

- OTA versus OpAmp, Applications
- Differential versus Single-Ended Output
- Characteristics
  - Frequency response, settling time, stability
  - Open-loop gain
  - Noise, dynamic range
  - PSRR, CMRR
  - Common-mode feedback circuit
- Topologies
  - Single-stage (telescopic, folded cascode, …)
  - Multi-stage, Miller compensation
  - Class A, A/B

OpAmp versus OTA

OpAmp

- Voltage source output (low impedance)
- Essential to drive resistive loads
- Essentially OTA + buffer
- Buffer increases power dissipation, noise

OTA

- Current source output (high impedance)
- Cannot drive resistive loads
- Use capacitive (SC) feedback
- Transistors are transconductors

Resistive Feedback

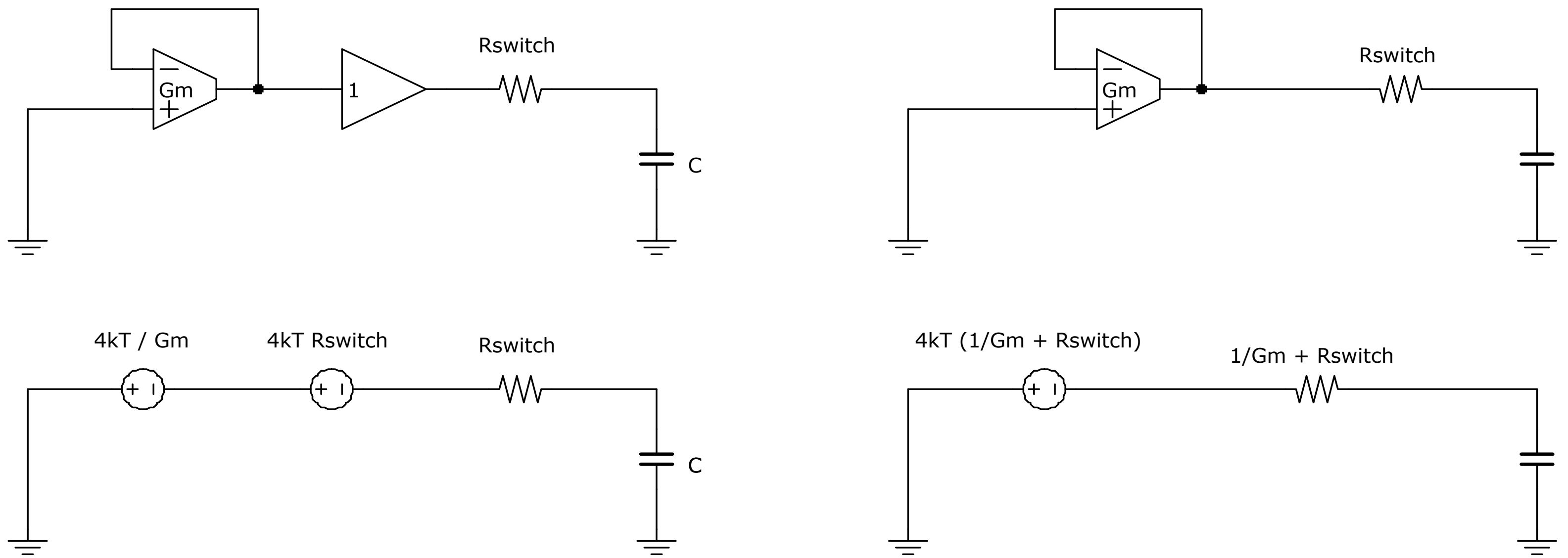
OpAmp

- Gain independent of feedback network
- Feedback network adds noise

OTA

- Resistive feedback network lowers loop gain
- Large feedback resistors?
  - Large area
  - Parasitic poles → stability?
- Solution: capacitive feedback
  - Needs initialization
  - Needs clock → Linear, time-variant circuit
- kT/C noise

OpAmp versus OTA Noise



$$\overline{v_{oT}^2} = \frac{kT}{C}\left(1 + \frac{R_{\text{noise}}}{\mathrm{R}_{\text{switch}}}\right)$$

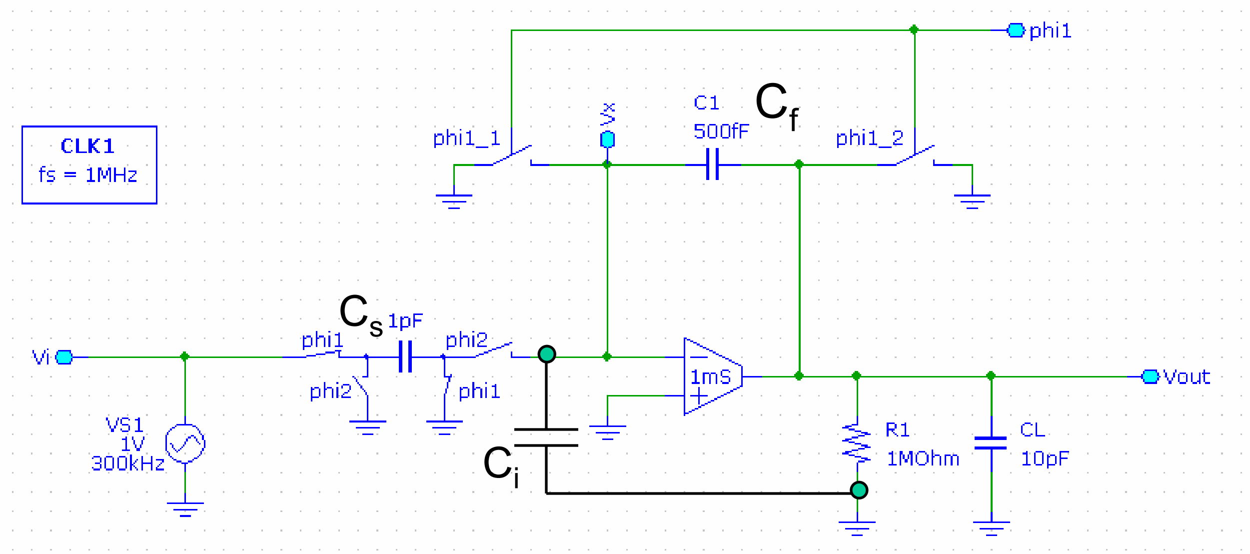
$$\overline{v_{oT}^2} = \frac{kT}{C}$$

Opamp and switch noise add

OTA contributes no excess noise (actual designs can increase noise)

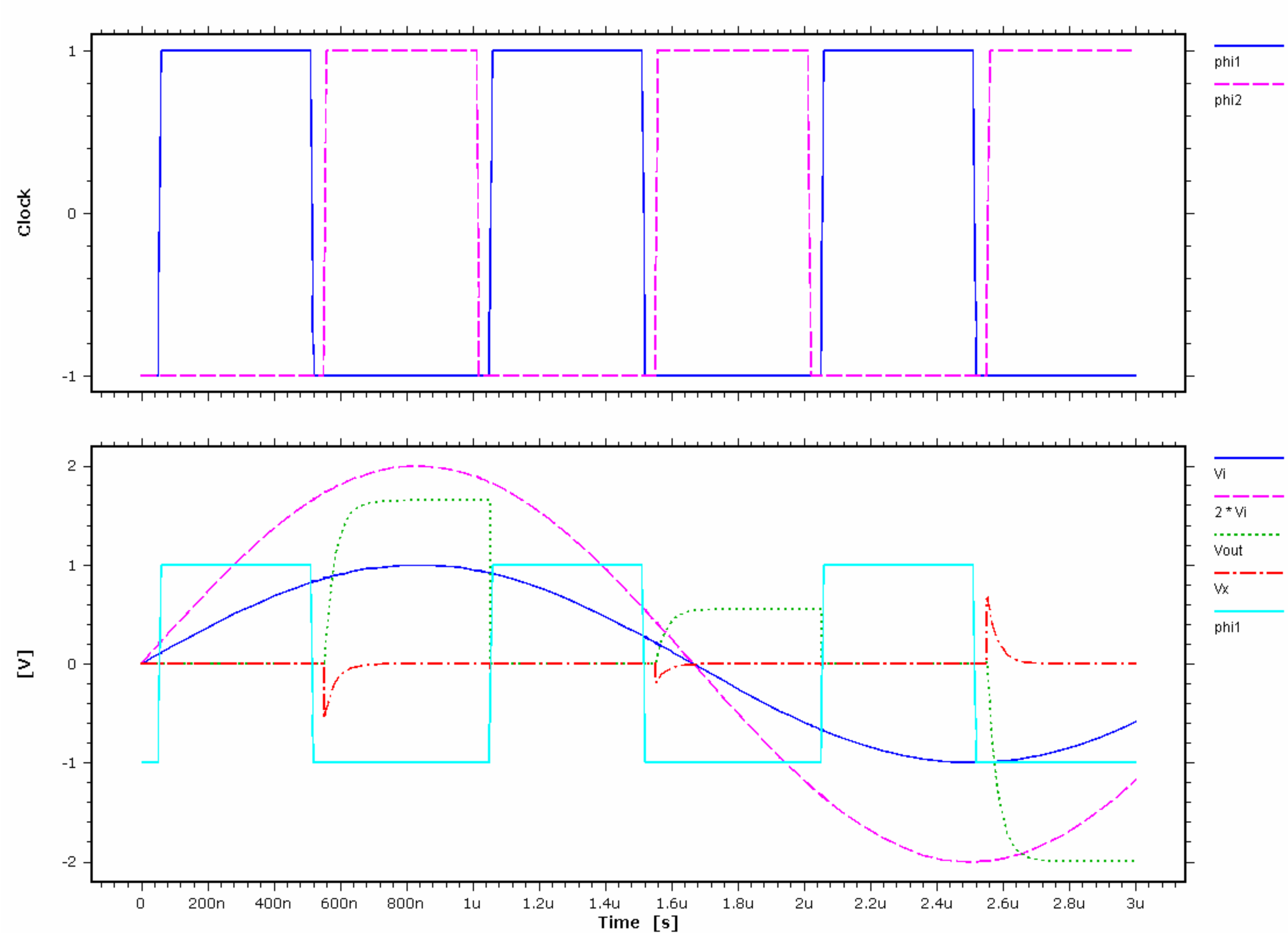
SC Gain Stage

- **Phase 1:**
  - sample V_i onto C_s:
  - $Q_s = V_i * C_s$
  - Null charge on C_f
- **Phase 2:**
  - Amplifier "moves" charge from C_s to C_f:
  - $Q_f = Q_s = V_i * C_s$
  - $V_{out} = Q_f / C_f$
    $= V_i * C_s / C_f$

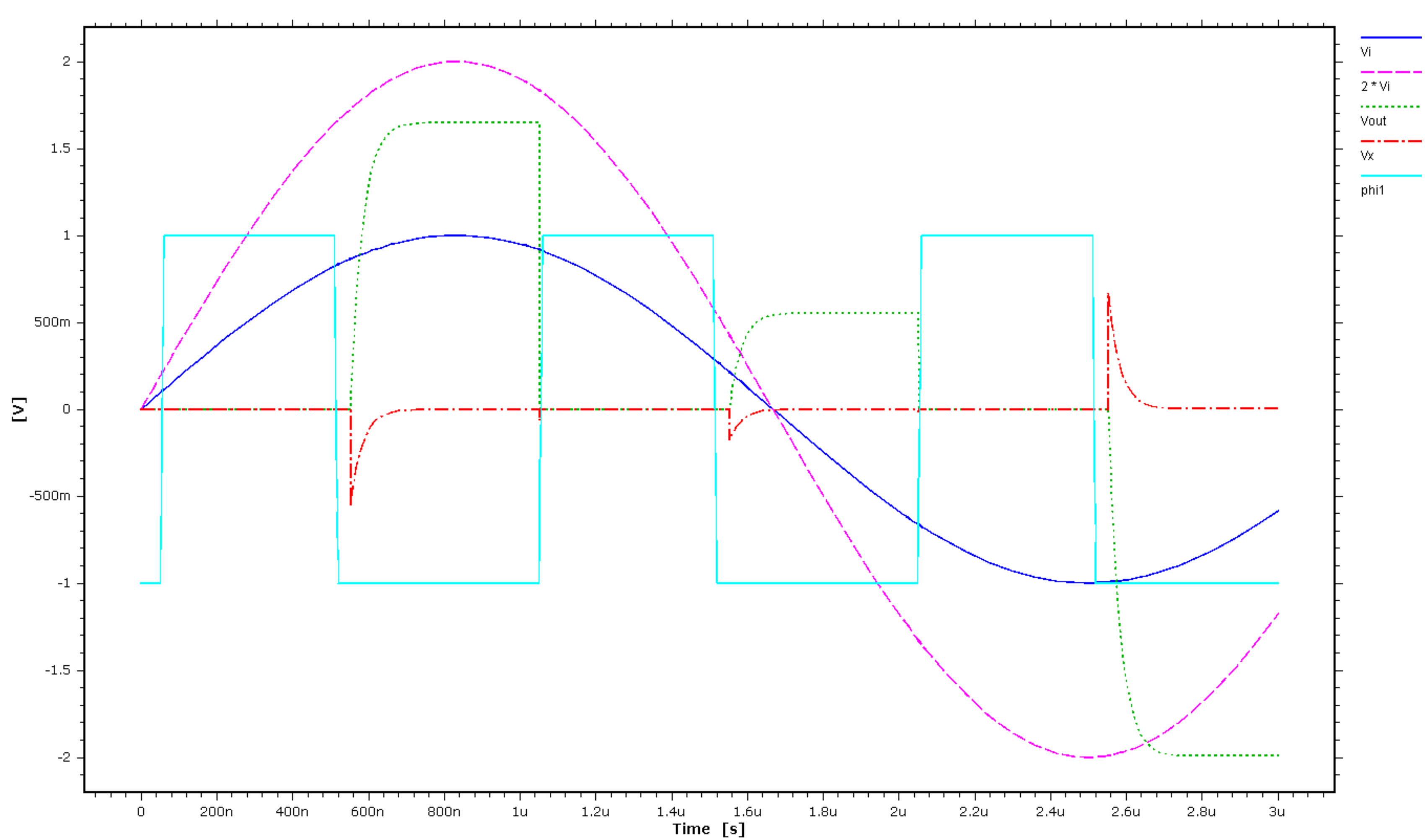


- Implement switches with MOSFETs. Drive with "2-phase non-overlapping clock".
- Gain set by capacitor ratio (precise). Output valid only at end of phase 2 and during phase 1.
- Cannot drive resistive load.

SC Gain Stage



SC Gain Stage



Noise

Phase 1:

$$\overline{v_{C_s}^2} = \frac{kT}{C_s} \underbrace{n_{f1}}_{\text{noise factor of amplifier driving } V_i}$$

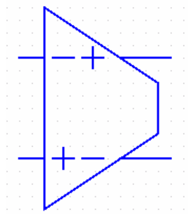
$$\overline{v_{C_F}^2} = \frac{kT}{C_f}$$

Phase 2: Phase 1 noise and OTA noise onto C_L

$$\overline{v_{on}^2} = \overline{v_{C_s}^2}\left(\frac{C_s}{C_f}\right)^2 + \frac{kT}{C_f} + \underbrace{\frac{kT}{C_L}}_{\text{for single-stage OTA}} \underbrace{\frac{1}{F}}_{\text{feedback factor}} \underbrace{n_{f2}}_{\text{noise factor of this amplifier}}$$

$$= \underbrace{\frac{kT}{C_f}\left(\frac{C_s}{C_f} n_{f1} + 1\right)}_{\text{feedback network}} + \underbrace{\frac{kT}{C_{Leff}} \frac{1}{F} n_{f2}}_{\text{OTA}} \quad \text{with} \quad F = \frac{C_f}{C_f + C_s + C_i}$$

Differential Output
"Fully differential amplifier"



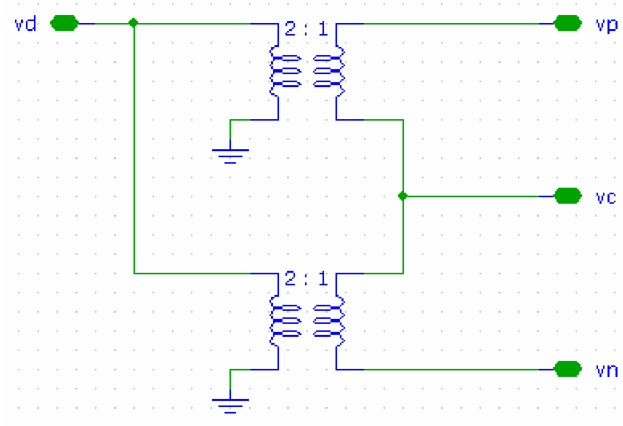
$$v_{id} = v_i^+ - v_i^-$$

$$v_{ic} = \tfrac{1}{2}\left(v_i^+ + v_i^-\right)$$

$$v_i^+ = v_{ic} + \tfrac{1}{2} v_{id}$$

$$v_i^- = v_{ic} - \tfrac{1}{2} v_{id}$$

- Differential versus common-mode signals
- Balun
- Common-mode feedback CMFB



PSRR & CMRR

- Any terminal is an input
- Important "undesired" inputs:
  - Supply
  - (Input) common-mode
- Figure-of-merit:
  - Desired gain over undesired gain >> 1
  - E.g. PSRR, CMRR

$$A_{dm} = \frac{v_{od}}{v_{id}} \to \infty$$

$$A_{cm} = \frac{v_{oc}}{v_{ic}} \to 0$$

$$A_{cdm} = \frac{v_{od}}{v_{ic}} \to 0$$

$$A_{VDD} = \frac{v_{od}}{v_{DD}} \to 0$$

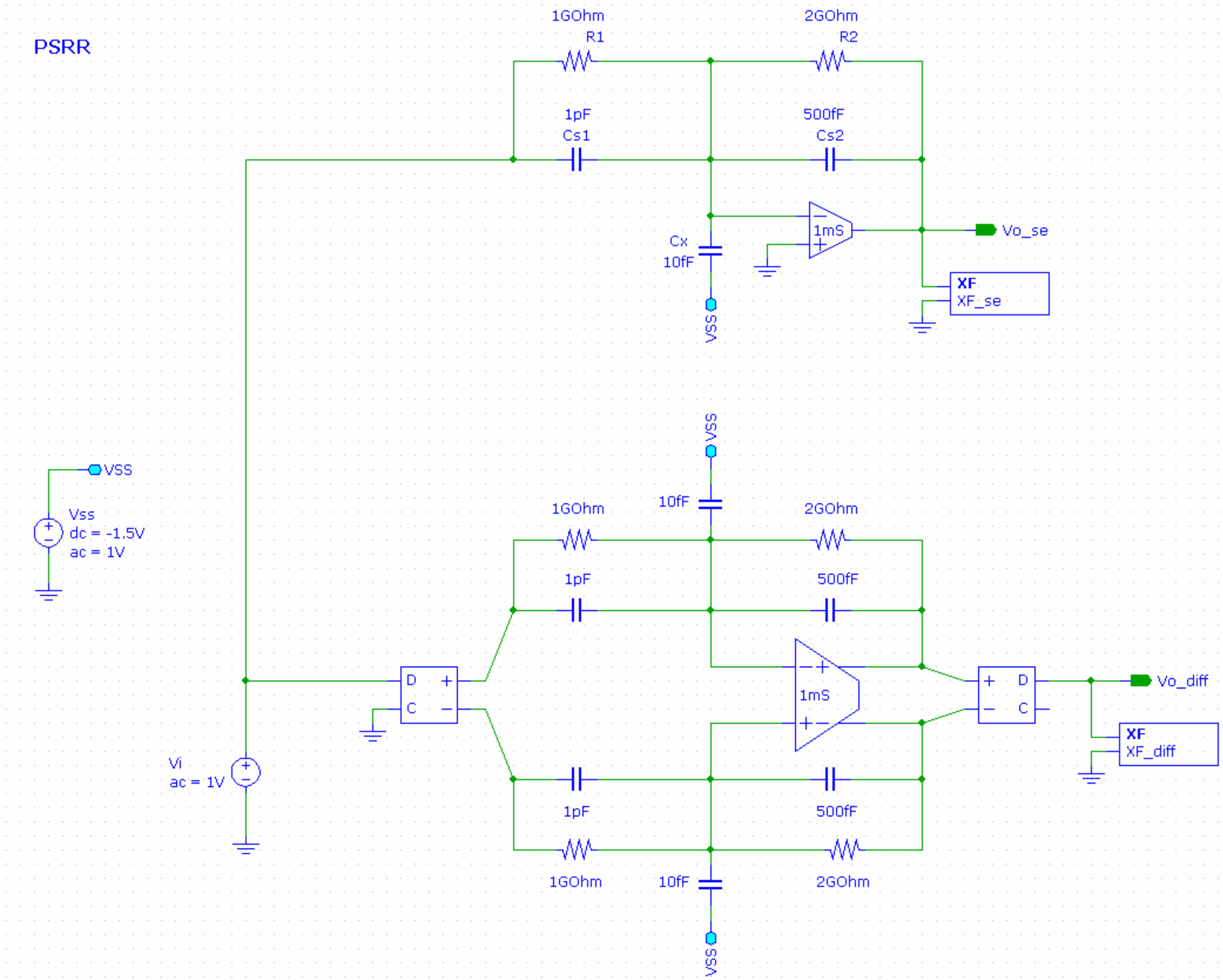
$$A_{VSS} = \frac{v_{od}}{v_{SS}} \to 0$$

$$CMRR = \left| \frac{A_{dm}}{A_{cdm}} \right| \to \infty$$

$$PSRR_{VDD} = \left| \frac{A_{dm}}{A_{VDD}} \right| \to \infty$$

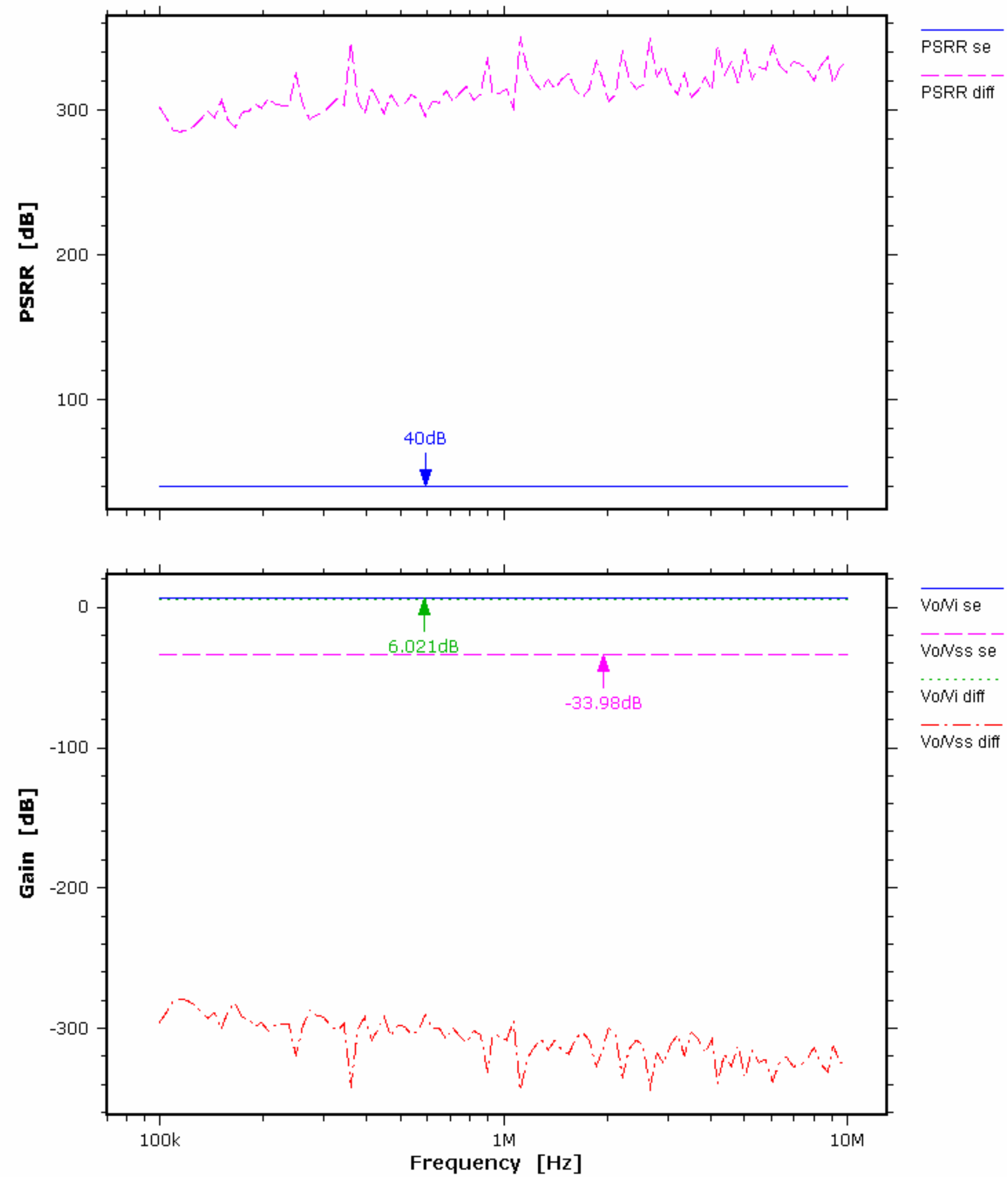
$$PSRR_{VSS} = \left| \frac{A_{dm}}{A_{VSS}} \right| \to \infty$$

PSRR Example

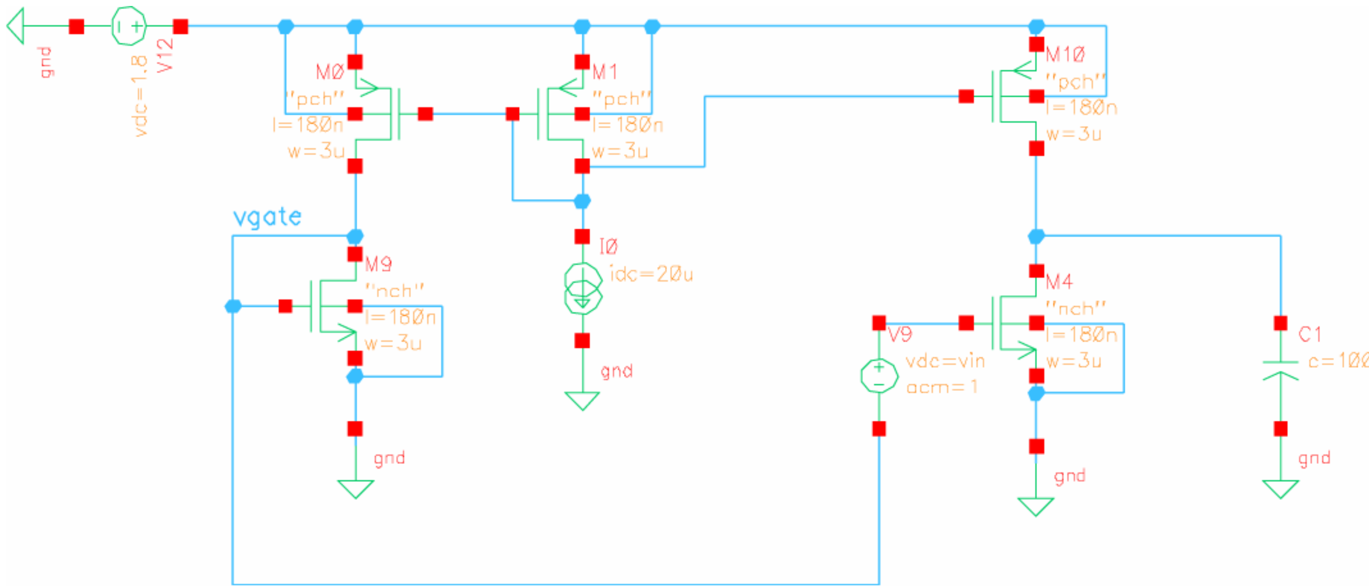


PSRR

Fully differential circuit has excellent PSRR limited only by matching

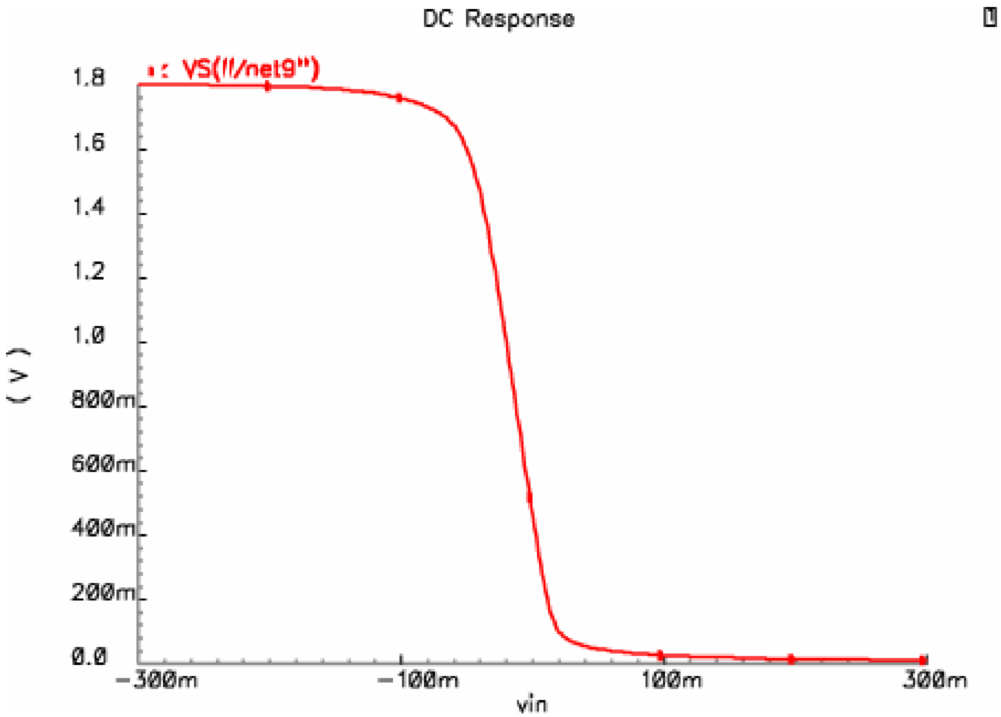


Common-Source Stage

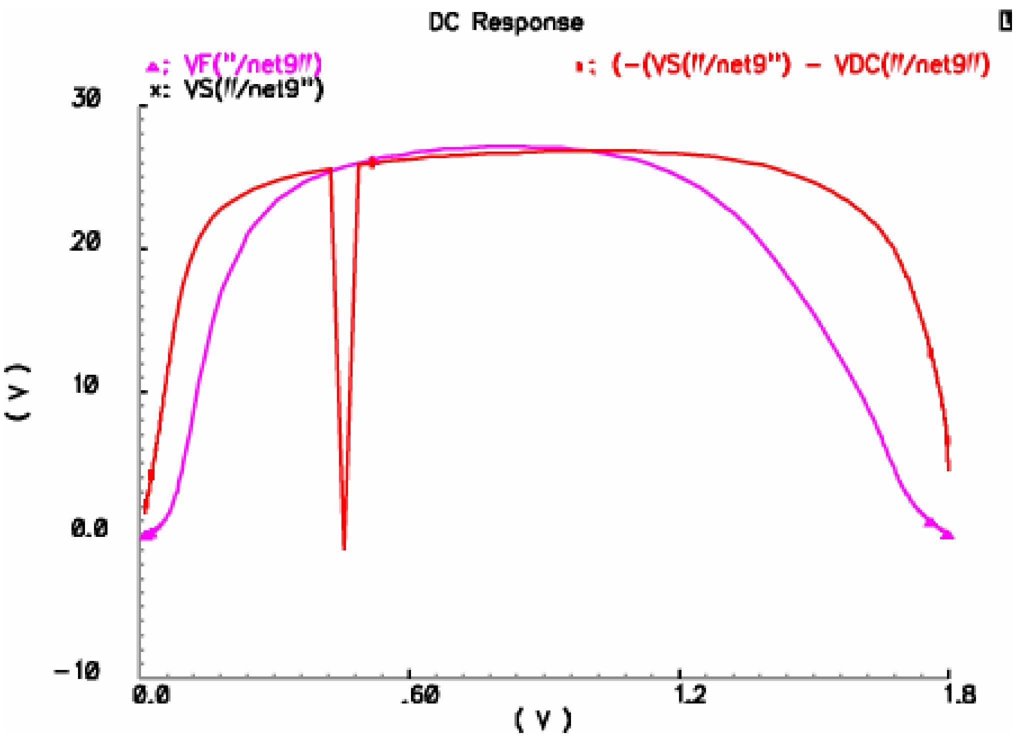


- Openloop gain, A_{vo}, a_{vo}
- Output range, ΔV_o
- Bandwidth, f_u, f_{3dB}
- Noise

DC Input/Output Operation



Gain, Output Range

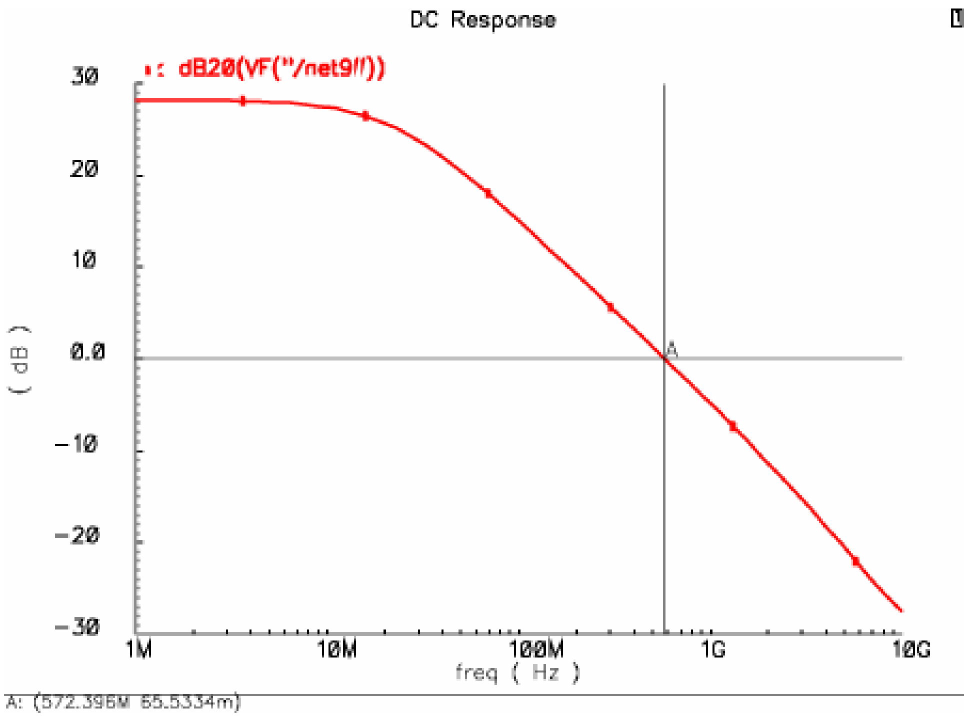


$$A_{vo} = \frac{V_{out} - V_{out\_o}}{V_{in} - V_{in\_o}}$$

$$a_{vo} = \frac{dV_{out}}{dV_{in}}$$

Note: plot is for
V_{out_o} = 0V and
V_{in_o} = 0V (unrealistic).

Frequency Response



$$0 = v_i g_m + v_o \left(sC_L + \frac{1}{r_o} \right)$$

$$\frac{v_o}{v_i} = -\frac{g_m r_o}{1 + s r_o C_L}$$

$$= -\frac{1}{\frac{1}{g_m r_o} + s\frac{C_L}{g_m}}$$

$$\approx -\frac{g_m}{sC_L} \quad \text{for} \quad g_m r_o >> 1$$

(when current through r_o is negligible)

Noise

$$\frac{\overline{v_{ieq}^2}}{\Delta f} = 4k_B T\gamma \frac{1}{g_{m1}^2}\left(g_{m1} + g_{m2}\right)$$

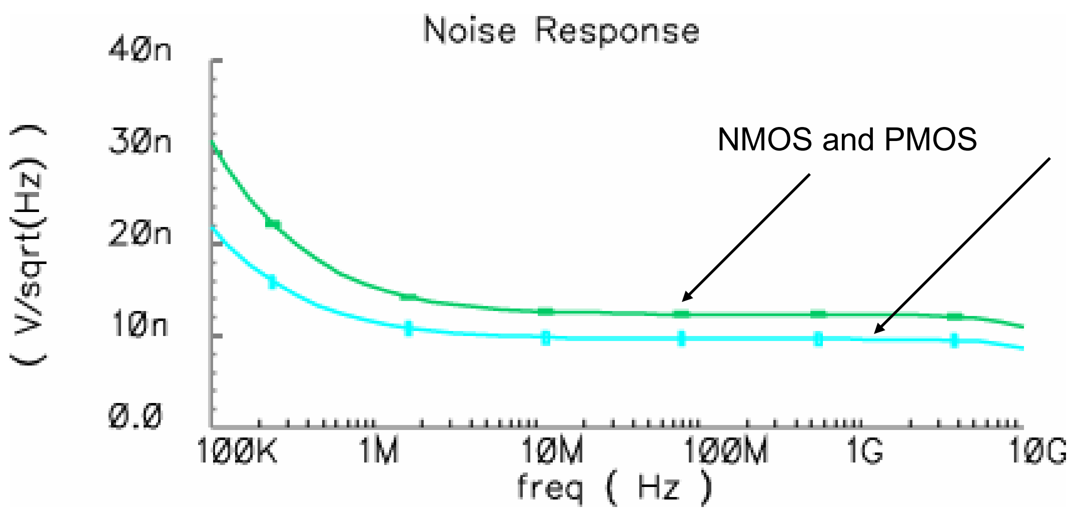
$$= 4k_B T\gamma \frac{1}{g_{m1}}\left(1 + \frac{g_{m2}}{g_{m1}}\right)$$

$$= 4k_B T\gamma \frac{1}{g_{m1}}\underbrace{\left(1 + \frac{V_1^*}{V_2^*}\right)}_{n_f}$$

Total noise is noise from M_1 multiplied by V_1^*/V_2^*

→ $V_2^* >> V_1^*$ (low noise)

→ Tradeoff with output range ΔV_{out}.

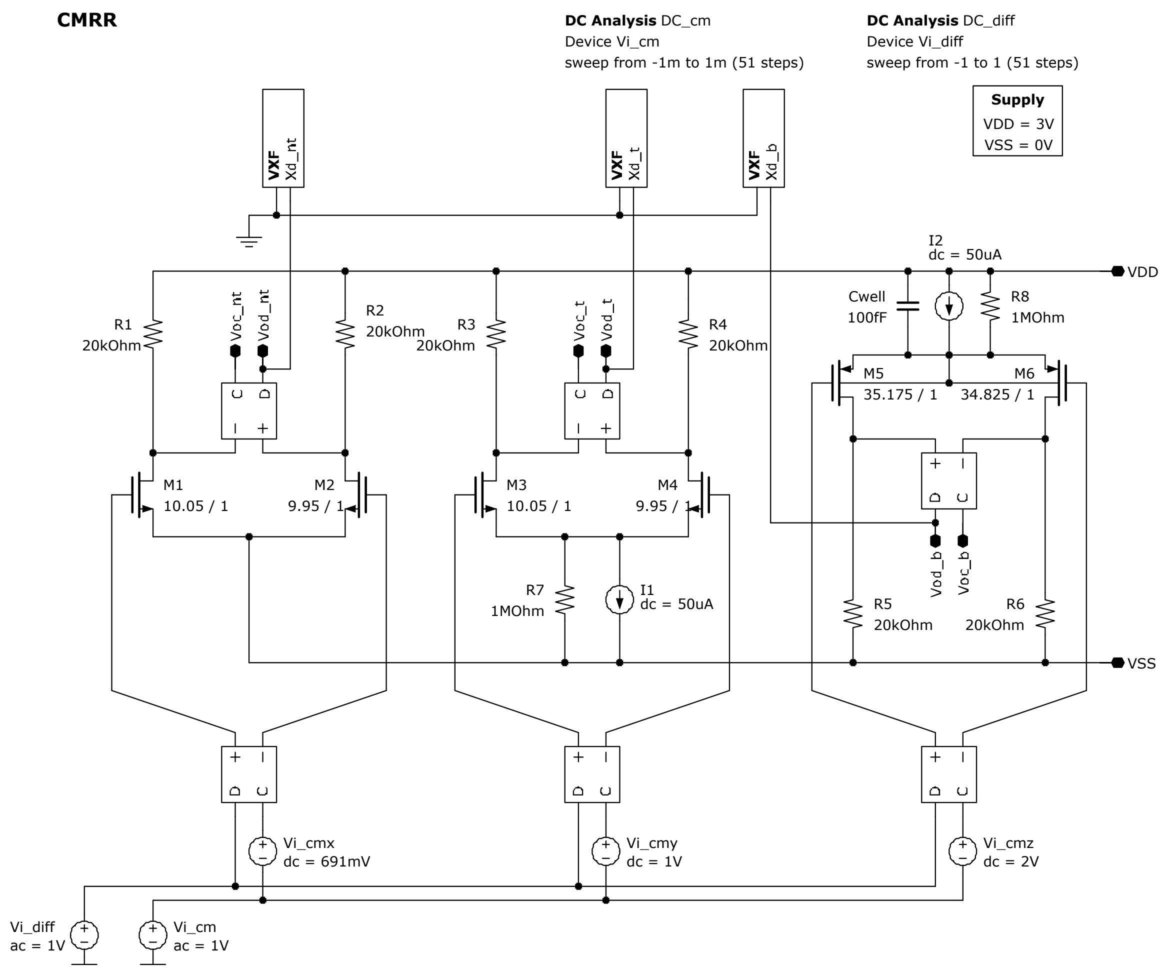


Differential Input

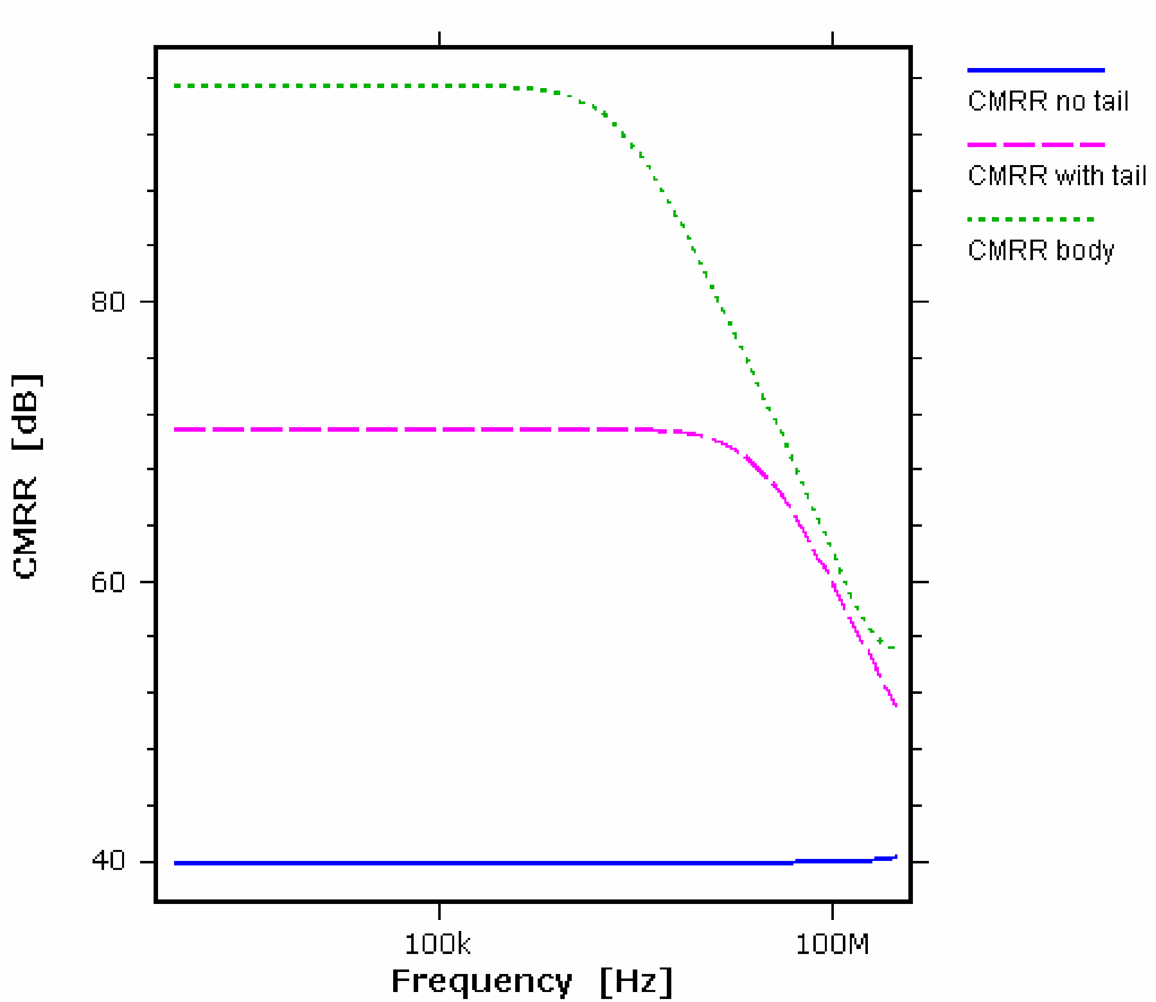
- Differential input:
  eliminates systematic offset

- Tail current source:
  provides CMRR

Differential Pair – CMRR



Simulation Result



For all cases:

$g_m = 290\ \mu S$

$V^* = 180\ mV$

$A_{vo} = 5.5$

CMRR Analysis

No tail current source	Tail / No Body Effect	Tail / With Body Effect
$A_{dm} = G_m R_o$ $A_{cm} = G_m R_o$ $A_{cdm} = \Delta G_m R_o + G_m \Delta R_o$ $= G_m R_o \left(\frac{\Delta G_m}{G_m} + \frac{\Delta R_o}{R_o} \right)$ $CMRR = \frac{1}{\frac{\Delta G_m}{G_m} + \frac{\Delta R_o}{R_o}}$ • **E.g.** **1/0.01 = 100 = 40dB**	$A_{dm} = G_m R_o$ $A_{cm} \approx \frac{R_o}{2R_{SS}}$ for $v_{sb} \approx v_{ic}$ $A_{cdm} = \frac{R_o}{2R_{SS}} \left(\frac{\Delta G_m}{G_m} + \frac{\Delta R_o}{R_o} \right)$ $CMRR = \frac{2 G_m R_{SS}}{\frac{\Delta G_m}{G_m} + \frac{\Delta R_o}{R_o}}$ • **E.g.** **2 x 1mS * 1MΩ / 0.01** **= 200,000 = 106dB**	• **Ignoring ΔG_m, Δr_o (use superposition)** $A_{dm} = G_m R_o$ $A_{cdm} = \Delta g_{mb} R_o$ for $v_{sb} \approx v_{ic}$ $CMRR = \frac{G_m}{\Delta g_{mb}}$ $= \frac{g_m / g_{mb}}{\Delta g_{mb} / g_{mb}}$ • **E.g.** **10/0.01 = 1000 = 60dB**

CMRR Summary

No tail current source	With tail current source	Well tied to source
• CMRR limited by matching	• CMRR improved by …	• Eliminates g_{mb} matching constraint
• Bias current is a strong function of input common-mode	• High frequency CMRR limited by capacitance at common-source node (C_{SB})	• CMRR limited by I_D modulation; cascode helps
• Impractical in most situations		• C_{well} sets high frequency CMRR
		• $C_{well} < C_{SB}$ in some deep sub-micron processes (with high S/D doping)