EECS 240
Analog Integrated Circuits

Topic 19: Offset Cancellation

Ali M. Niknejad and Bernhard E. Boser
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Department of Electrical Engineering and Computer Sciences

Offset Cancellation Overview

- Techniques:
  - Correlated double sampling (CDS)
  - Chopper stabilization

- Reject offset and 1/f noise

- Alphabet soup
  - CDS: autozeroing, ping-pong opamp, self-calibrating opamp
  - Chopping: synchronous detection, dynamic element matching

- Reference
  - Ch. Enz and G. C. Temes, “Circuit Techniques for Reducing the Effects of Op-Amp Imperfections,” Proc. IEEE, Nov. 1996, pp. 1584-1614.

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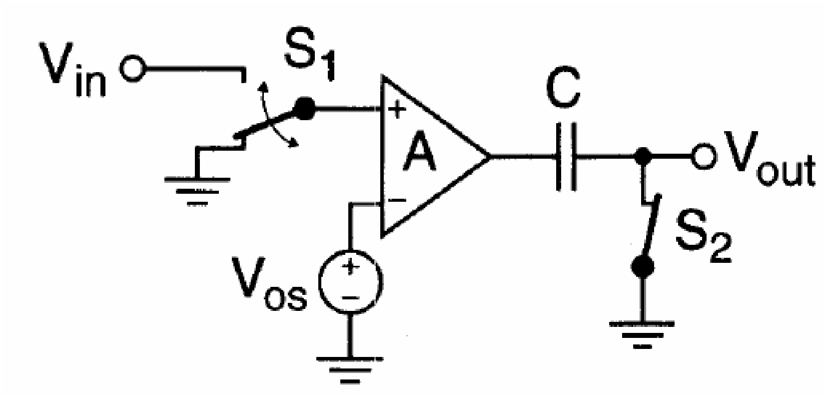
Output Offset Cancellation



- Output still corrupted by switch charge injection
  → bottom plate sampling

- Requires

$$AV_{os} < V_{DD}$$

Phase 1 :

$$V_C = -AV_{os}$$

Phase 2 :

$$V_{out} = A(V_{in} - V_{os}) - V_C$$
$$= AV_{in}$$

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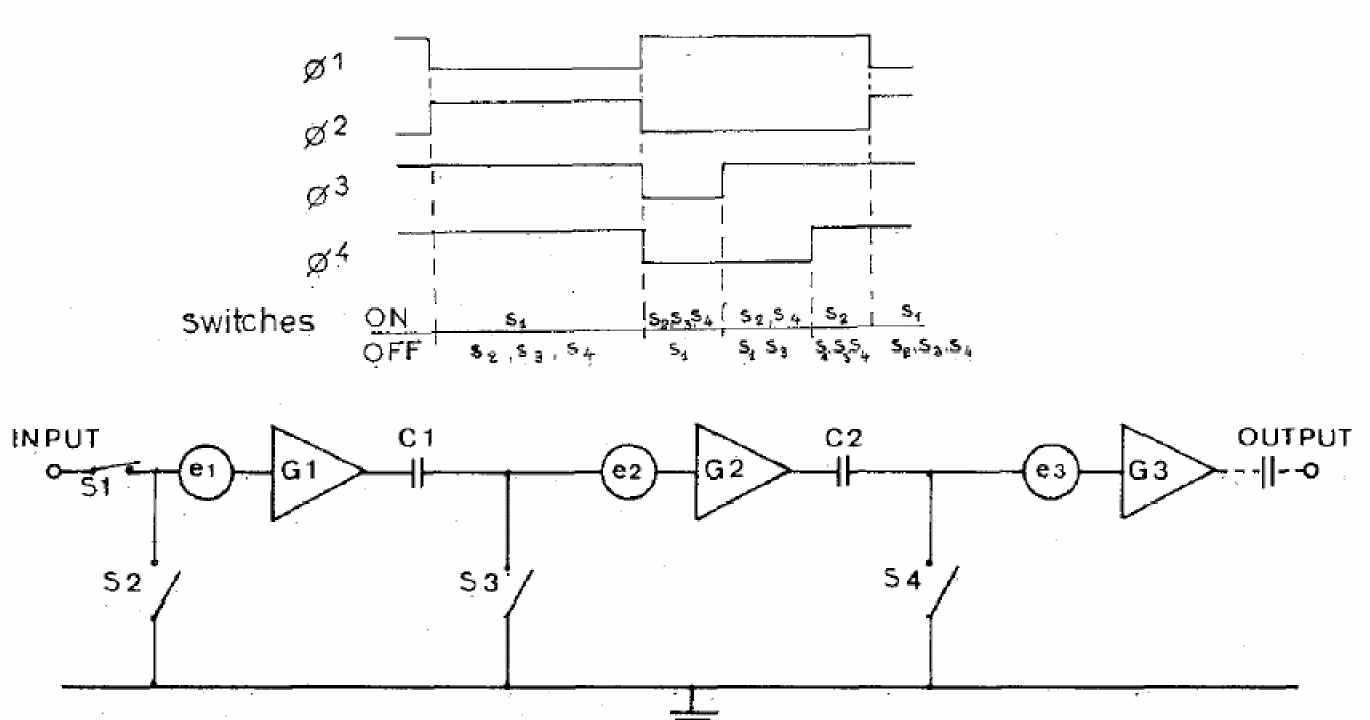
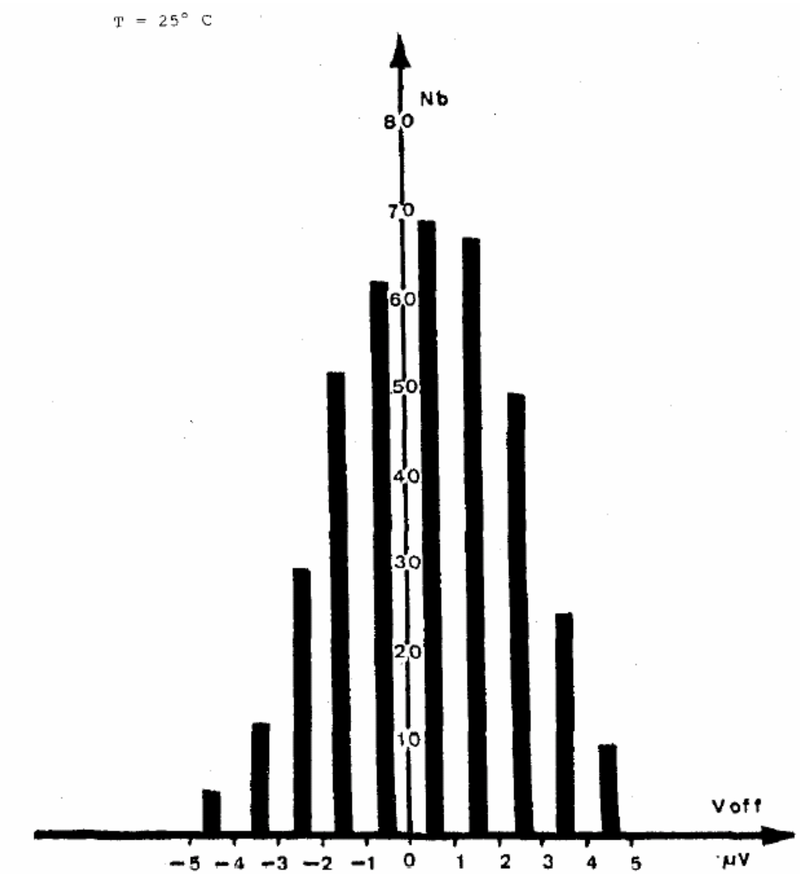
Multistage Implementation



R. Poujois and J. Borel, "A low drift fully integrated MOSFET operational amplifier," *IEEE Journal of Solid-State Circuits,* vol. 13, pp. 499 - 503, August 1978.

Results



$$\sigma_{V_{os}} < 5\mu\mathrm{V}$$

Differential implementation also uses chopper stabilization.

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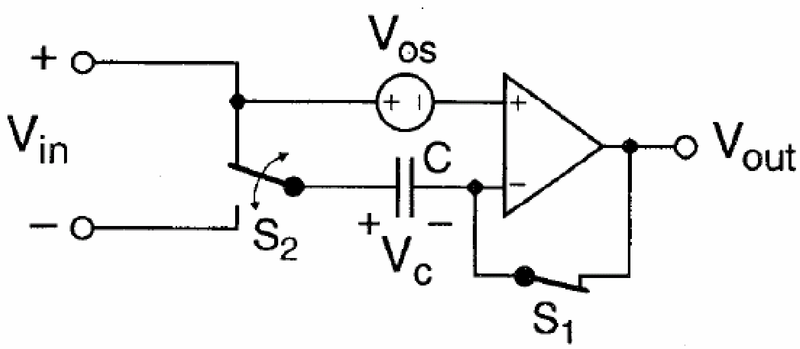
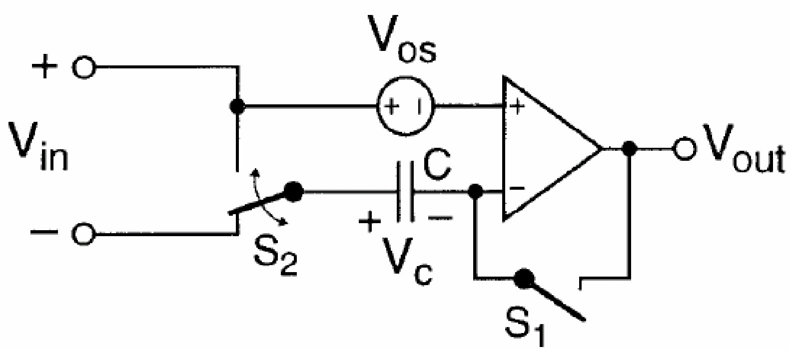
Input Offset Cancellation



(a)



(b)

Phase (a) :

$$V_o = -A(V_{os} - V_o)$$

$$V_c = -V_o = V_{os}\frac{A}{A+1}$$

Phase (b) :

$$V_o = A(V_{in} - V_{os} + V_c)$$

$$V_o = A\left(V_{in} - \frac{V_{os}}{A+1}\right)$$

$$V_{os,res} = -\frac{V_{os}}{A+1}$$

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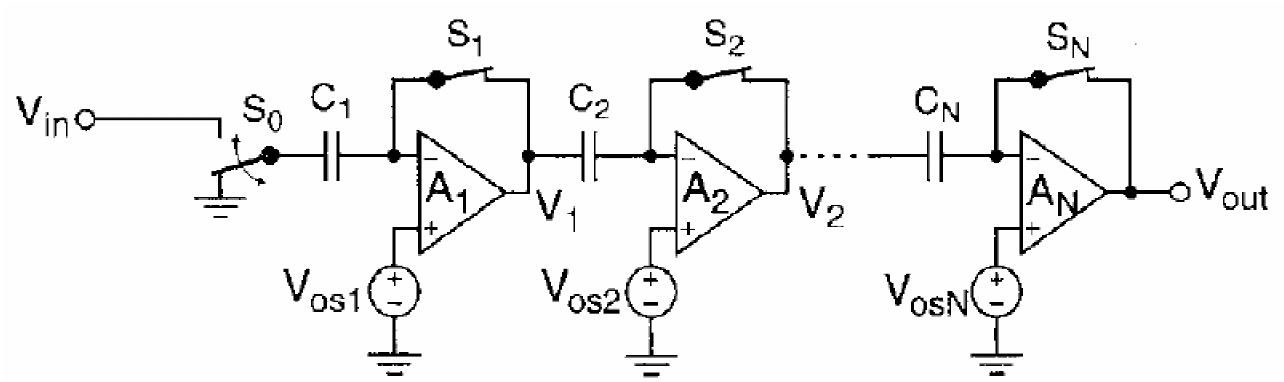
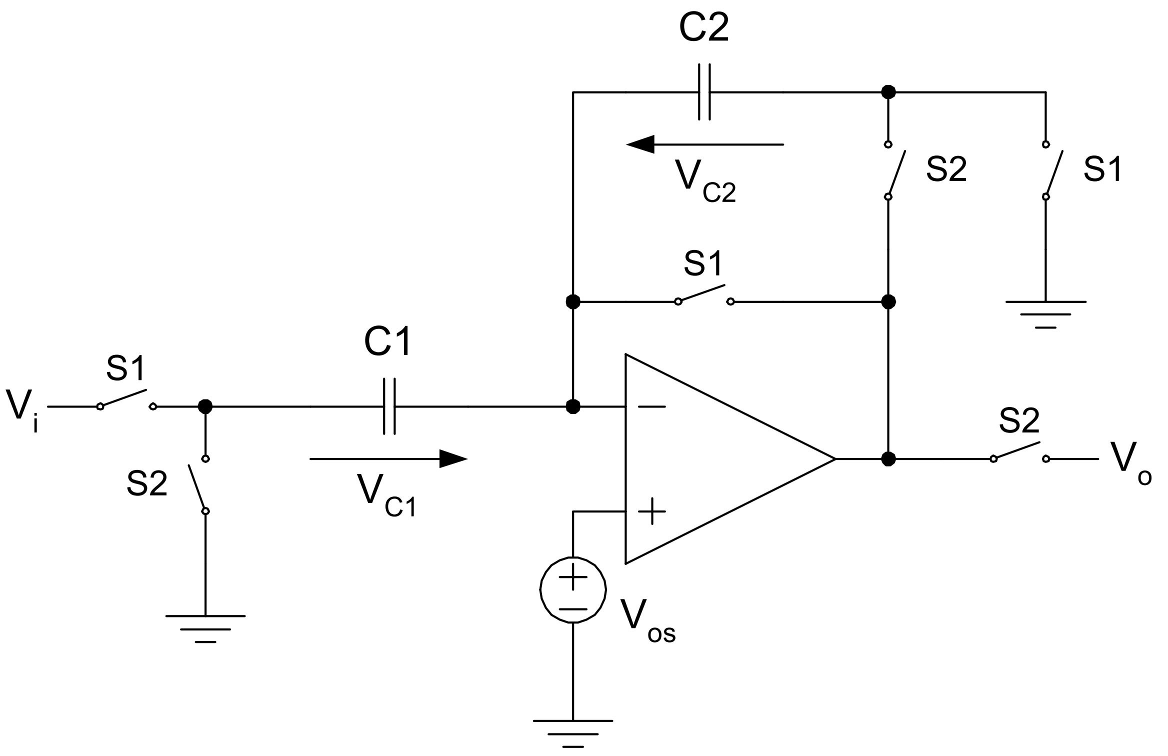
Multistage Cancellation

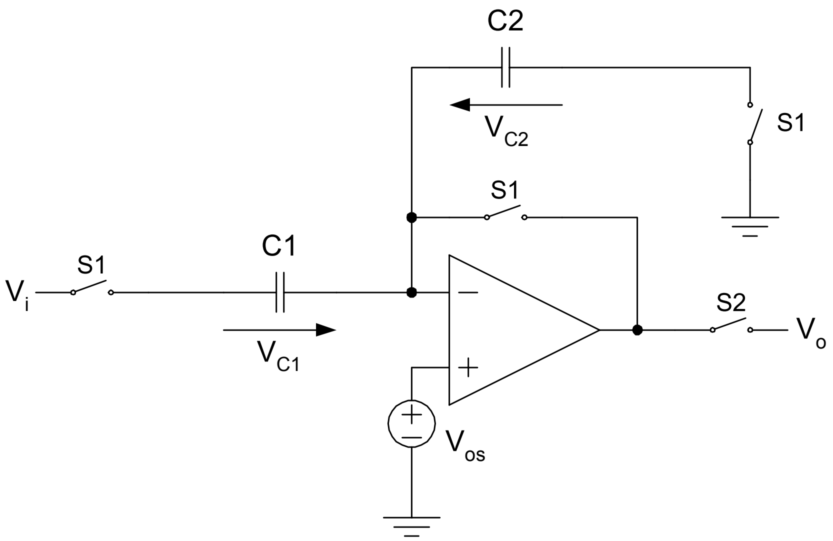


- Open switches left to right
- Residual offset from S_1 … S_{N-1} (charge injection?) cancelled by final stage
- Capacitive coupling reduces gain
- Application: comparators

Offset Compensated SC Gain Stage



SC Gain Stage: Φ_1



$$V_{C1} = V_i - V_{os}$$

$$V_{C2} = -V_{os}$$

$$Q_{tot}^{\Phi_1} = C_1 V_{C1} + C_2 V_{C2}$$
$$= C_1 V_i - (C_1 + C_2) V_{os}$$

Assuming infinite open-loop gain.

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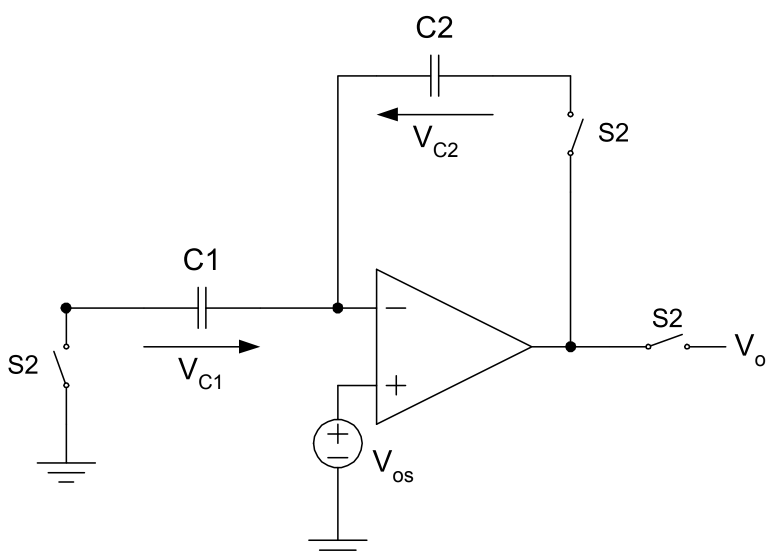
SC Gain Stage: Φ_2



- Charge on C1, C2 is redistributed
- Total charge stays same!
- At end of phase 2:

$$V_{C1} = -V_{os}$$
$$V_{C2} = V_o - V_{os}$$

$$Q_{tot}^{\Phi_2} = C_2 V_o - (C_1 + C_2) V_{os}$$
$$Q_{tot}^{\Phi_1} = C_1 V_i - (C_1 + C_2) V_{os}$$

$$Q_{tot}^{\Phi_2} = Q_{tot}^{\Phi_1} \rightarrow$$
$$V_o = \frac{C_1}{C_2} V_i$$

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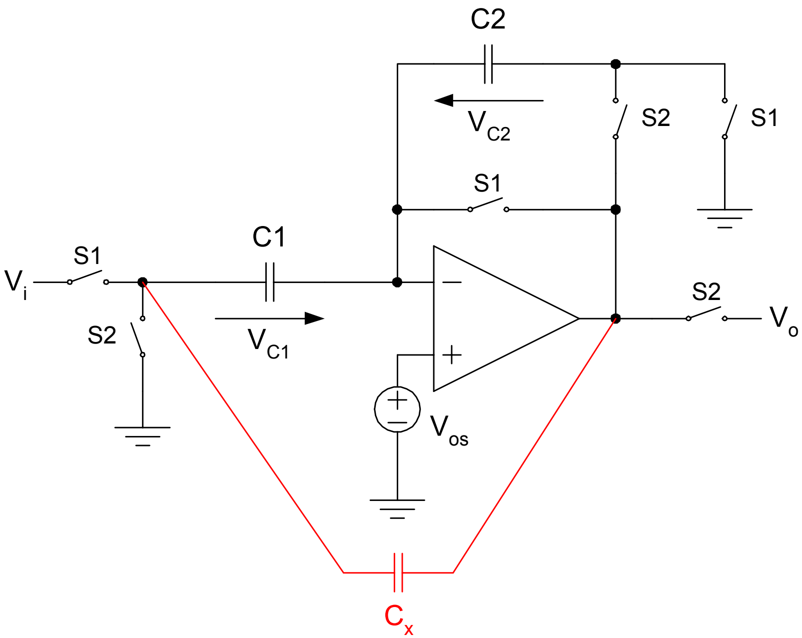
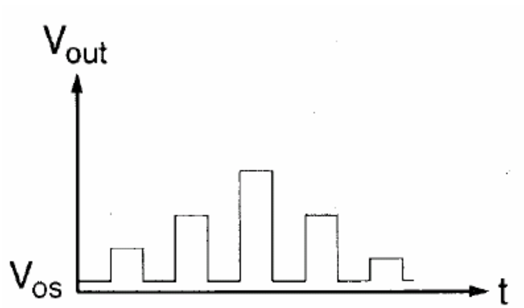
SC Gain Stage Implementation





- Amplifier must be unity-gain stable
- Output pulled back to V_{os} in each cycle
- No feedback during clock non-overlap → C_x
- Charge injected at input node

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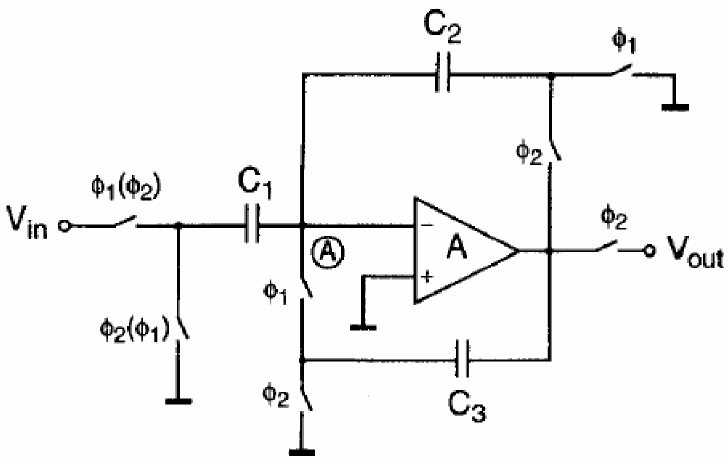
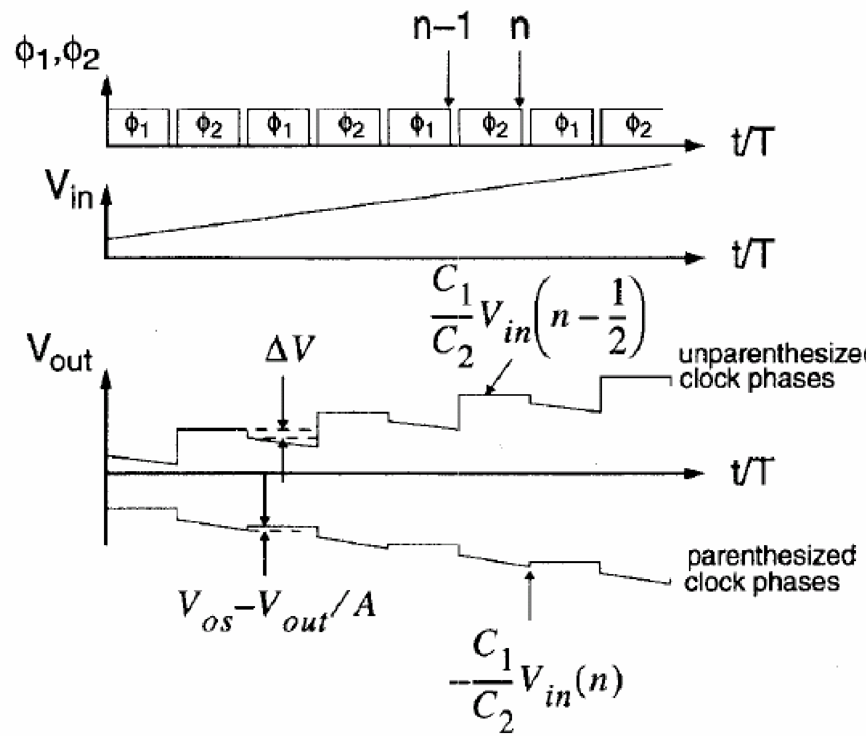
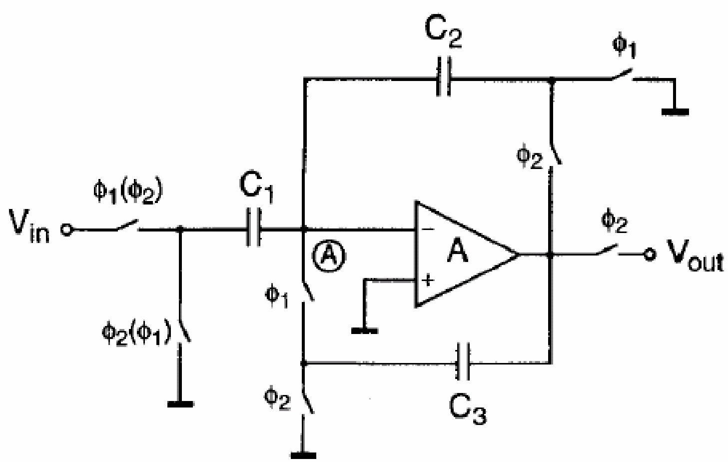
Gain Compensated SC Stage





Clocks in parentheses are for inverting operation.

Gain Compensated SC Stage

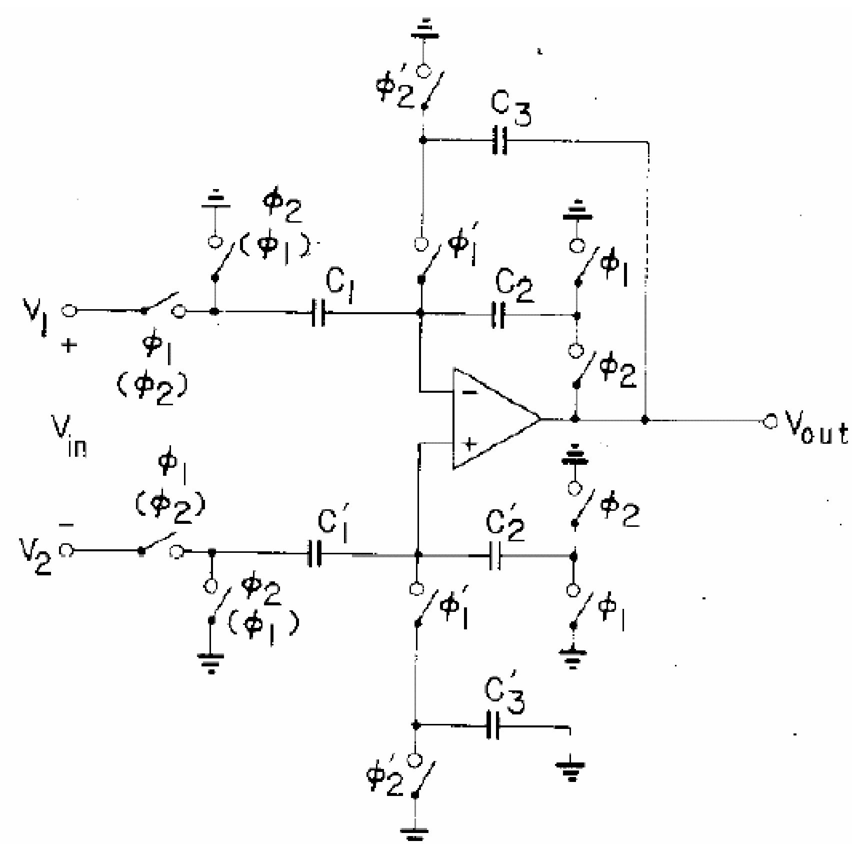


- C_3 replaces unity-gain feedback reset
- C_3 charged to V_{out} during Φ_2
- Output never reset (to zero)
- Reduced slewing requirement
- Reduced static error:

$$\frac{V_{out}}{V_{in}} = \frac{C_1}{C_2} \frac{1}{1 + \frac{1 + \frac{C_1}{C_2}}{\underline{\underline{A^2}}}}$$

- Lowdown: works only for highly oversampled inputs!

Gain Compensated SC Stage



- V_{os} = 5 … 10mV
- CMRR = 50dB
- Distortion: 0.1 … 0.2%
- Is it worth it?

K. Martin, L. Ozcolak, Y. S. Lee, and G. C. Temes, "A differential switched-capacitor amplifier," *IEEE Journal of Solid-State Circuits,* Vol. 22, pp. 104 - 106, February 1987.

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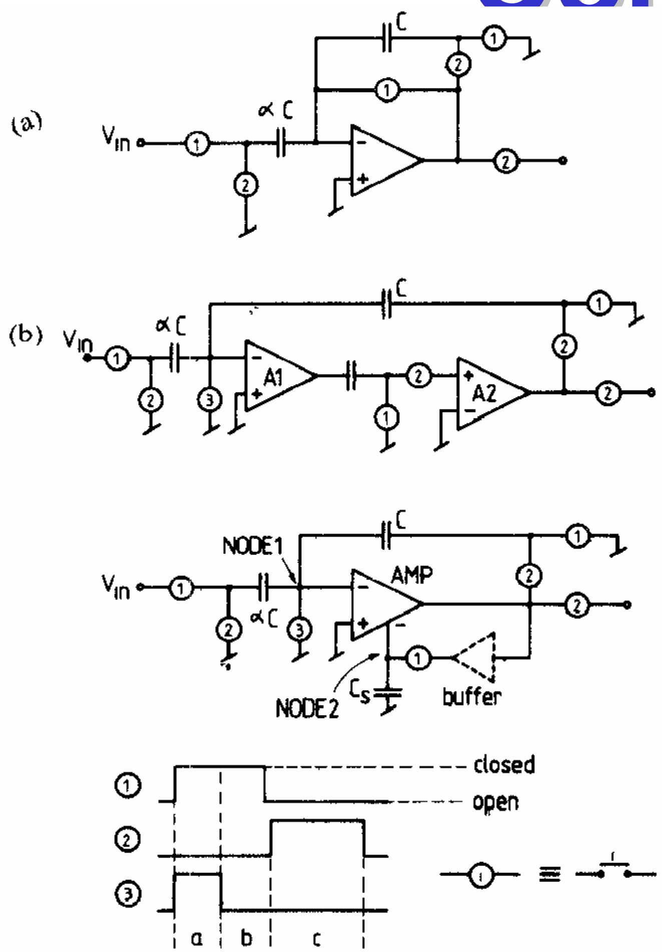
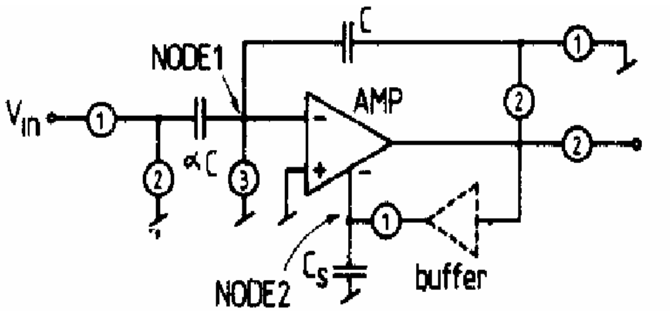
Offset Cancellation Comparison

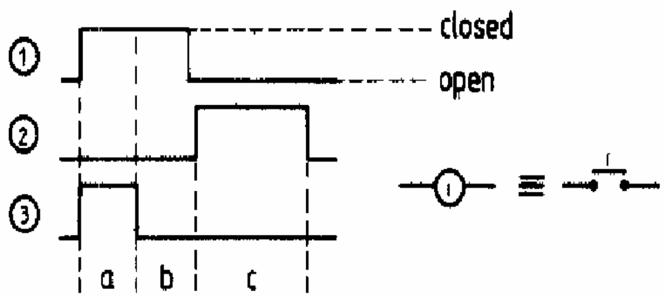


- Offset cancellation options
  - At input
  - At output (of first gain stage)
  - At input of auxiliary amp

M. Degrauwe, E. Vittoz, and I. Verbauwhede, "A micropower CMOS-instrumentation amplifier," *IEEE Journal of Solid-State Circuits,* vol. 20, pp. 805 - 807, June 1985.

Auxiliary Amplifier Offset Cancellation





$$V_{out} = \underbrace{-A_1\left(V_1 - V_{OS1}\right)}_{\text{main amp}} \underbrace{- A_2\left(V_2 - V_{OS2}\right)}_{\text{aux amp}}$$

$$V_2 = V_o = A_1 V_{OS1} - A_2\left(V_2 - V_{OS2}\right)$$

$$V_2 = \frac{A_1}{1+A_2}\left(V_{OS1} + V_{sw1}\right) + \frac{A_2}{1+A_2} V_{OS2} + V_{sw2}$$

$$V_{out} = A_1 V_{OS1} - A_2 V_2 + A_2 V_{OS2}$$

$$= A_1 \left(\underbrace{\frac{V_{OS1} + V_{sw1}}{1+A_2} + \frac{A_2}{A_1}\frac{A_2}{1+A_2} V_{OS2} + \frac{A_2}{A_1} V_{sw2}}_{\text{input referred offset}} \right)$$

Switch Charge Injection :

V_{sw1} : phase a, node 1

V_{sw2} : phase b, node 2

→ Offset, charge injection attenuated if $A_1 >> A_2$

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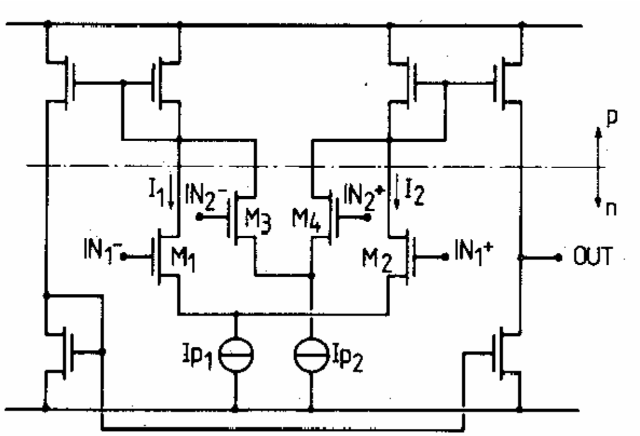
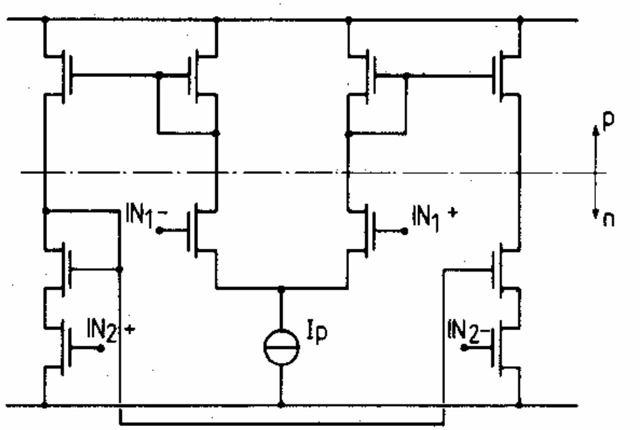
Aux Amp Options

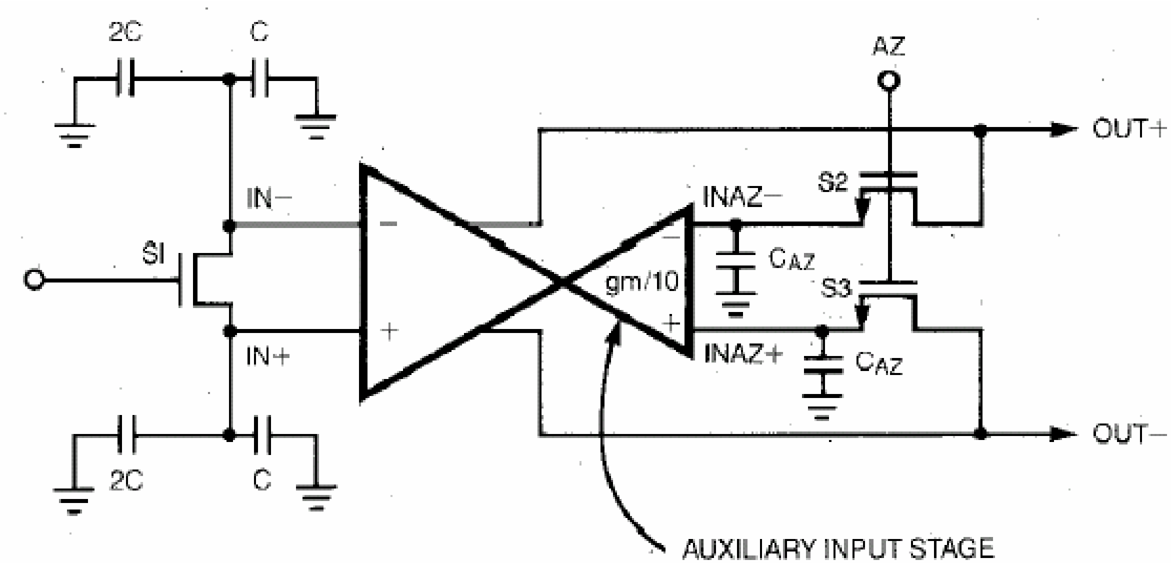




Gain (= α C/C)	20 dB
Max. clock frequency (C_L = 22 pF)	8 kHz
Offset (at 8 kHz) $\bar{x}$	90 µV
Offset (at 8 kHz) σ	370 µV
Equivalent input noise (0.5 Hz-4 kHz)	79 µV
No 1/f noise was observed above 0.5 Hz (= under limit of measurement equipment)	
CMRR	> 95 dB
Current consumption	7 µA
$PSRR^-$ (at DC)	54 dB
$PSRR^+$ (at DC)	66 dB

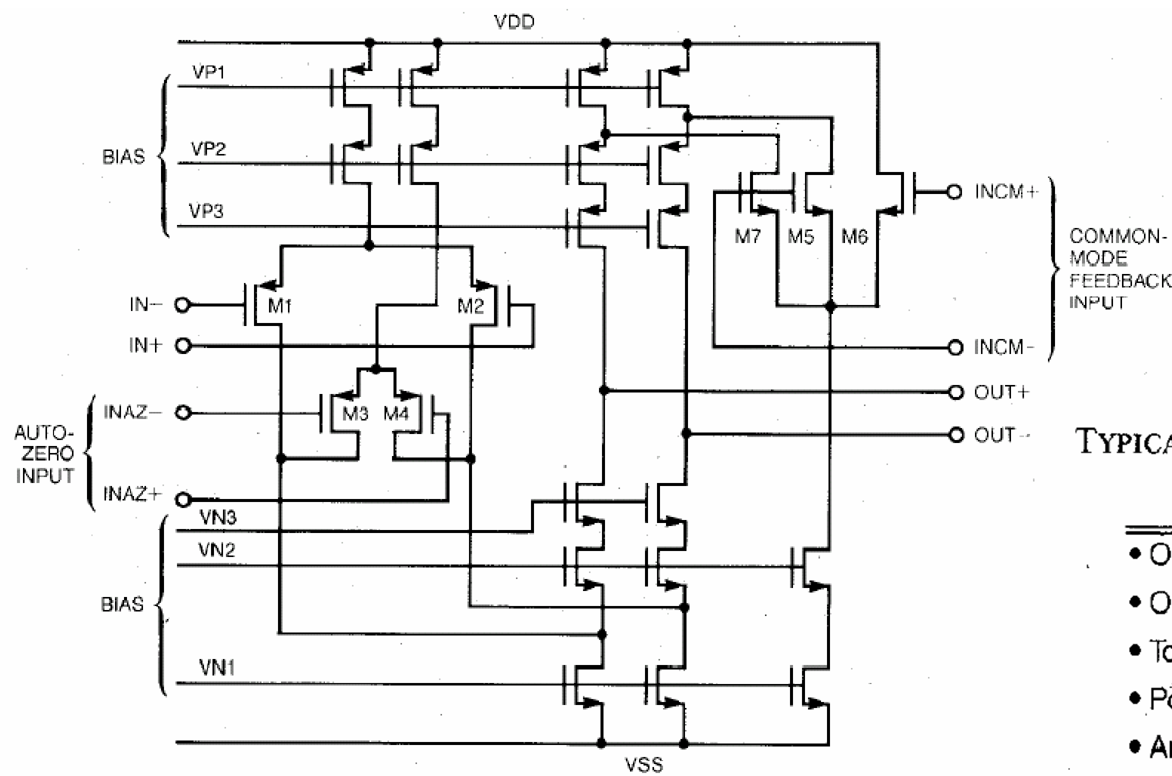
M. Degrauwe, E. Vittoz, and I. Verbauwhede, "A micropower CMOS-instrumentation amplifier," *IEEE Journal of Solid-State Circuits,* vol. 20, pp. 805 - 807, June 1985.

Precision Gain Stage



H. Ohara, H. X. Ngo, M. J. Armstrong, C. F. Rahim, and P. R. Gray, "A CMOS programmable self-calibrating 13-bit eight-channel data acquisition peripheral," *IEEE Journal of Solid-State Circuits,* vol. 22, pp. 930 - 938, December 1987.

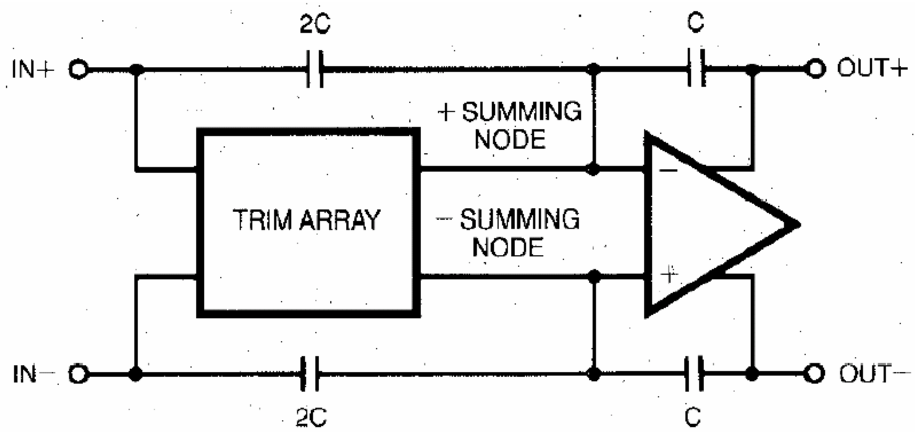
Amplifier with Auxiliary Input

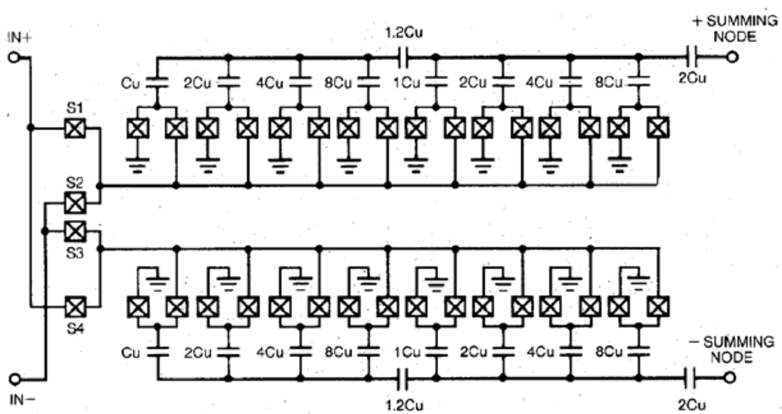


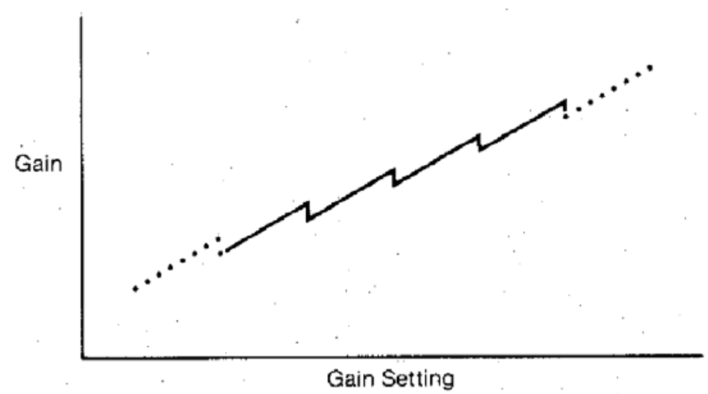
TYPICAL AMPLIFIER PERFORMANCE PARAMETERS
(± 5 V; 25°C)

- Open loop gain: 125 dB
- Output voltage swing: within 1.5 V of rails
- Total settling time to 0.01%, 6 volt step: 300 ns
- Power dissipation: 30 mW
- Area: 1700 square mils
- Offset: 300 μV

Gain Trimming







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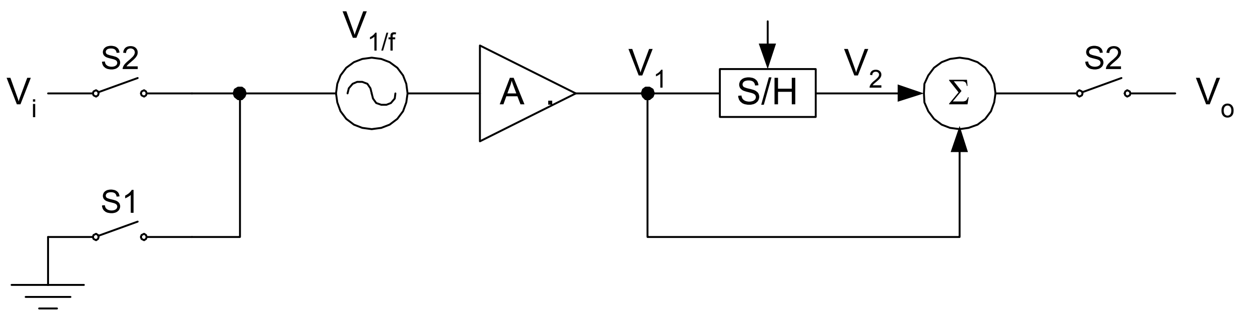
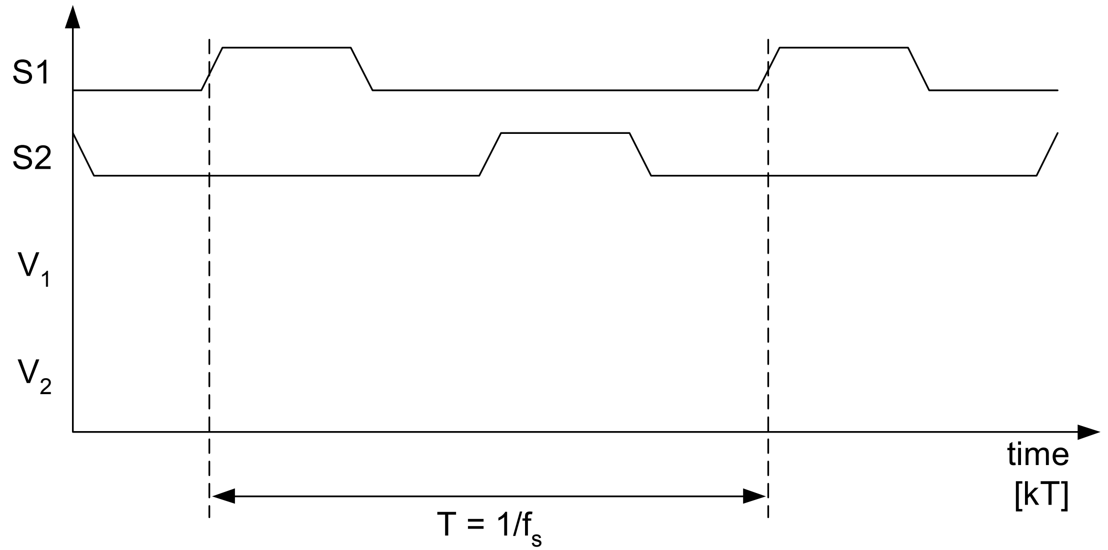
CDS and Flicker Noise





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Flicker Noise Analysis

$$V_o(kT) = A\left\{\underbrace{V_i(kT)}_{\text{signal}} + \underbrace{V_{1/f}(kT) - V_{1/f}\left(kT - \frac{T}{2}\right)}_{\text{input referred error } V_{nieq}}\right\}$$

<u>Laplace Transform</u>

$$\text{Delay by } t_d \quad \rightarrow \quad e^{-st_d}$$

$$V_{nieq}(s) = V_{1/f}(s)\underbrace{\left\{1 - e^{-s\frac{T}{2}}\right\}}_{H_n(s)}$$

Flicker Noise Frequency Response

$$H_n(s) = 1 - e^{-s\frac{T}{2}}$$

$$= 1 - e^{-j\omega\frac{T}{2}}$$

$$= 1 - \cos\frac{\omega T}{2} + j\sin\frac{\omega T}{2}$$

$$\left|H_n(s)\right|^2_{s\to j\omega} = \left(1 - \cos\frac{\omega T}{2}\right)^2 + \left(\sin\frac{\omega T}{2}\right)^2$$

$$= 1 - 2\cos\frac{\omega T}{2} + \underbrace{\cos^2\frac{\omega T}{2} + \sin^2\frac{\omega T}{2}}_{1}$$

$$= 2\left(1 - \cos\frac{\omega T}{2}\right)$$

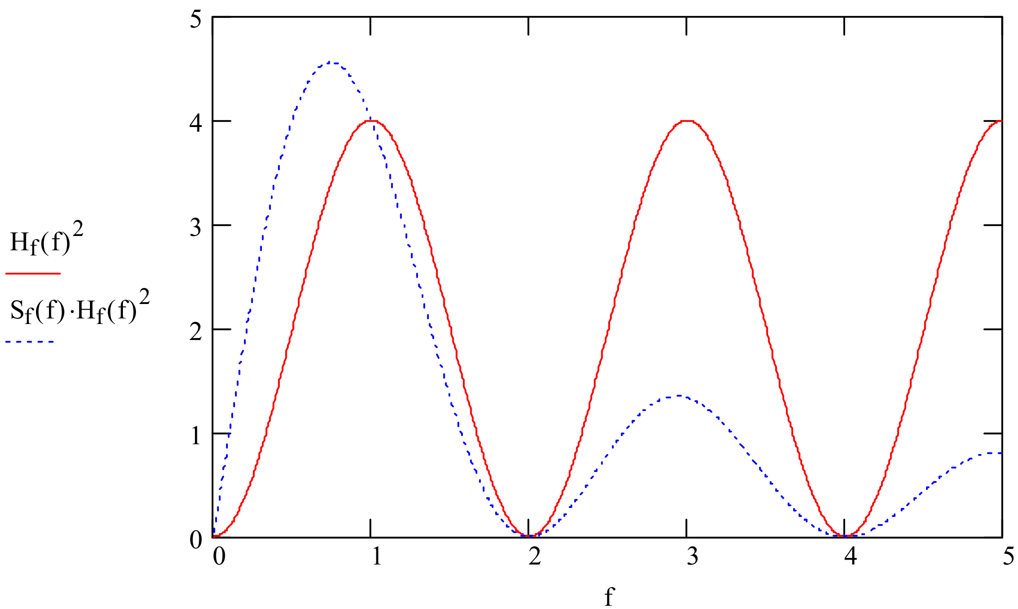
$$= 4\sin^2\frac{\omega T}{4}$$

$$\boxed{\left|H_n(s)\right|_{s\to j\omega} = \left|2\sin\frac{\omega T}{4}\right| = \left|2\sin\frac{\pi f}{2 f_s}\right|}$$

Flicker Noise Spectrum

$$K := 1 \qquad f_s := 1$$

$$S_f(f) := \frac{K}{f} \qquad H_f(f) := \left| 2 \cdot \sin\left(\frac{\pi \cdot f}{2 \cdot f_s} \right) \right|$$



- Flicker noise is differentiated
- Essentially removed at low frequency
- Choosing $f_s/2$ sufficiently large effectively removes flicker noise
- Noise above $f_s/2$ folds to baseband
- Thermal noise folded to 0 … $f_s/2$

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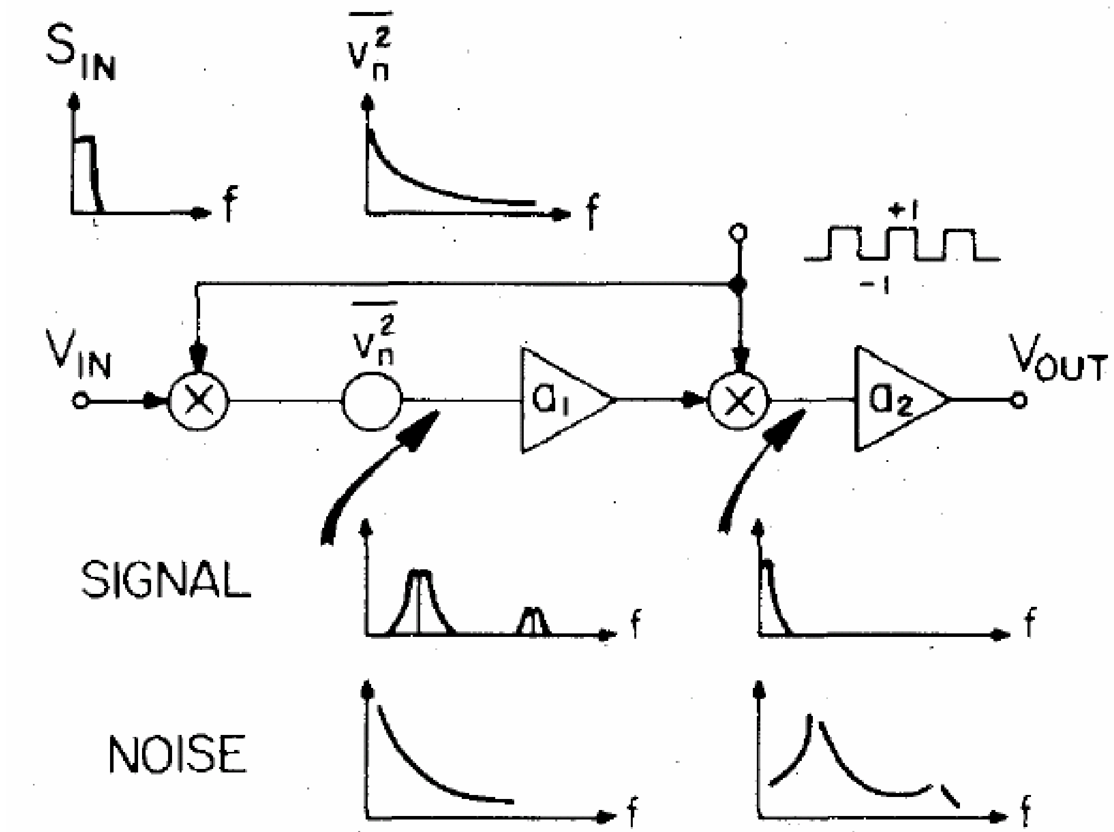
Chopper Stabilization



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Chopper Amp Bandwidth & Delay

Example 1:

Amplifier is ideal LPF

- Gain A_o
- BW 2 f_s

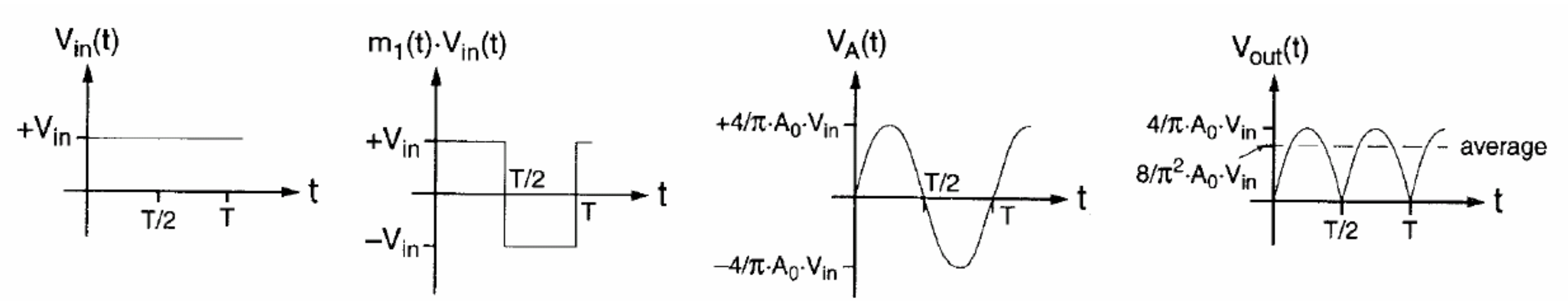
→ DC gain ~ 0.8 A_o

Example 2:

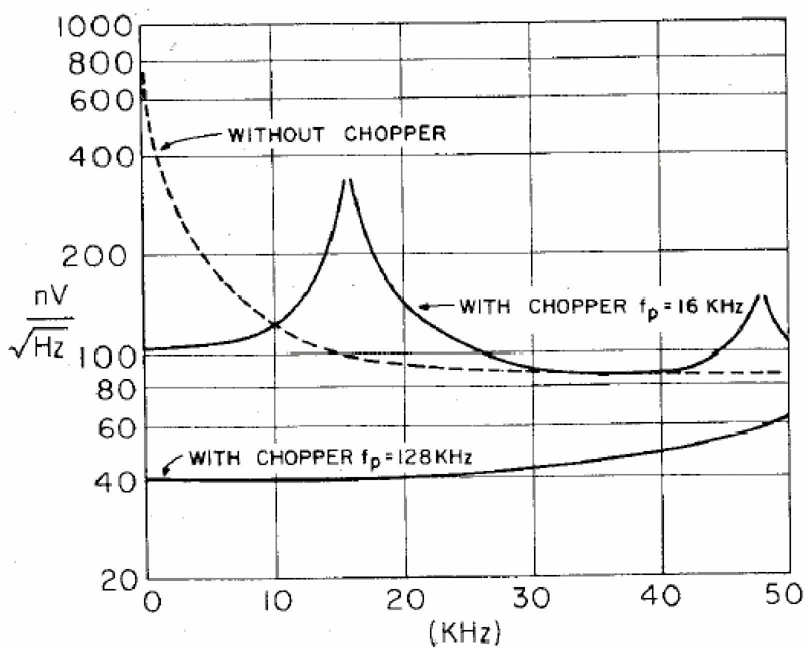
Amplifier introduces 90° phase shift

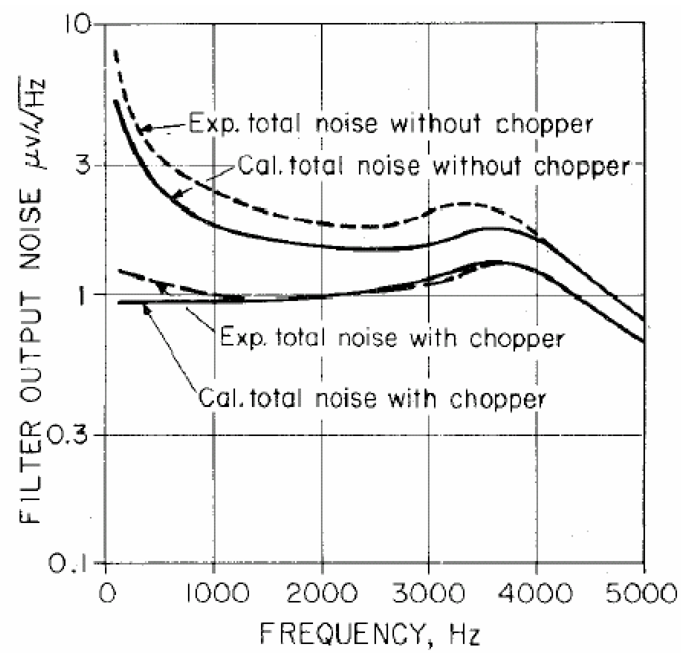
→ DC gain is 0

$$\cos x \cos y = \tfrac{1}{2}\left[\cos(x-y)+\cos(x+y)\right]$$
$$\sin x \cos y = \tfrac{1}{2}\left[\sin(x-y)+\sin(x+y)\right]$$



Chopper Results





K. Hsieh, P. R. Gray, D. Senderowicz, and D. G. Messerschmitt, "A low-noise chopper-stabilized differential switched-capacitor filtering technique," *IEEE Journal of Solid-State Circuits,* vol. 16, pp. 708 - 715, December 1981.

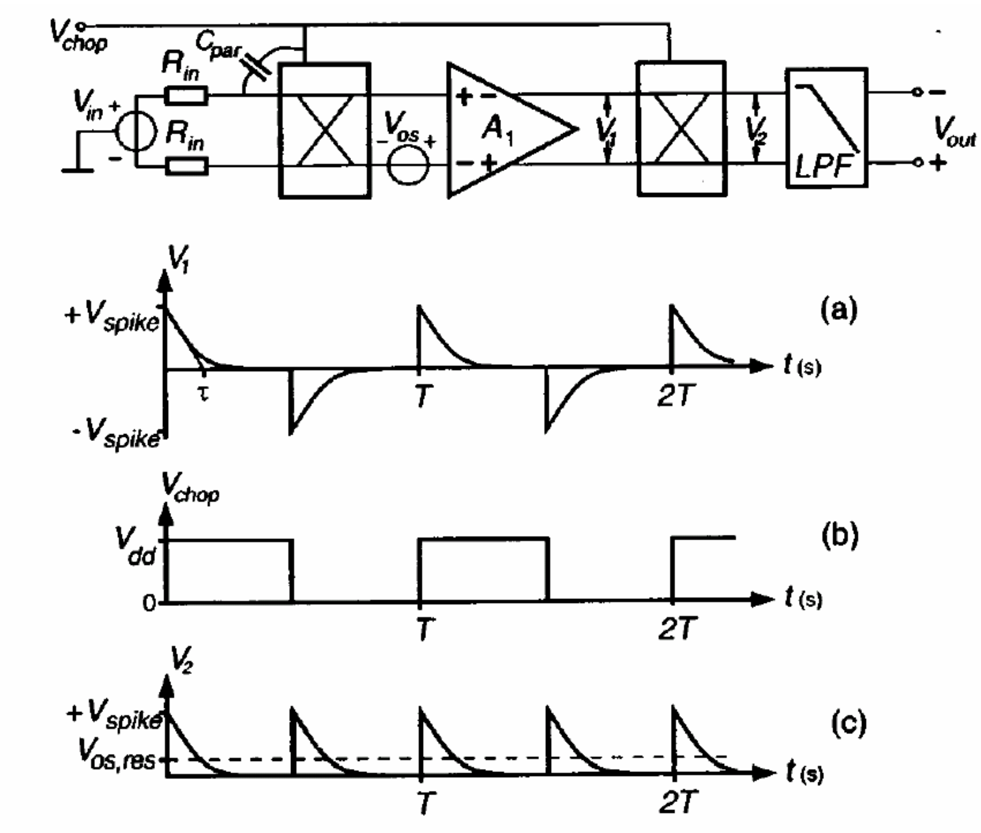
LINEAR TECHNOLOGY

LTC1050

Precision Zero-Drift Operational Amplifier with Internal Capacitors

- Offset: 0.5μV
- Offset drift: 0.01μV/°C
- Input noise: 1.5μ$V_{p\text{-}p}$ DC … 10Hz → 480nV/rt-Hz avg
- Open-loop gain: 160dB
- Slew rate: 4V/μS
- Unity-gain bandwidth: 4MHz
- PSRR: 125dB
- CMRR: 120dB

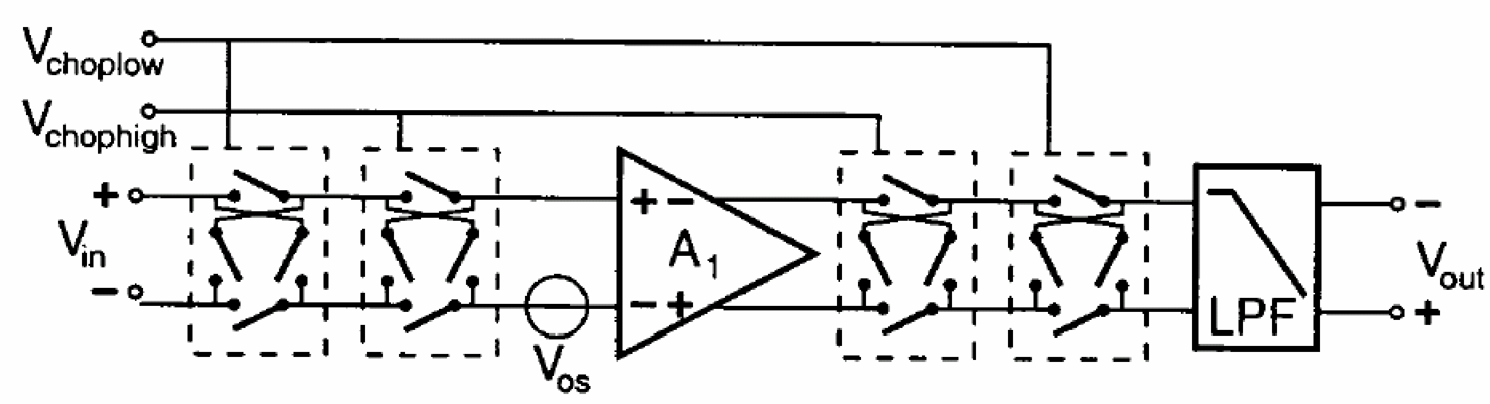
Chopper Residual Offset



Spikes from input chopper due to charge injection mismatch.

A. Bakker, K. Thiele, and J. H. Huijsing, "A CMOS nested-chopper instrumentation amplifier with 100-nV offset," *IEEE Journal of Solid-State Circuits,* vol. 35, pp. 1877 - 1883, December 2000.

Nested Chopper Amplifier



- Inner chopper runs at high frequency to remove 1/f noise
- Outer chopper runs at low frequency to minimize “spiking” and remove residual offset from inner chopper. 1/f-noise is no issue since it has been reduced by inner chopper.

Results

	Typ	Unit
Supply voltage	5	V
Supply current	200	uA
High chopping frequency	2	kHz
Low chopping frequency	16	Hz
Offset	100	nV
Offset temperature coefficient (20-50^{o}C)	3	nV/^{o}C
Noise (input referred, 0.1-3Hz)	27	nV/sqrt(Hz)
CMRR (0.1-3Hz)	140	dB

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Comparison

CDS

- Samples Signal
  - No continuous time operation (except ping-pong)
- Flicker noise removed
  - No need for LPF
- Increased baseband noise due to thermal noise folding
- Can enhance amplifier gain

Chopper Stabilization

- Modulates Signal
  - Compatible with continuous time operation
- Flicker noise to high frequency
  - Requires LPF to remove noise
- Virtually no thermal noise folding if $f_{clk} >> B$
- Finite BW amp reduces gain

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