EECS 240
Analog Integrated Circuits

Topic 18: MOS S/H

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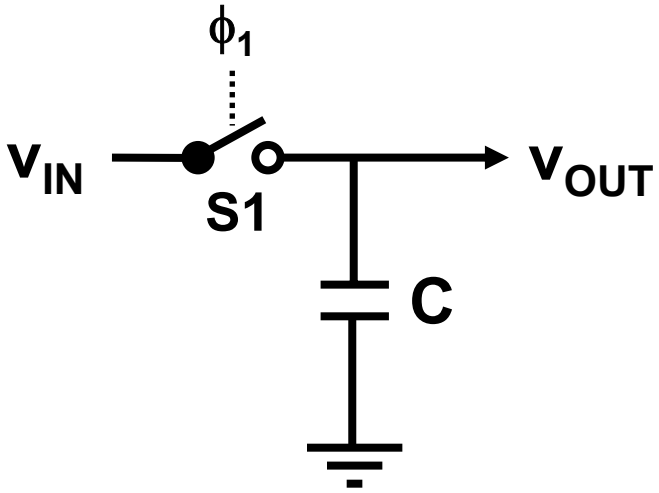
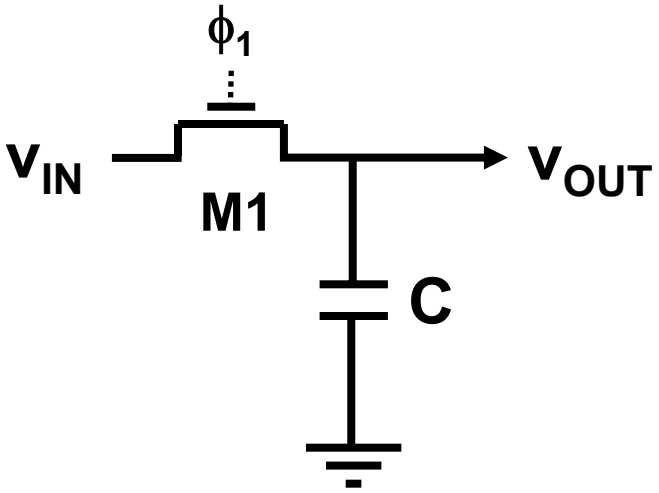
MOS Sample & Hold

Ideal Sampling



- Grab exact value of V_{in} when switch opens

Practical Sampling



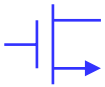
- kT/C noise
- Finite R_{sw} → limited bandwidth
- $R_{sw} = f(V_{in})$ → distortion
- Switch charge injection
- Clock jitter

kT/C Noise

$$\frac{k_B T}{C} \leq \frac{\Delta^2}{12}$$

$$C \geq 12 k_B T \left(\frac{2^B - 1}{V_{FS}} \right)^2$$

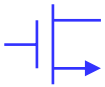
B [bits]	C_{min} (V_{FS} = 1V)
8	0.003 pF
12	0.8 pF
14	13 pF
16	206 pF
20	52,800 pF



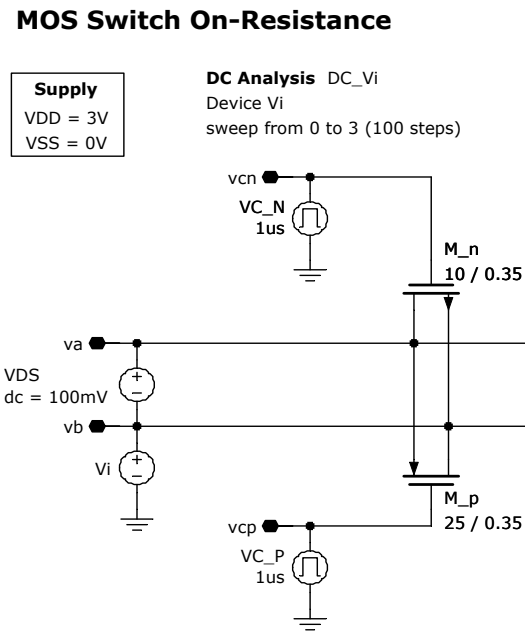
MOSFET as Resistor

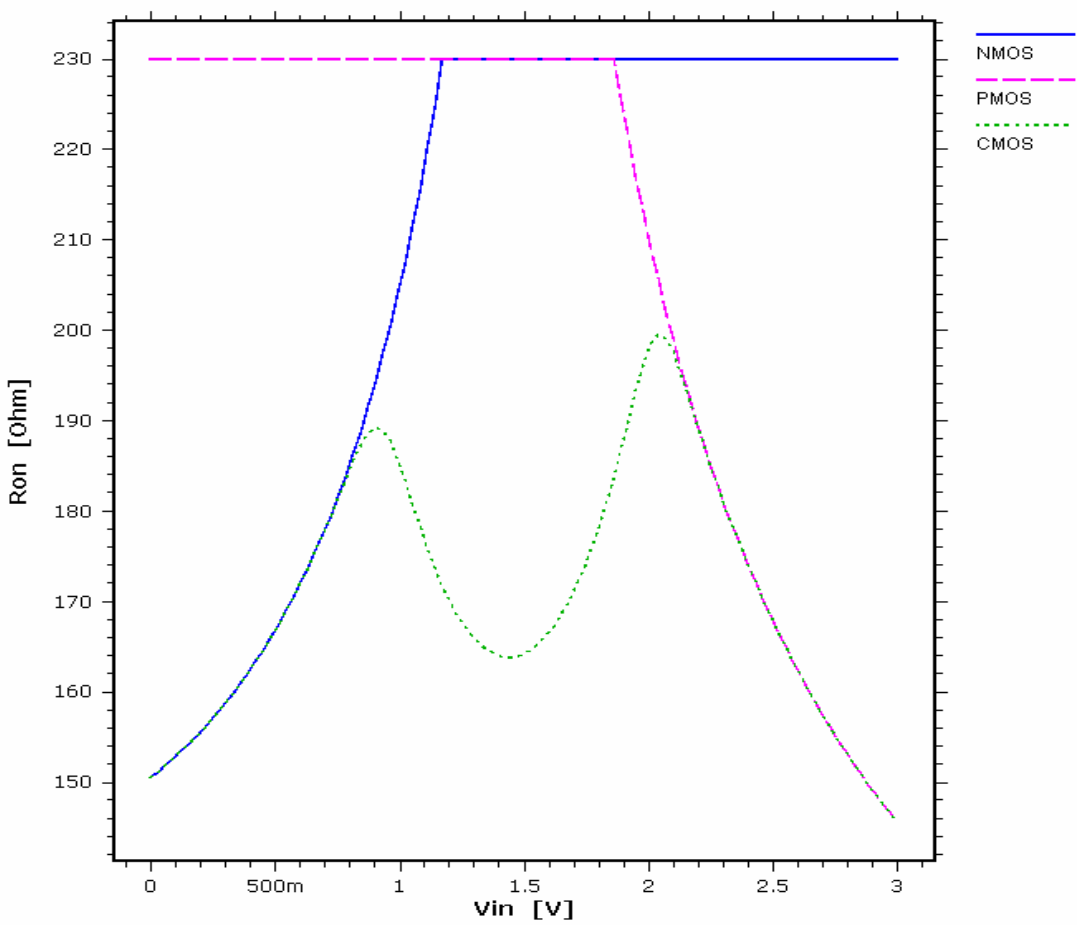
- "off" state
  - R_{off}
  - I_{off} … beware of subthreshold conduction
  - Capacitive coupling
  - T-switch

- "on" state
  - Operate in triode region with V_{DS} small
  - Nonlinear
  - Threshold voltage, Body effect
  - N/P/C-MOS
  - Constant V_{GS} switch



Switch On-Resistance

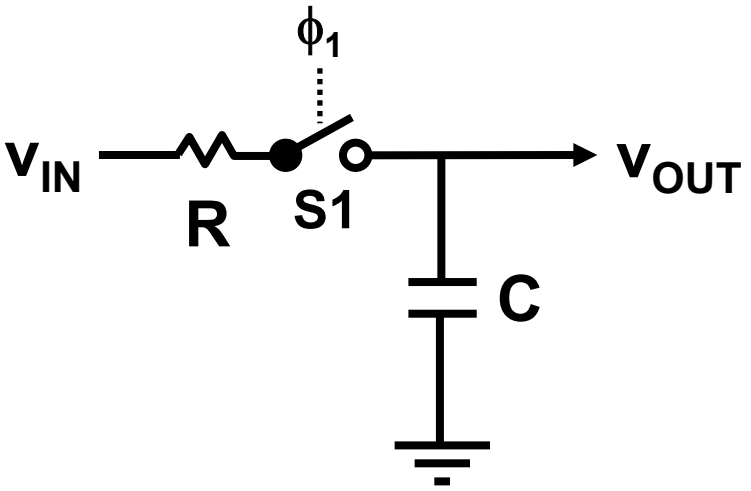




Acquisition Bandwidth

- The resistance R of switch S1 turns the sampling network into a lowpass filter with risetime = RC = τ

- Assuming V_{in} is constant during the sampling period and C is initially discharged (a good idea—why?):



$$v_{out}(t) = v_{in}\left(1 - e^{-t/\tau}\right)$$

Switch On-Resistance

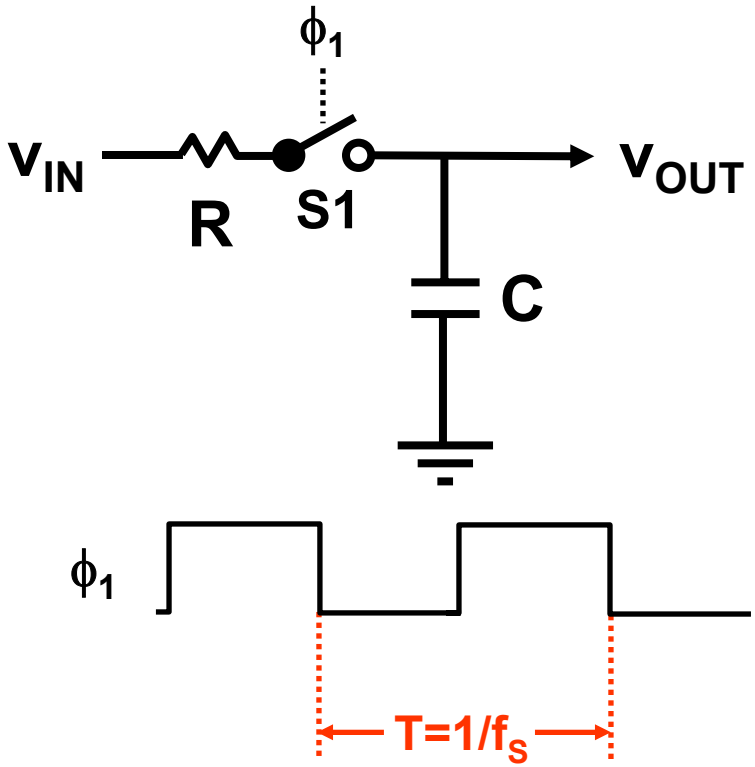
$$v_{in} - v_{out}\left(t = \frac{1}{2f_s}\right) << \Delta$$

$$v_{in} e^{-1/2 f_s \tau} << \Delta$$

$$\text{Worst Case}: \quad v_{in} = V_{FS}$$

$$\tau << \frac{T}{2}\frac{1}{\ln\left(2^B - 1\right)} \approx \frac{0.72T}{B}$$

$$R << \frac{0.72}{f_s CB}$$



Example:

B = 14, C = 13pF, f_s = 100MHz

T/τ >> 19.4, R << 40Ω

Switch On-Resistance

$$I_{D(triode)} = \mu C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS}$$

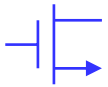
$$\frac{1}{R_{ON}} \cong \left.\frac{dI_{D(triode)}}{dV_{DS}}\right|_{V_{DS}\to 0}$$

$$R_{ON} = \frac{1}{\mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)}$$

$$= \frac{1}{\mu C_{ox}\frac{W}{L}\left(V_{DD} - V_{TH} - v_{in}\right)}$$

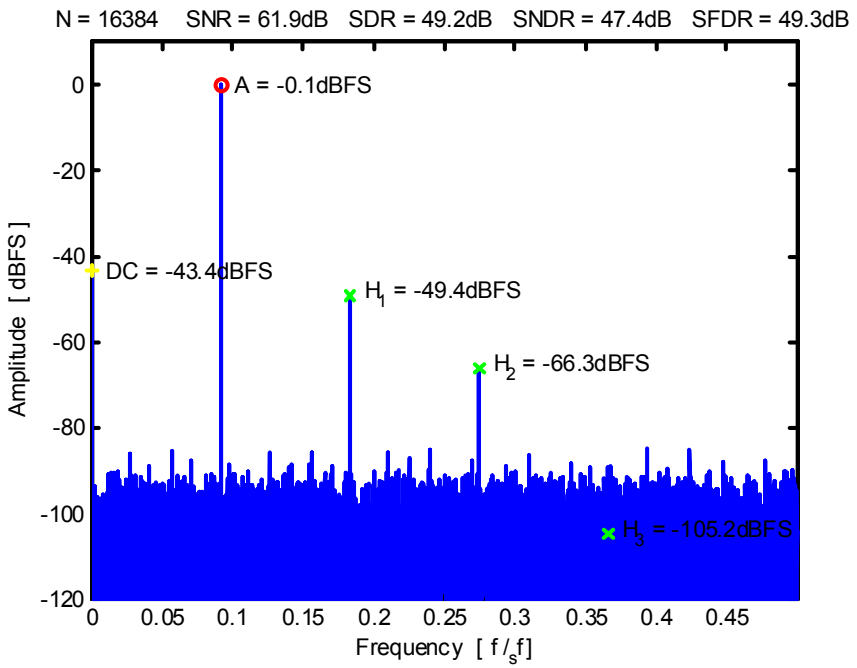
$$= \frac{R_o}{1 - \frac{v_{in}}{V_{DD} - V_{TH}}} \qquad \text{with} \qquad R_o = \frac{1}{\mu C_{ox}\frac{W}{L}\left(V_{DD} - V_{TH}\right)}$$

$$R_{ON} = \frac{R_o}{1 - \frac{v_{in}}{V_{DD} - V_{TH}}}$$



Sampling Distortion

$$v_{out} = v_{in}\left(1 - e^{-\frac{T}{2\tau}\left(1-\frac{v_{in}}{V_{DD}-V_{TH}}\right)}\right)$$

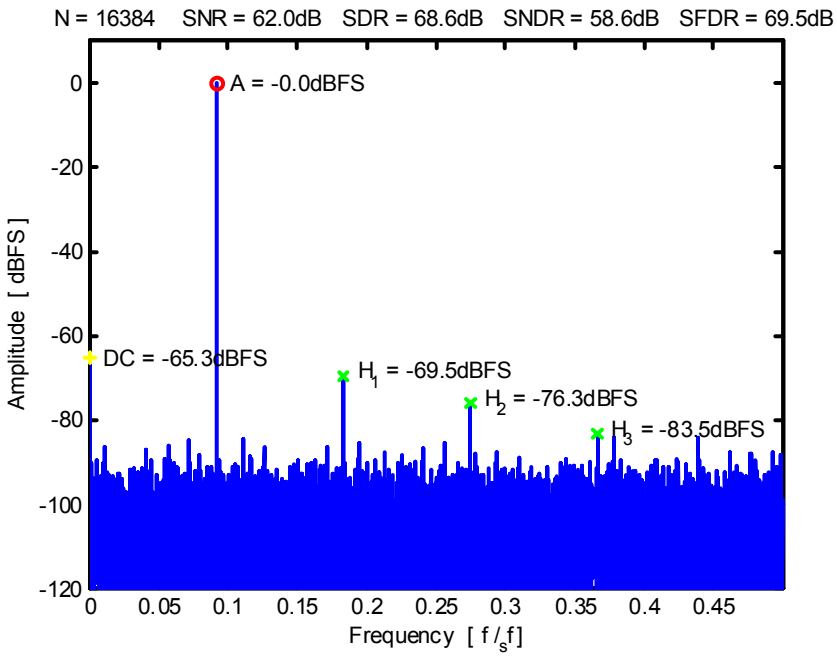


$T/\tau = 10$

$V_{DD} - V_{TH} = 2V$ $V_{FS} = 1V$

Sampling Distortion

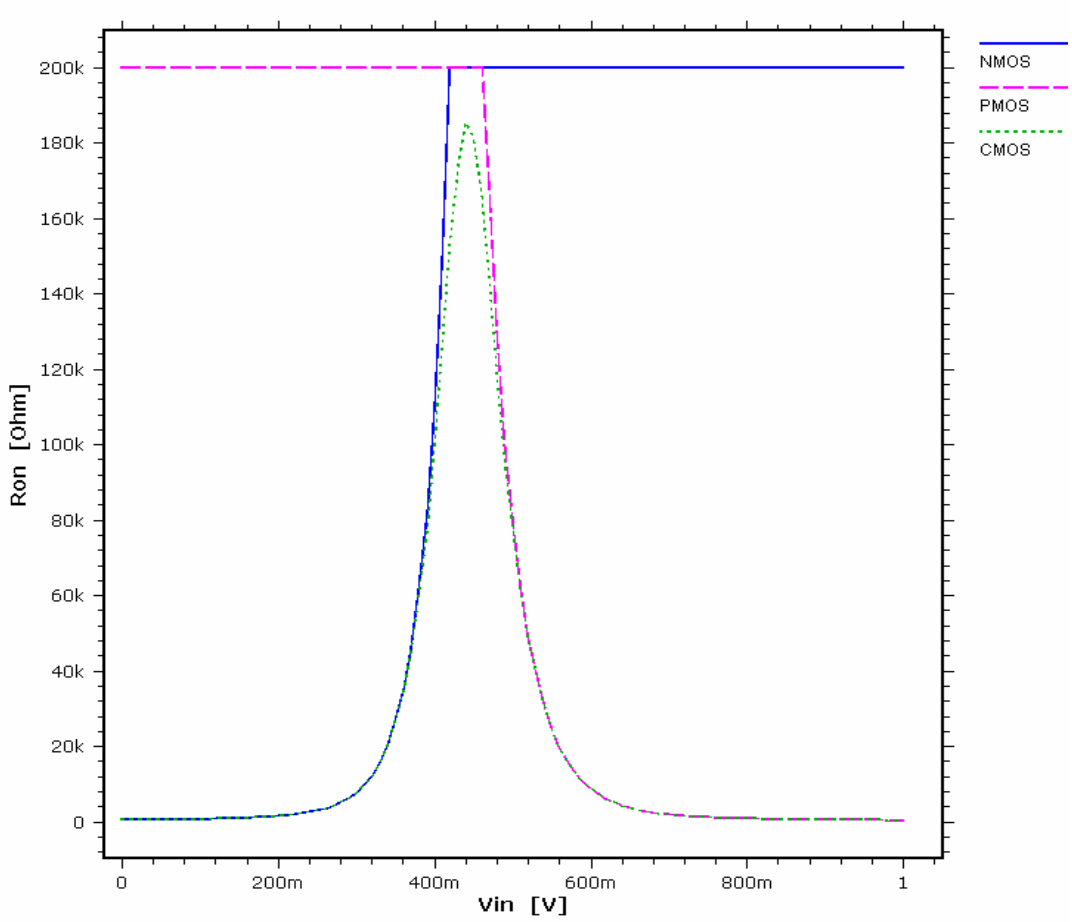
- SFDR is very sensitive to sampling distortion
- Solutions:
  - Overdesign switches
    → increased switch charge injection
    → increased clock pwr
  - Complementary switch
  - Large V_{DD}/V_{FS}
    → increased noise
  - Constant $V_{GS} \neq f(V_{in})$
    → …



T/τ = **20**

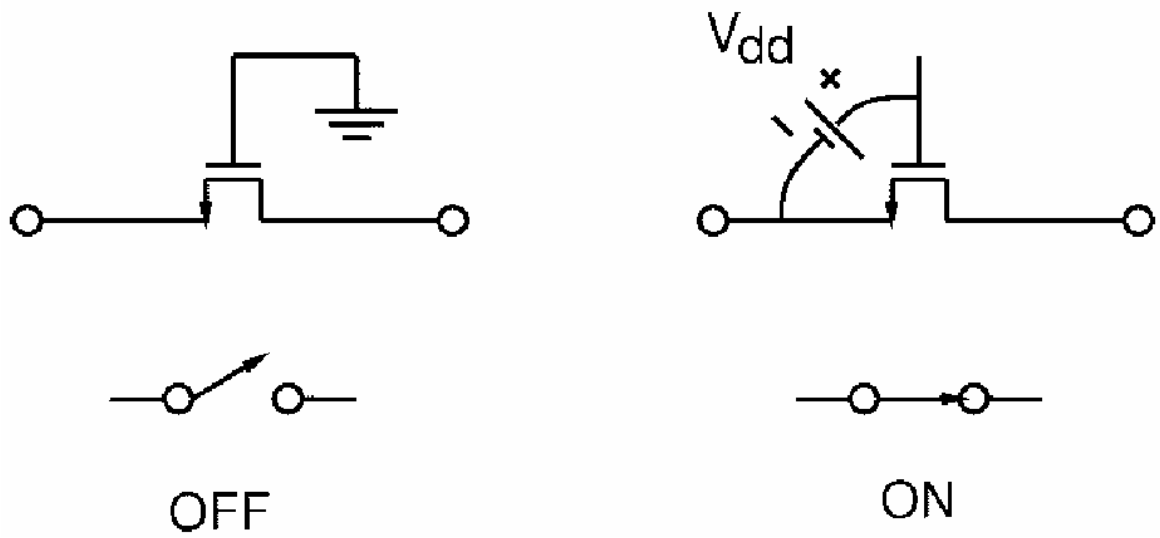
$V_{DD} - V_{TH}$ = 2V V_{FS} = 1V

Switch On-Resistance



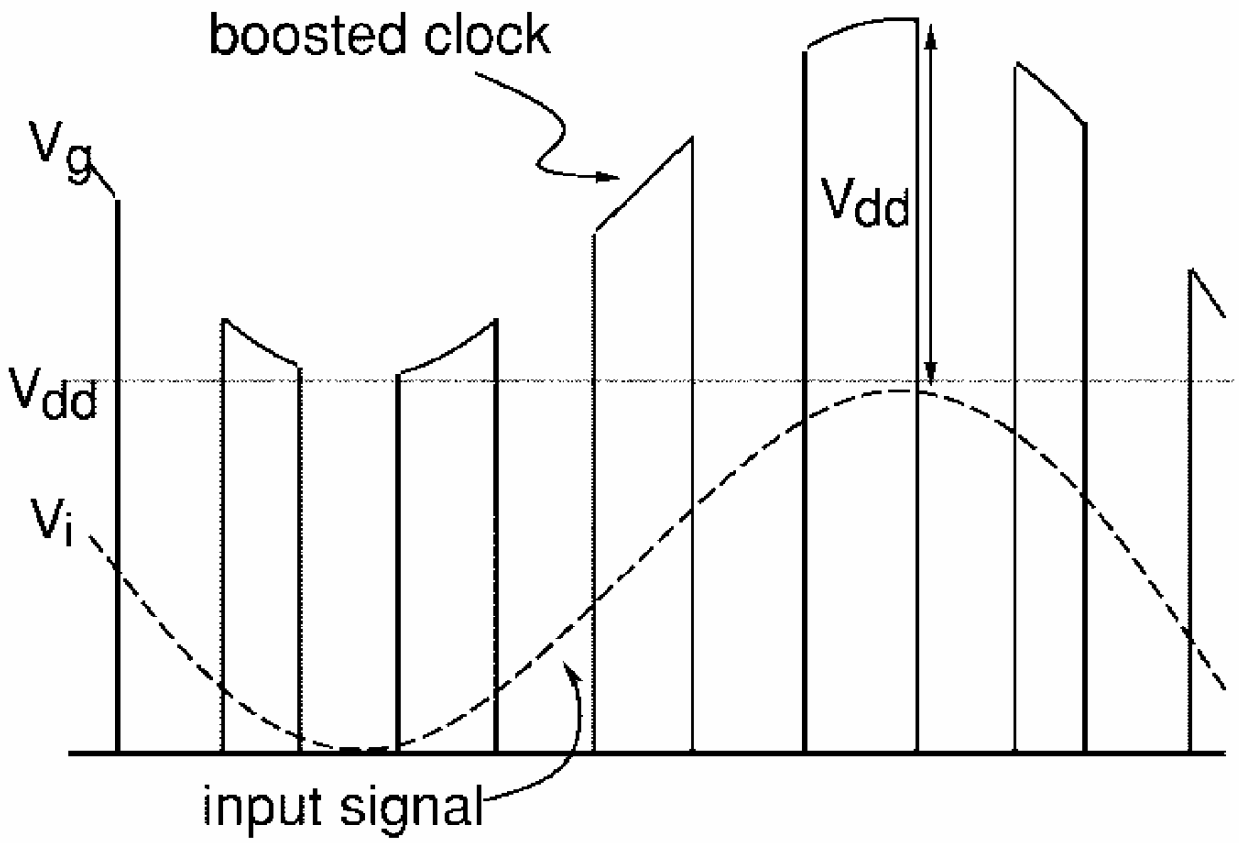
$V_{DD} = 1V$

Constant V_{GS} Sampling

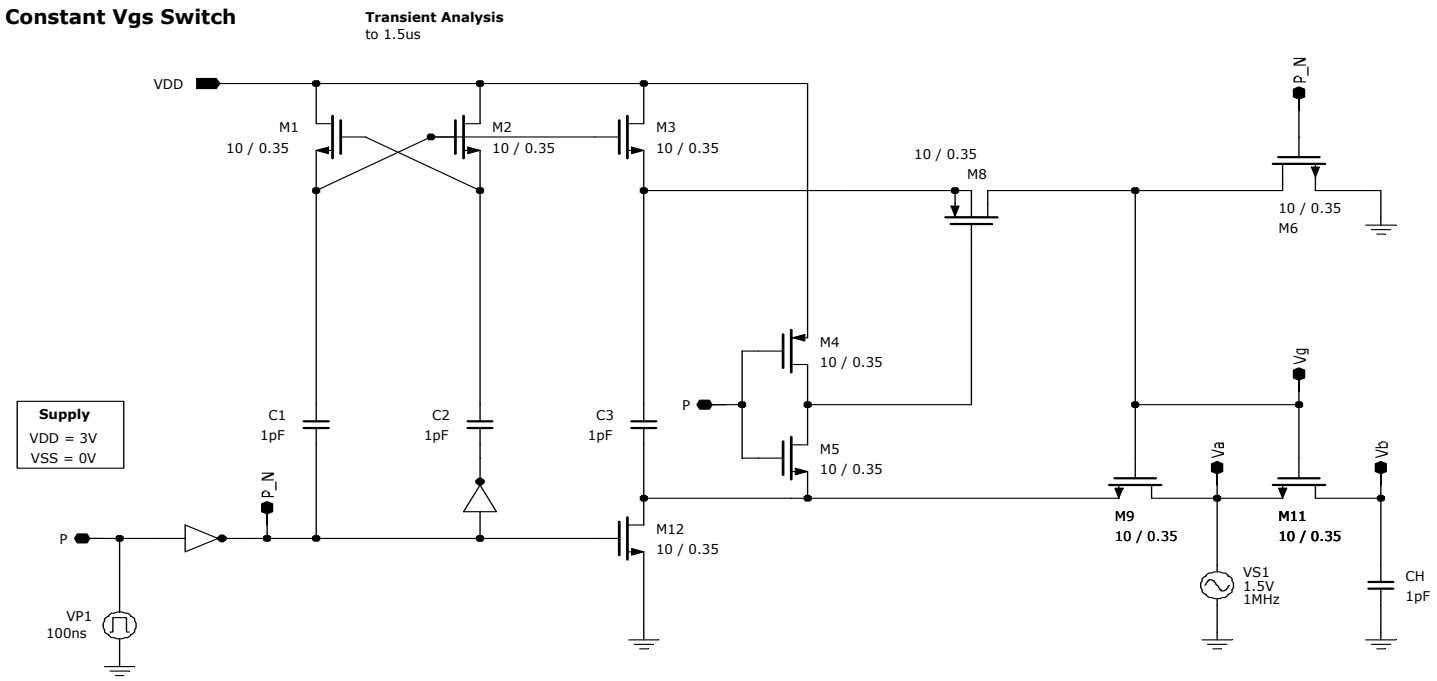


- Switch overdrive voltage is independent of signal
- Error from finite R_{ON} is linear (to first order)

Constant V_{GS} Sampling

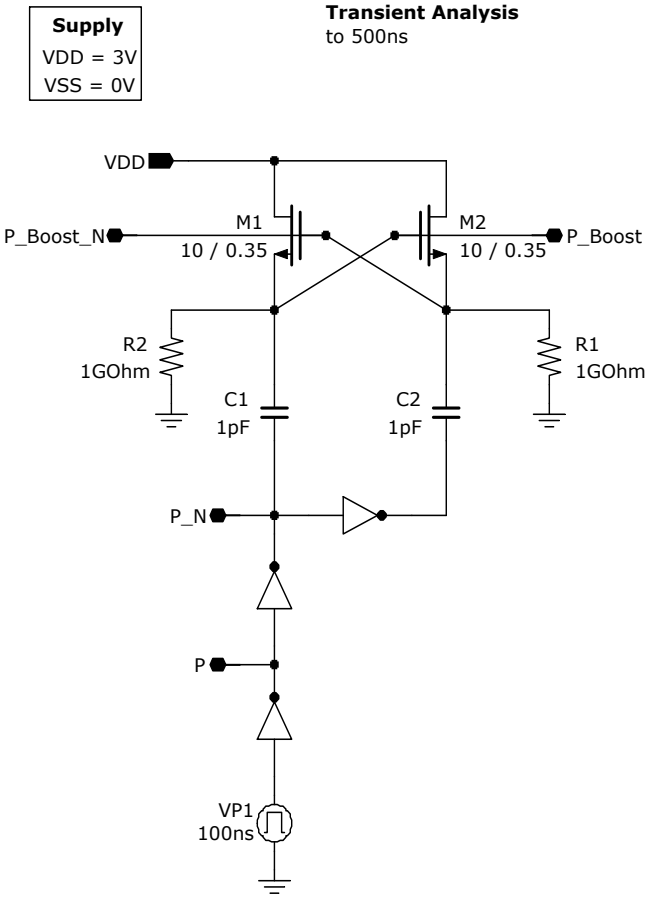


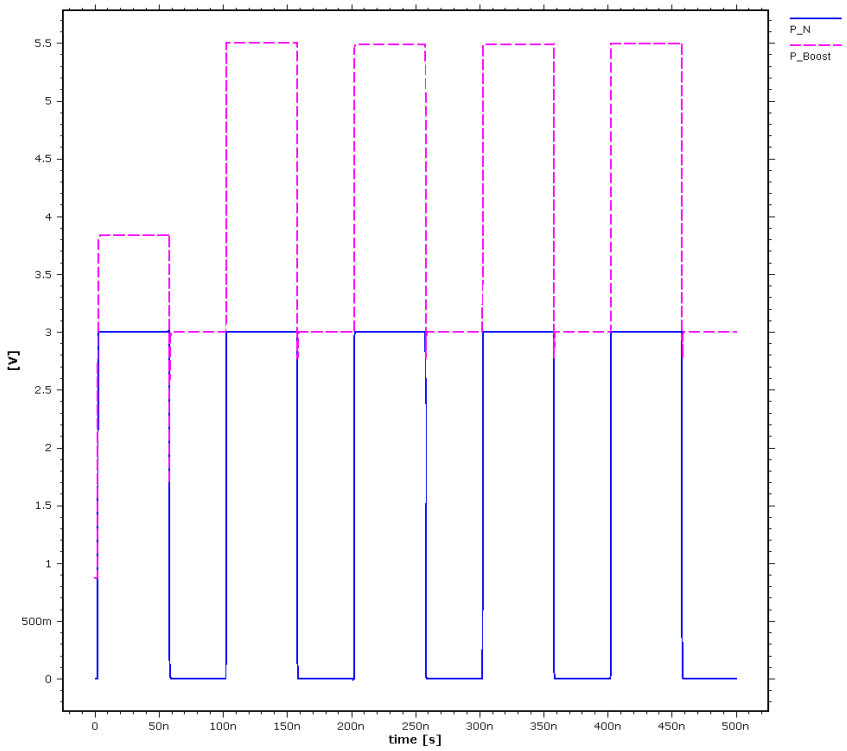
Constant V_{GS} Sampling Circuit



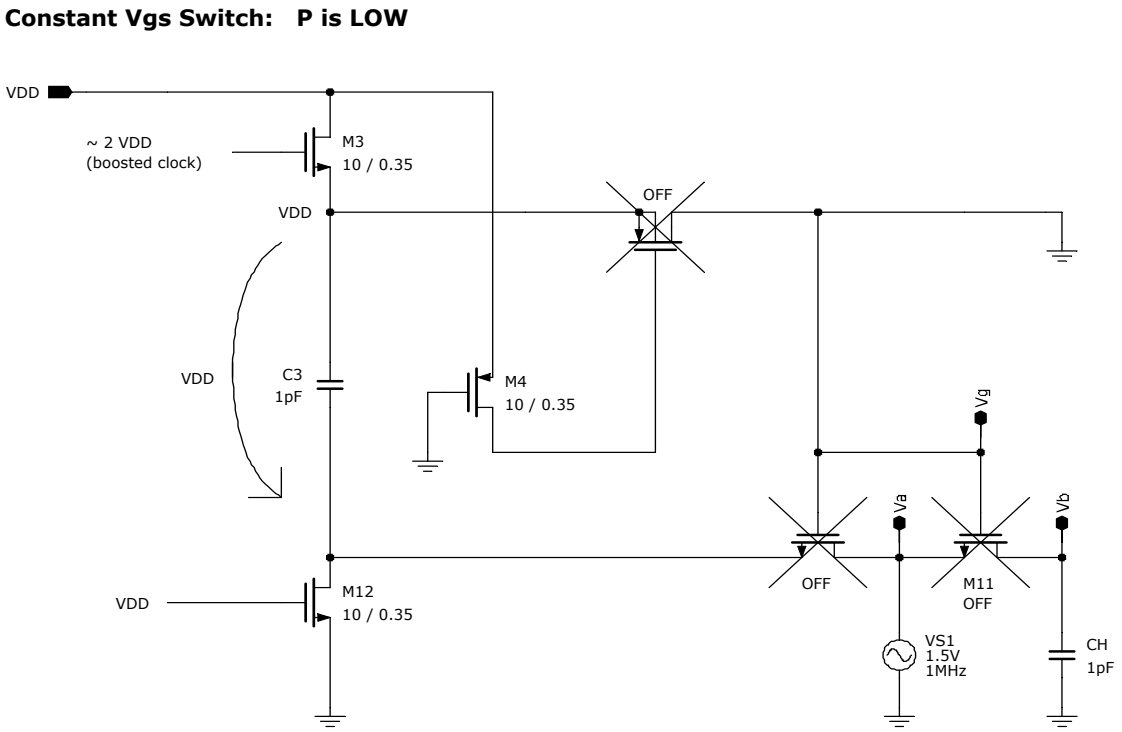
Clock Multiplier

Clock Booster



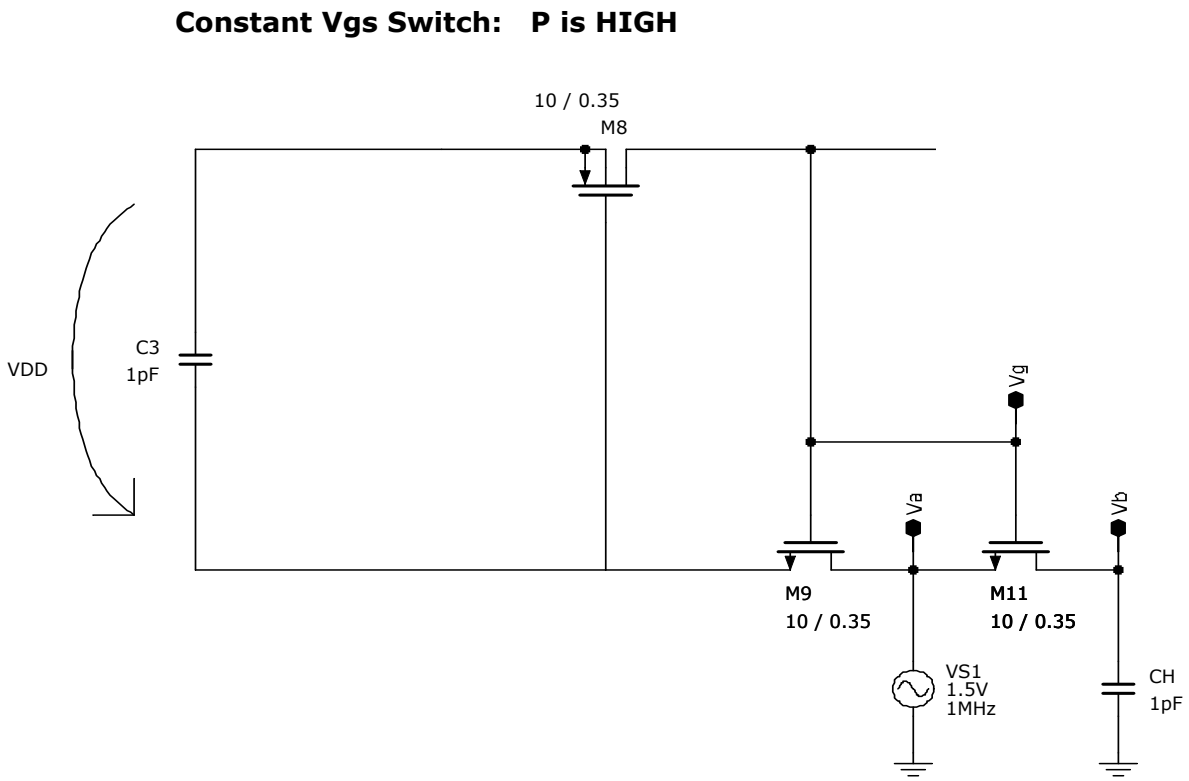


Constant V_{GS} Sampler: Φ LOW



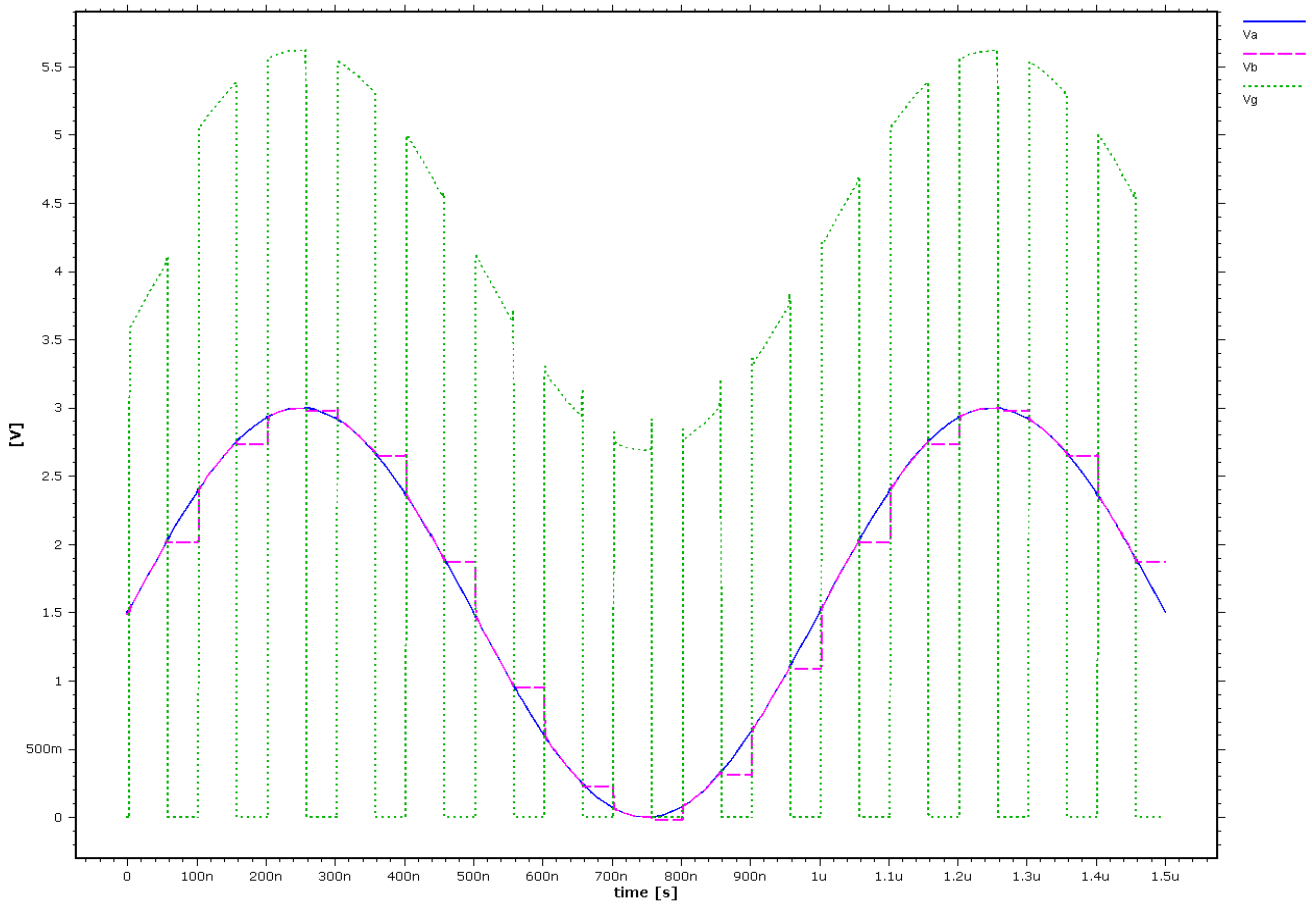
- Sampling switch M11 is OFF
- C3 charged to VDD

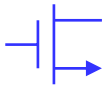
Constant V_{GS} Sampler: Φ HIGH



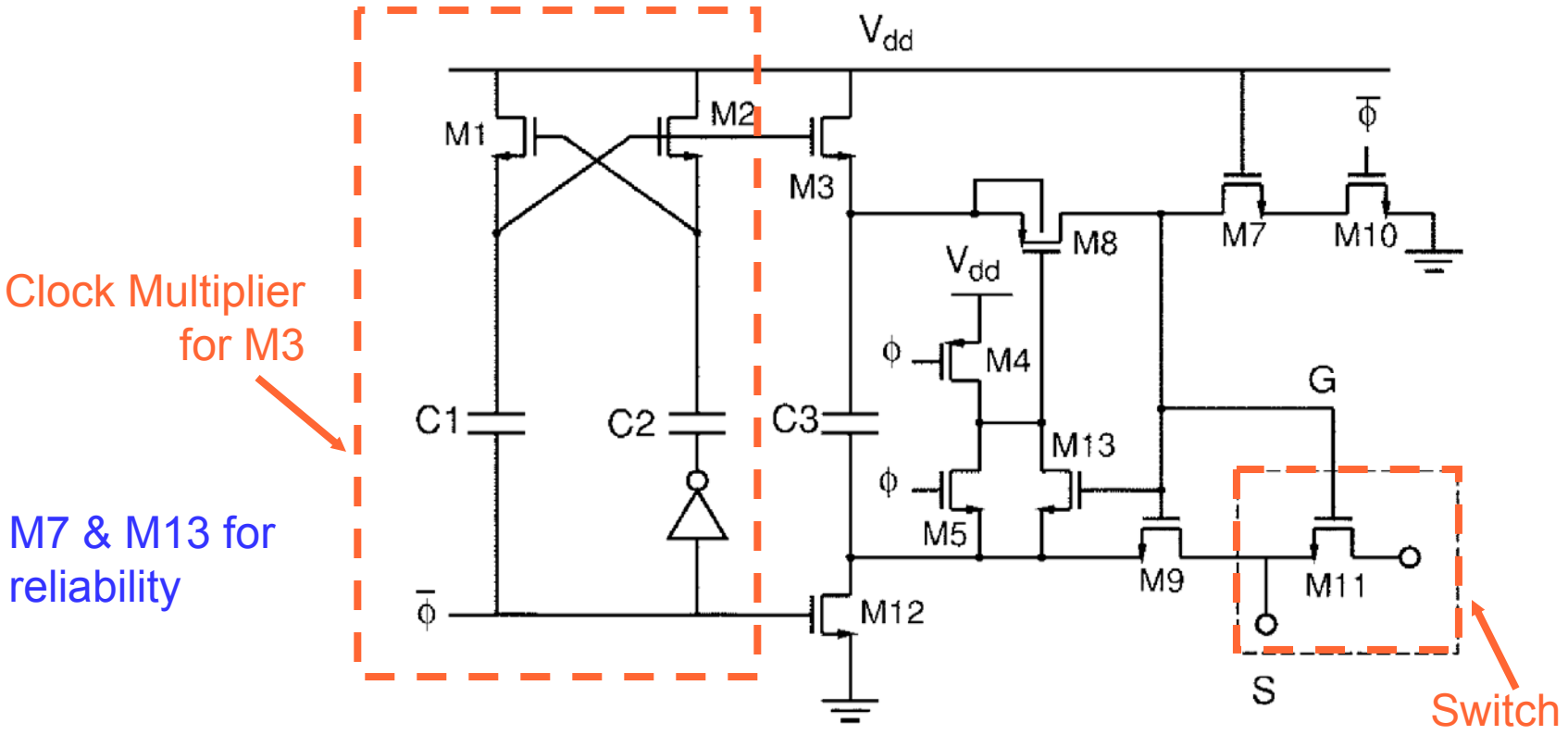
- C3 previously charged to VDD
- M8 & M9 are on: C3 across G-S of M11
- M11 on with constant VGS = VDD

Constant V_{GS} Sampling



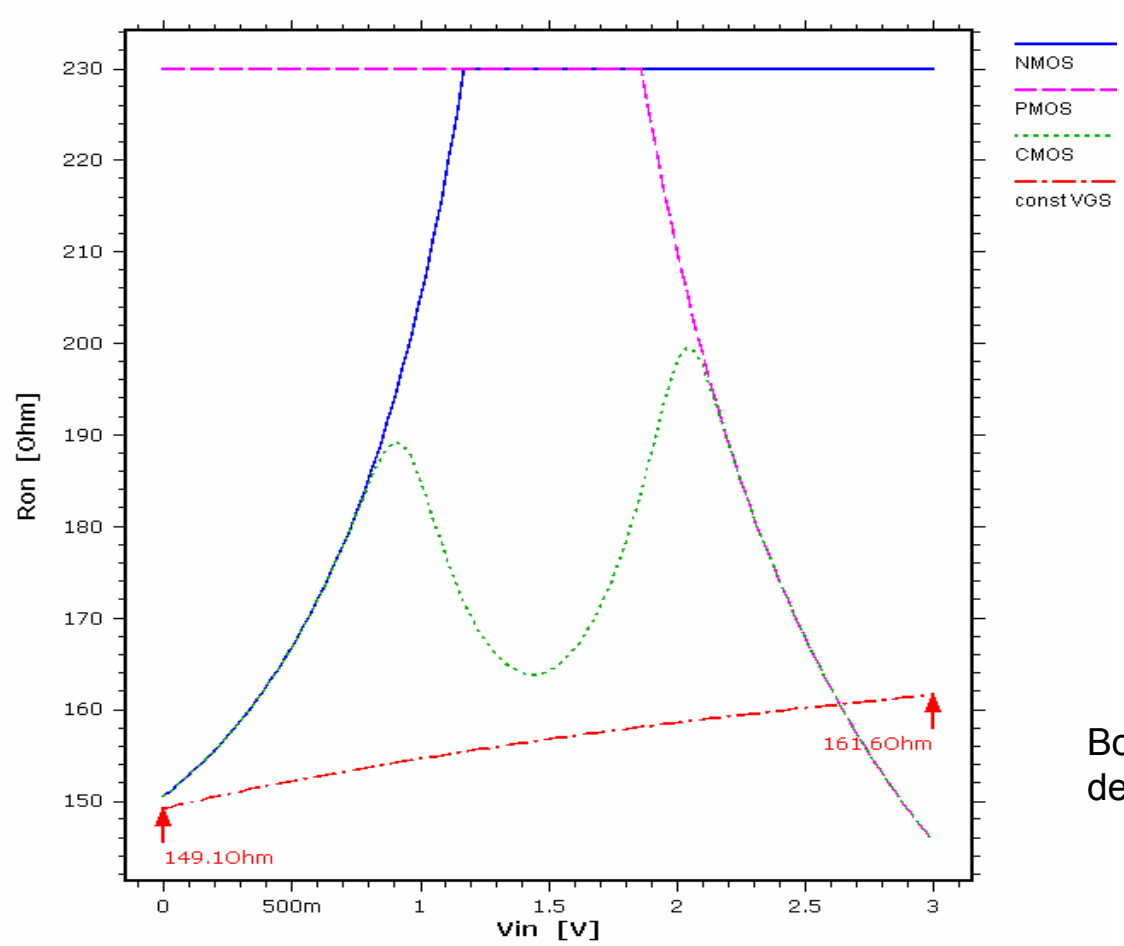


Complete Circuit



Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

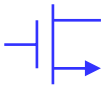
Switch On-Resistance



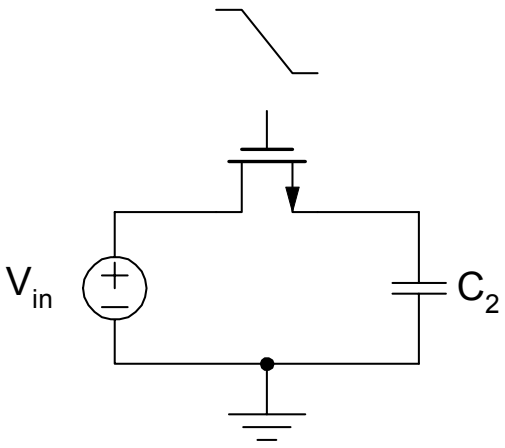
Body-effect causes residual dependence of R_{on} on V_{in}

Charge Injection

- "Extra" charge dumped onto holding capacitor
- Cause:
  - C_{ov} charge sharing
  - Channel charge
- Problems:
  - Offset
  - Distortion (error charge is function of V_{IN})
- Solutions:
  - Dummy switches
  - Bottom-plate sampling



Worst-Case Error



channel charge :

$$Q_{CH} = WLC_{ox}\left(V_{DD} - V_{in} - V_{TH}\right)$$

max pedestal error : $V_{in} = V_{SS}$

$$\Delta V = \frac{Q_{CH}}{C_2} = \frac{WLC_{ox}}{C_2}\left(V_{DD} - V_{SS} - V_{TH}\right)$$

Example :

$$\Delta V = \frac{10 \times 0.35 \times 5}{1000}\left(3 - 0.6\right) = \underline{42\text{mV}}$$

- Error significant in many applications
- Worst case: not all Q_{CH} goes onto C_2
- Signal dependent: Q_{CH}, V_{TH} → $f(V_{in})$
- Solution?

"Small Switch"

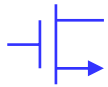
$$\tau = R_o C_2 = \frac{C_2}{\mu C_{ox} \frac{W}{L}(V_{DD} - V_{TH})}$$

$$\Delta V = \frac{Q_{CH}}{C_2} = \frac{WLC_{ox}}{C_2}(V_{DD} - V_{SS} - V_{TH})$$

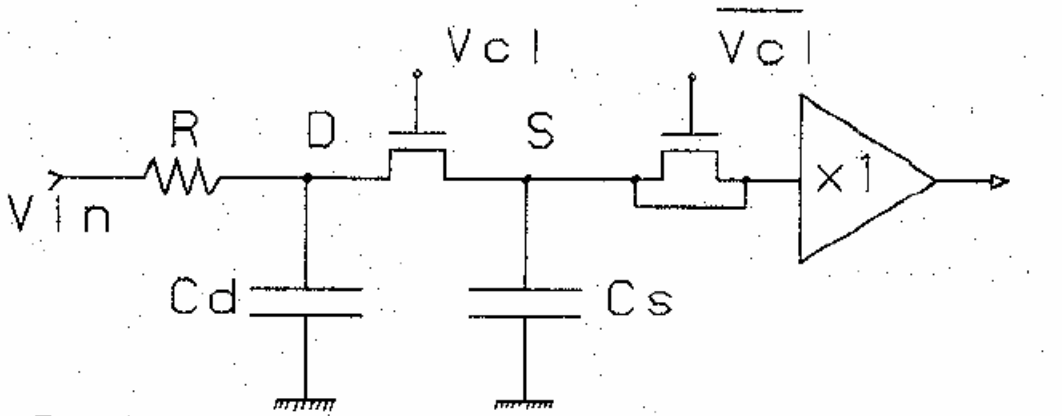
$$FOM = \frac{C_2}{\mu C_{ox} \frac{W}{L}(V_{DD} - V_{SS} - V_{TH})} \times \frac{WLC_{ox}}{C_2}(V_{DD} - V_{SS} - V_{TH})$$

$$= \frac{L^2}{\mu}$$

Reduced ΔV → incase in τ: no optimum



Dummy Switch

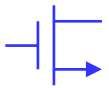


Vin	UNCOMPENSATED SWITCH	COMPENSATED WITH DUMMY	BALANCED SWITCH
0v	-160mV	-45mV	6mV
5v	-105mV	-30mV	1mV
10v	-40mV	-11mV	0.5mV

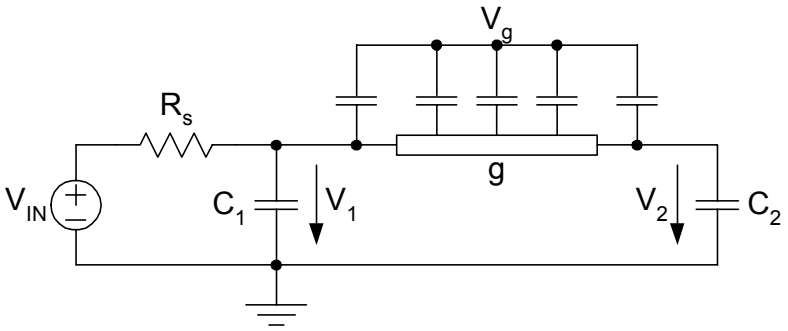
- Dummy switch is half width
- Depends on equal charge split between source and drain
- Is split equal?

Ref: Bienstman et al, JSSC 12/1980, pp. 1051.

Eichenberger et al, JSSC 8/1989, pp. 1143.



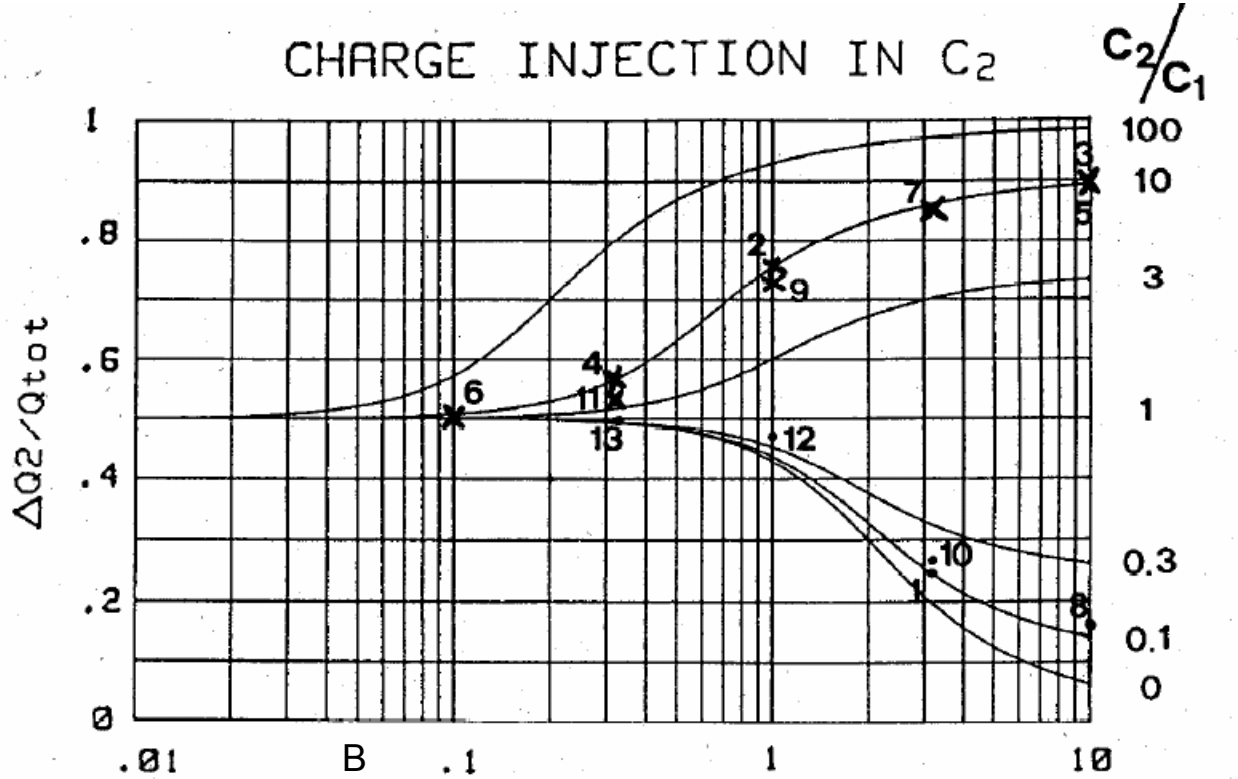
Charge Injection Model



- On-state: MOSFET charge storage
  - Channel: $Q_{CH} \cong WLC_{ox}(V_G - V_{IN} - V_{TH})$
  - Overlap capacitance
- Turn-off:
  - Charge splits between C_1 and C_2
  - Charge injected onto C_2 corrupts signal
  - Error

$$\frac{\Delta Q_2}{C_2 V_{IN}} = ?$$

Charge Injection Analysis



Ref: Wegmann et al, "Charge Injection in Analog MOS Switches," IEEE J. Solid-State Circuits, pp. 1091, Dec. 1987.

Charge Injection Analysis

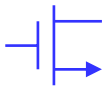
Partition parameter:

$$B = \sqrt{(V_{DD} - V_{SS} - V_{TH}) t_{FALL} \frac{\mu}{L^2} \frac{WLC_{ox}}{C_2}}$$

$$= \sqrt{\underbrace{\frac{V_{DD} - V_{SS} - V_{TH}}{V^*}} \times \underbrace{\frac{WLC_{ox}}{C_2}} \times \underbrace{t_{FALL}\omega_T}}$$

SPICE (BSIM 3v3):

XPART	Source	Drain
0 (default)	60%	40%
0.5	50%	50%
1	0%	100%



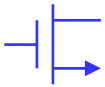
Minimizing Injection Error

1. B >> 1: $t_{FALL} >> 1/\omega_T$ and $C_1 >> C_2$
   - All charge injected onto C_2 flows back onto C_1 during "slow" turnoff
   - Impractical: slow and uselessly large C_1

2. $C_1 = C_2$ and dummy switch (cf. Bienstmann)
   - Useless C_1 (extra area and power)

3. B << 1: requires fast switching, only approximate

4. CMOS Switch
   - Partial cancellation for "some" V_{in} (when both XTR are on)
   - Depends on (poor) matching between NMOS and PMOS
   - Beware of PM→AM conversion (jitter):
     - Amount of injected charge depends on which switch turns of first
     - Better to depend on only on type switch turning off



Rejecting Injection Error

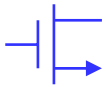
$$\Delta V = V_{OS} + f(V_{in})$$

V_{OS} → differential circuit

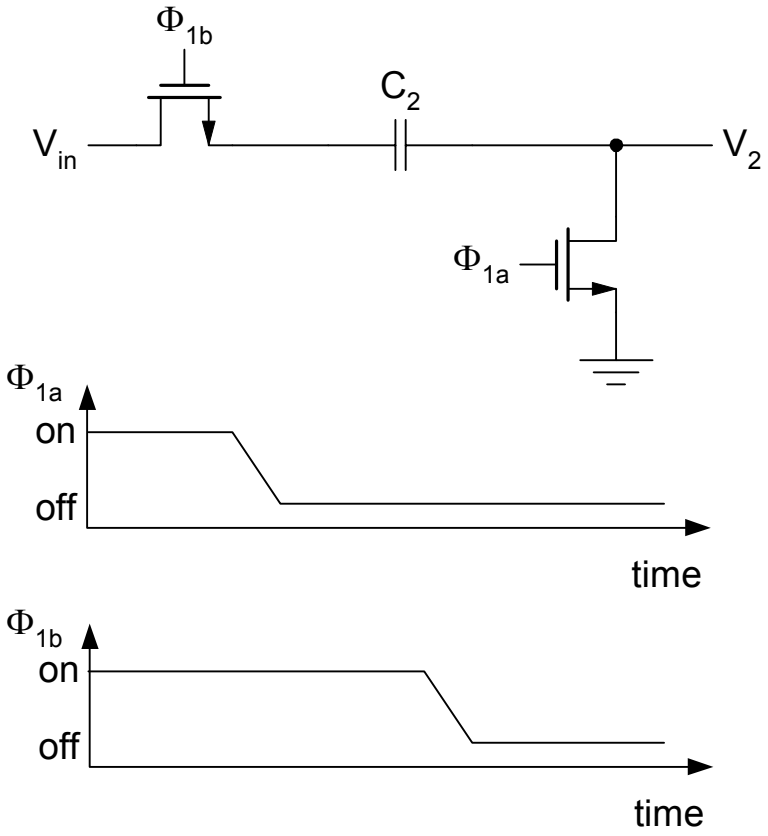
$f(V_{in})$ → bottom plate = const. V_{in} sampling

Refs: R. C. Yen and P. R. Gray, "An MOS switched capacitor sampling differential instrumentation amplifier," *IEEE International Solid-State Circuits Conference,* vol. XXV, pp. 82 - 83, February 1982.

K. Lee and R. G. Meyer, "Low-distortion switched-capacitor filter design techniques," *IEEE Journal of Solid-State Circuits,* vol. 20, pp. 1103 - 1113, December 1985.

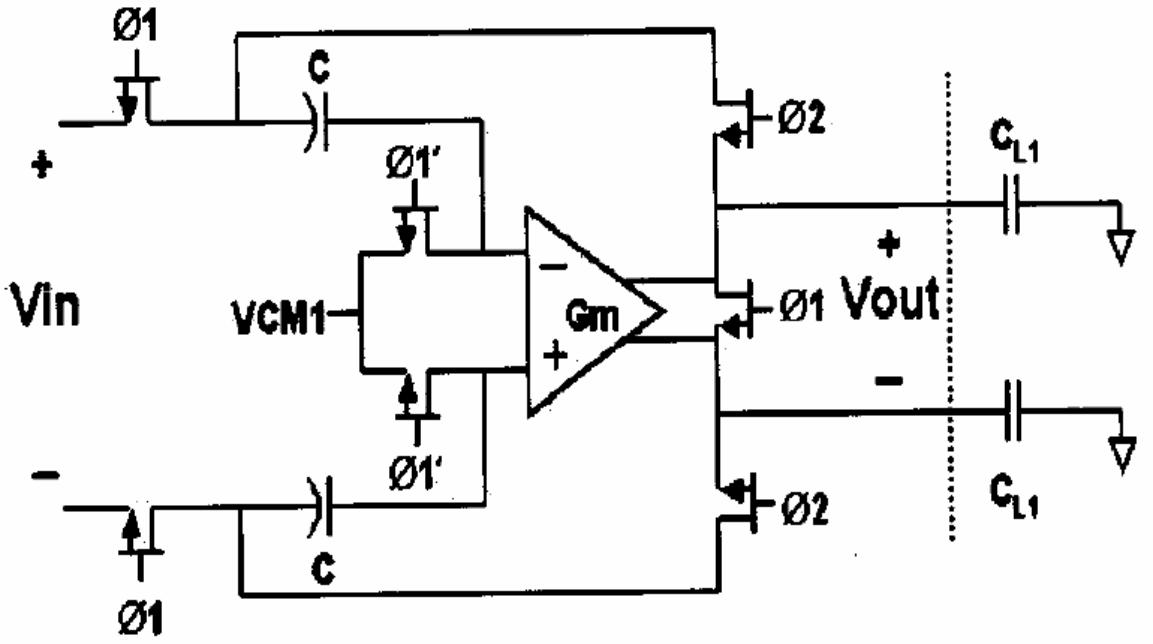


Bottom-Plate Sampling



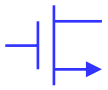
- Switch Φ_{1a} opens first
  - Injected charge is constant, i.e. not f(Vin)
  - Removed by differential implementation
- Switch Φ_{1b} opens later
  - C_2 disconnected → no charge injected

MOS T&H

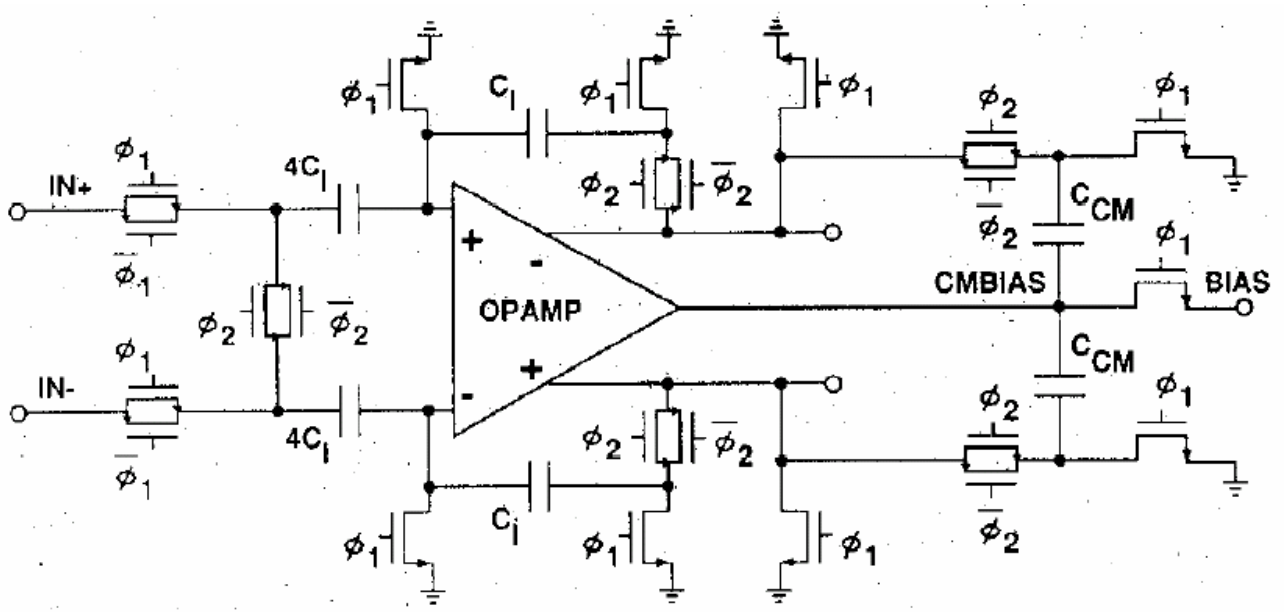


- G = 1
- $F_{max} = 1$
- ΔV_{icm} at input of G_m

Ref: W. Yang, D. Kelly, I. Mehr, M. T. Sayuk, and L. Singer, "A 3-V 340mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input," *IEEE Journal of Solid-State Circuits,* vol. 36, pp. 1931 - 1936, December 2001.



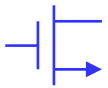
SC Gain Stage



- $G = C_s / C_f$
- $F_{max} = 1 / (1+G)$
  $= 0.5$ for $G=1$
- ΔV_{icm} remains on C_s

Refs: R. C. Yen and P. R. Gray, "An MOS switched capacitor sampling differential instrumentation amplifier," *IEEE International Solid-State Circuits Conference,* vol. XXV, pp. 82 - 83, February 1982.

S. H. Lewis and P. R. Gray, "A pipelined 5-Msample/s 9-bit analog-to-digital converter," *IEEE Journal of Solid-State Circuits,* vol. 22, pp. 954 - 961, December 1987.

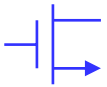


Jitter

- All of the preceding analyses assume that sampling impulses are spaced evenly in time
- Actual clocks show some distribution around the nominal value T
- The variability in T is called jitter
- Typical clocks have >100ps+ jitter
- Excellent (and expensive) clocks have <1ps jitter

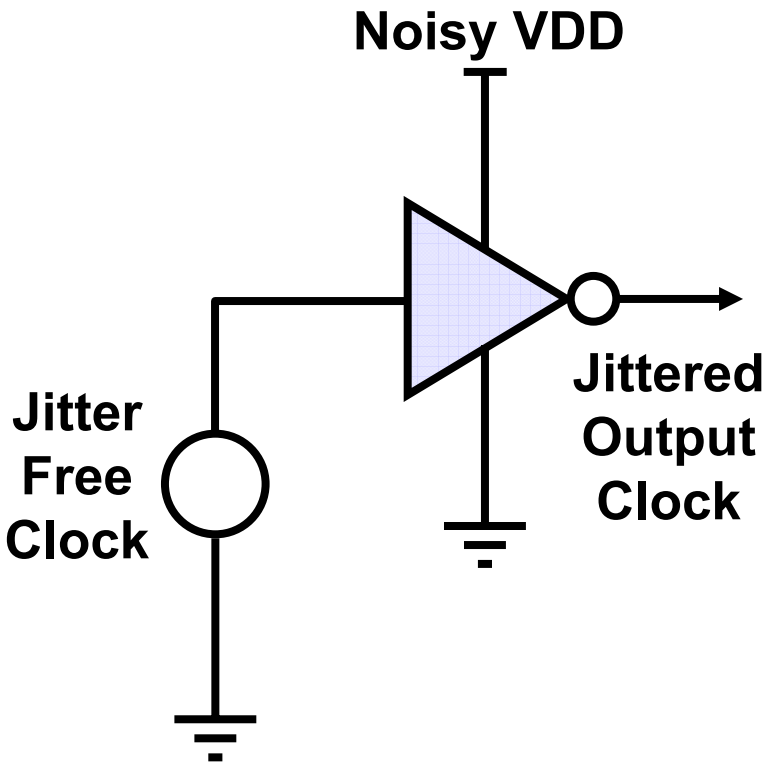
Refs: T. H. Lee, K. S. Donnelly, J. T. C. Ho, J. Zerbe, M. G. Johnson, and T. Ishikawa, "A 2.5 V CMOS delay-locked loop for 18 Mbit, 500 megabyte/s DRAM," *IEEE Journal of Solid-State Circuits,* vol. 29, pp. 1491 - 1496, December 1994.

R. Farjad-Rad, W. Dally, H. Ng, R. Senthinathan, M. E. Lee, R. Rathi, and J. Poulton, "A low-power multiplying DLL for low-jitter multigigahertz clock generation in highly integrated digital chips," *IEEE Journal of Solid-State Circuits,* vol. 37, pp. 1804 - 1812, December 2002.



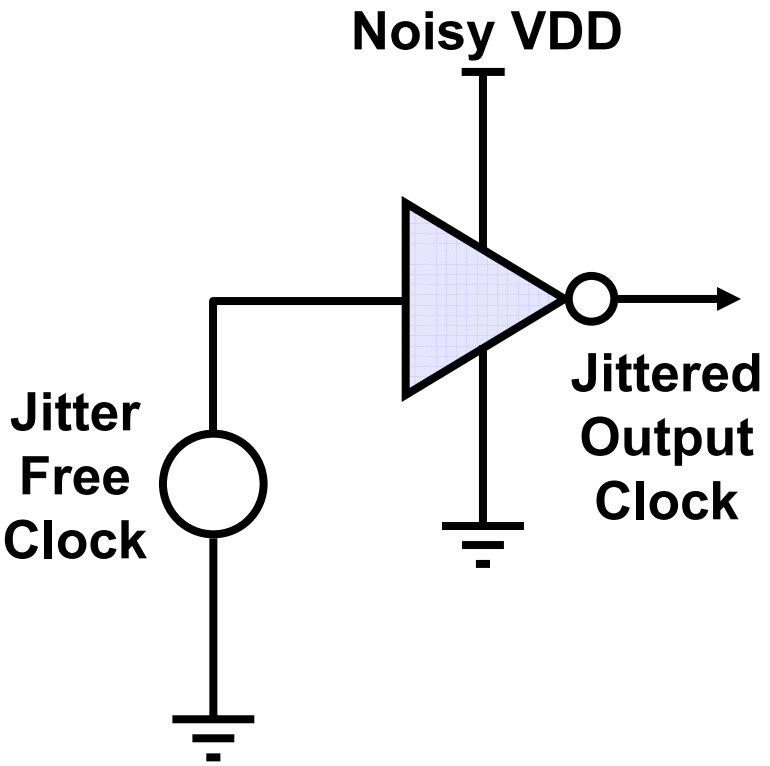
Jitter

- The dominant cause of clock jitter in most chips is power supply noise produced by unrelated activity in other parts of the chip
- The inverter symbol represents a chain of gates in the sampling clock path



Jitter

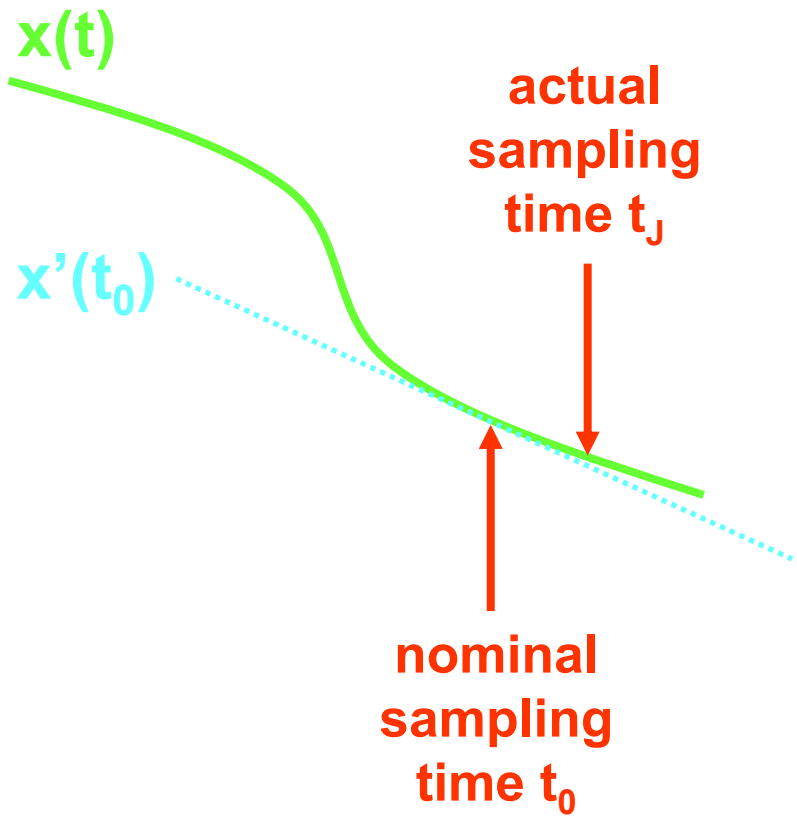
- Let's assume the inverter delay is 100psec, and that the delay varies by 20% per volt change in V_{DD} (20psec/V)
- 200mV of power supply noise becomes 4psec of clock jitter



Jitter

- Sampling jitter adds an error voltage proportional to the product of (t_J-t_0) and the derivative of the input signal at the sampling instant

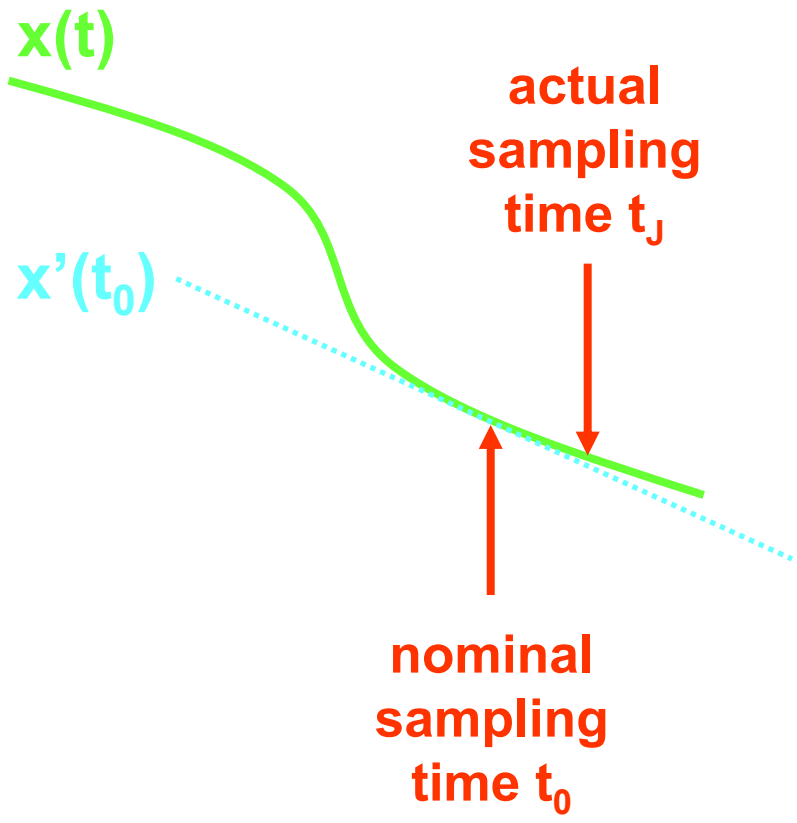
- Jitter doesn't matter when sampling dc signals



Jitter

Error voltage (1st order):

$$e = (t_j - t_o)\frac{dx(t_o)}{dt}$$



Jitter Estimate

Sinusoidal input

Amplitude : A

Frequency : f_x

Jitter : Δt

$$x(t) = A\sin(2\pi f_x t)$$
$$x'(t) = 2\pi f_x A\cos(2\pi f_x t)$$
$$|x'(t)| \le 2\pi f_x A$$
$$|e(t)| \le |x'(t)|\Delta t$$

Worst case

$$A = A_{FS}$$
$$f_x = f_s/2$$
$$|e(t)| << \frac{\Delta}{2} \cong \frac{A_{FS}}{2^{B+1}}$$
$$\Delta t << \frac{1}{2^B \pi f_s}$$

B	f_s	Δt << than
16	10 MHz	0.5 ps
12	100 MHz	0.8 ps
8	1000 MHz	1.2 ps