EECS 240
Analog Integrated Circuits

Topic 17: Device Matching

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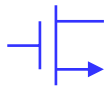
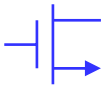


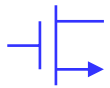
Device Matching Mechanisms

- Spatial effects
  - Wafer-to-wafer
  - Long range
    - Gradients
  - Short range
    - Statistics
- Circuit effects
  - Differential structures
    - Differential pair
    - Current mirror
  - Bias
- Layout effects



Mismatch Model

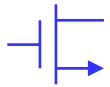
- What is modeled?
  - Short-range, random processes, e.g.
    - Dopant fluctuations
    - Mobility fluctuations
    - Oxide trap variations
- What is NOT modeled?
  - Batch-to-batch or wafer-to-wafer variations
  - Long-range effects such as gradients
  - Electrical, lithographic, or timing offsets



References

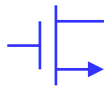
- M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits,* vol. 24, pp. 1433 - 1439, October 1989.
  - Mismatch model
  - Statistical data for 2.5μm CMOS

- Jeroen A. Croon, Maarten Rosmeulen, Stefaan Decoutere, Willy Sansen, Herman E. Maes; *An easy-to-use mismatch model for the MOS transistor*, IEEE Journal of Solid-State Circuits, vol. 37, pp. 1056 - 1064, August 2002.
  - 0.18μm CMOS data
  - Qualitative analysis of short-channel effects on matching

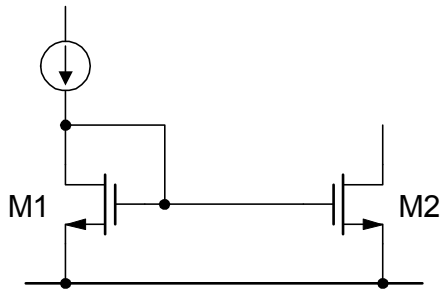


Mismatch Statistics

- Composed of many single events
  E.g. dopant atoms
- Individual effects are small
  → linear superposition applies
- Correlation distance << device dimensions
- → Mismatch has Gaussian distribution, zero mean



MOSFET Mismatch Parameter



Experiment:

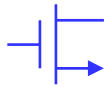
$$\frac{\Delta I_D}{I_D} = 1\%$$

- Experimental result applies to one particular configuration
- What about:
  - Device size
    - W
    - L
    - Area
  - Bias
    - V_{GS}
  - Physical proximity
  - …
- Need parameterized model

Geometry Effects

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D_x^2$$

$\sigma^2(\Delta P)$:	standard deviation of P
WL:	active gate area
D_x:	distance between device centers
A_P:	measured area parameter
S_P:	measured distance parameter,
:	$\cong 0$ for common-centroid layout



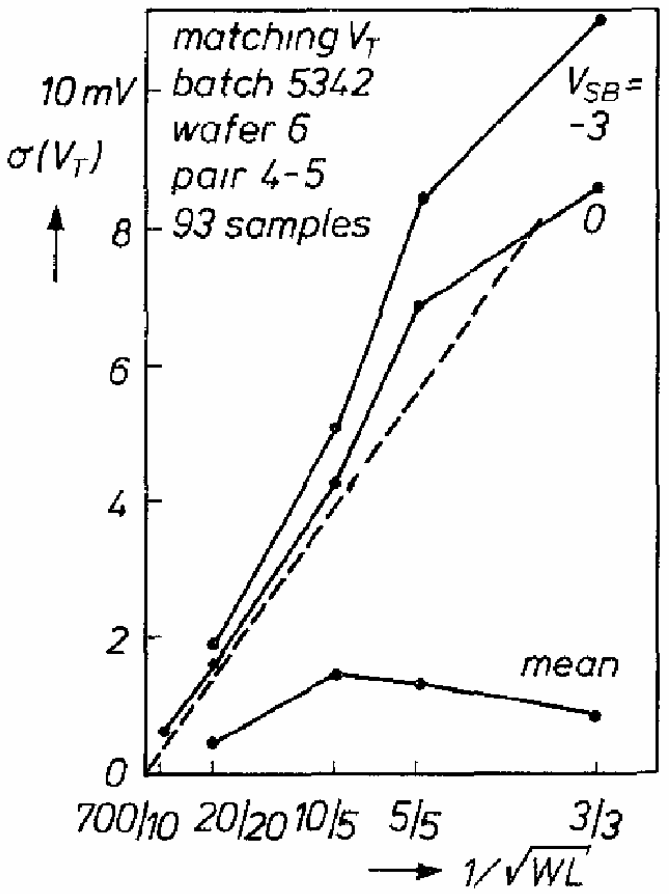
Example: V_{TH}

$$\sigma^2\left(\Delta V_{TH0}\right) = \frac{A^2_{P,V_{TH0}}}{WL} + S^2_{P,V_{TH0}} D^2_x$$

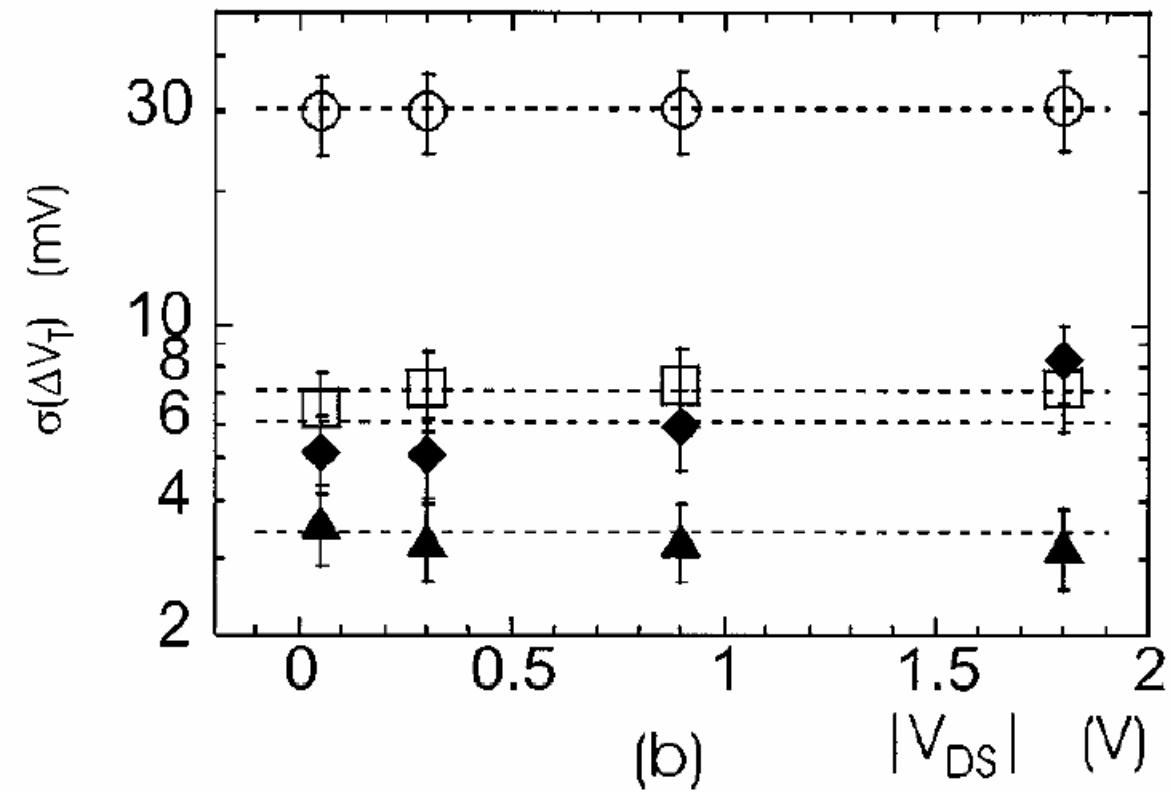
$A_{P,NMOS} \cong 30\,\text{mV}\,\mu\text{m}$

$A_{P,PMOS} \cong 35\,\text{mV}\,\mu\text{m}$

(2.5µm CMOS process)

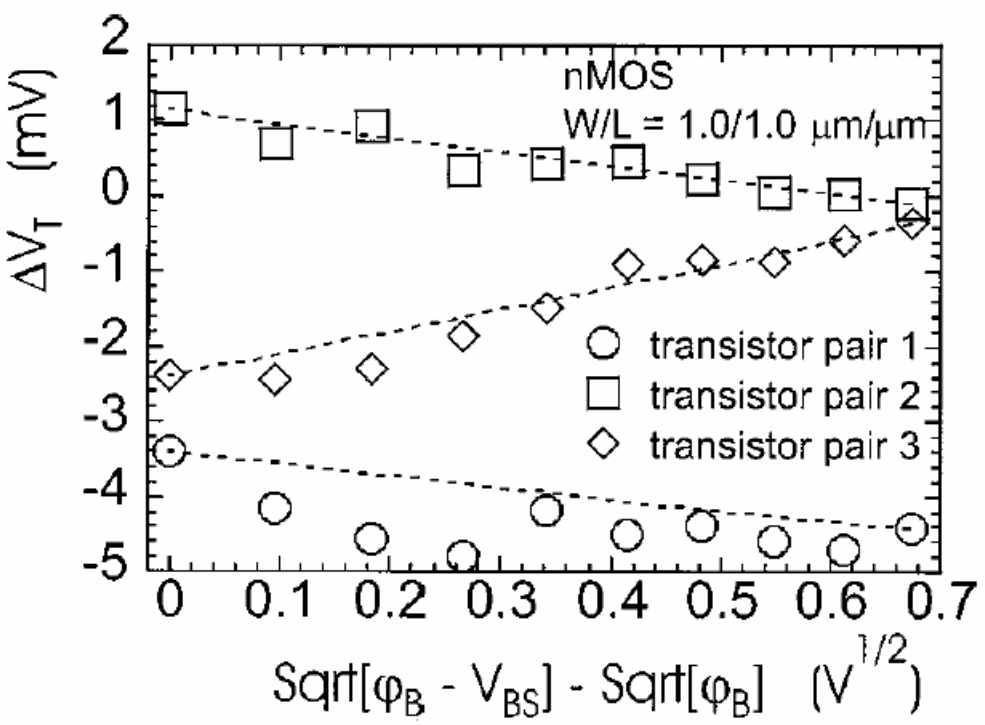


Drain Bias, V_{DS}



ΔV_{TH0} virtually independent of V_{DS}

Back-Gate Bias, V_{SB}



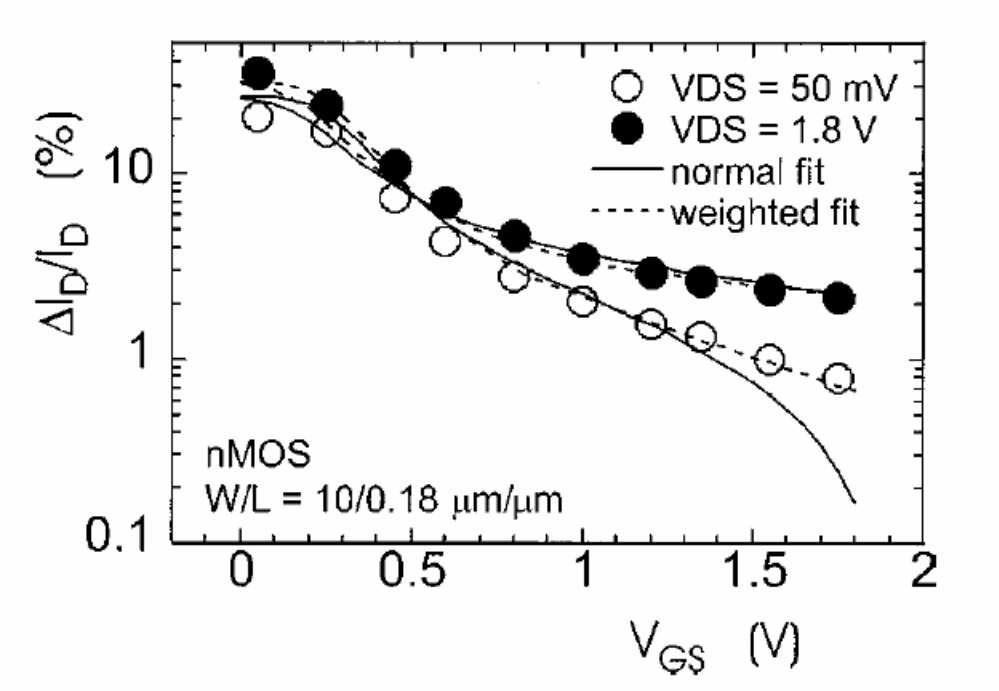
- Pair 3 exhibits significant V_{SB} dependence
- Why?
  - Non-uniform doping profile (V_{TH} adjust)

$$V_{TH} = V_{TH0} + \gamma\left[\sqrt{\Phi_B - V_{BS}} - \sqrt{\Phi_B}\right]$$

$$\sigma^2(V_{TH}) = \ldots$$

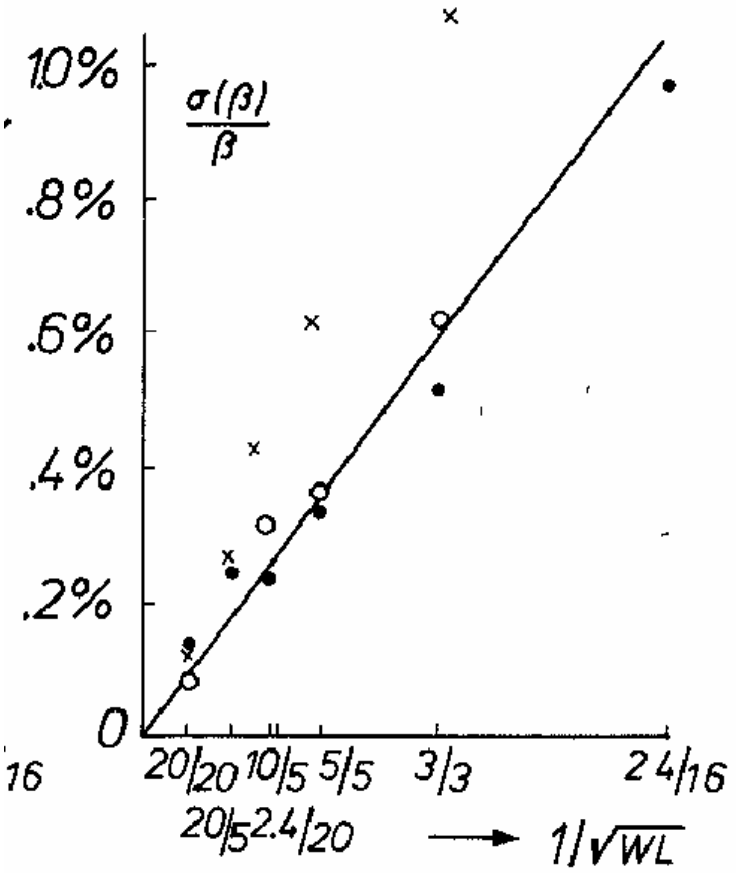
$$\sigma^2(\gamma) = \ldots$$

Current Matching, $\Delta I_D/I_D$



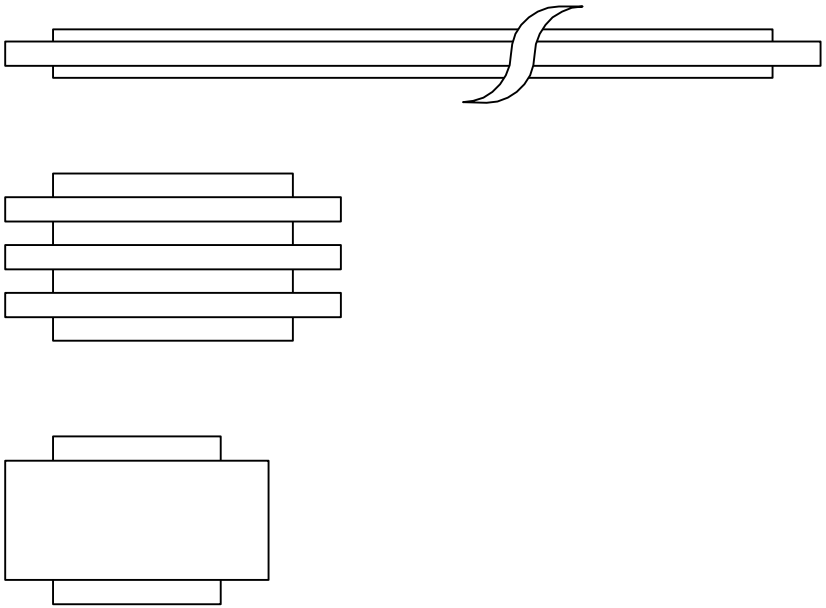
Strong bias dependence (we knew that already)

Current Factor



$$\beta = \mu C_{ox} \frac{W}{L}$$

Edge Effects



- Relative Matching?
- Model?

Edge Model

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{\sigma^2(W)}{W^2} + \frac{\sigma^2(L)}{L^2} + \frac{\sigma^2(C_{ox})}{C_{ox}^2} + \frac{\sigma^2(\mu_n)}{\mu_n^2}$$

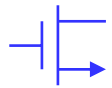
for

$$\sigma^2(W) \propto 1/W \quad \text{and} \quad \sigma^2(L) \propto 1/L$$ ← WRONG

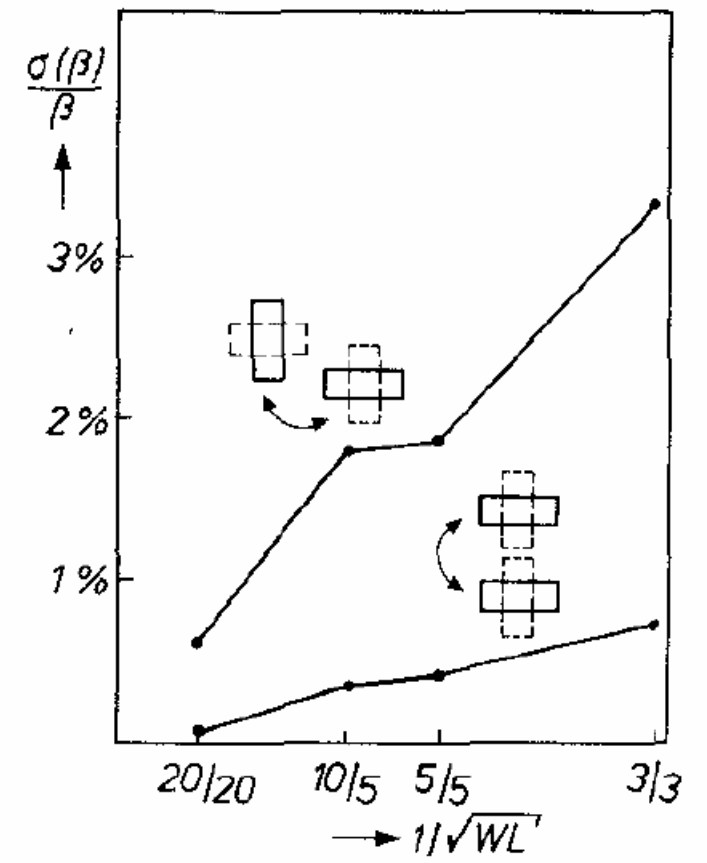
this simplifies to

$$\sigma^2(W) \propto 1/L \quad \text{and} \quad \sigma^2(L) \propto 1/W$$

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_L^2}{WL^2} + \frac{A_W^2}{W^2L} + \frac{A_{C_{ox}}^2}{WL} + \frac{A_\mu^2}{WL} + S_\beta^2 D^2$$

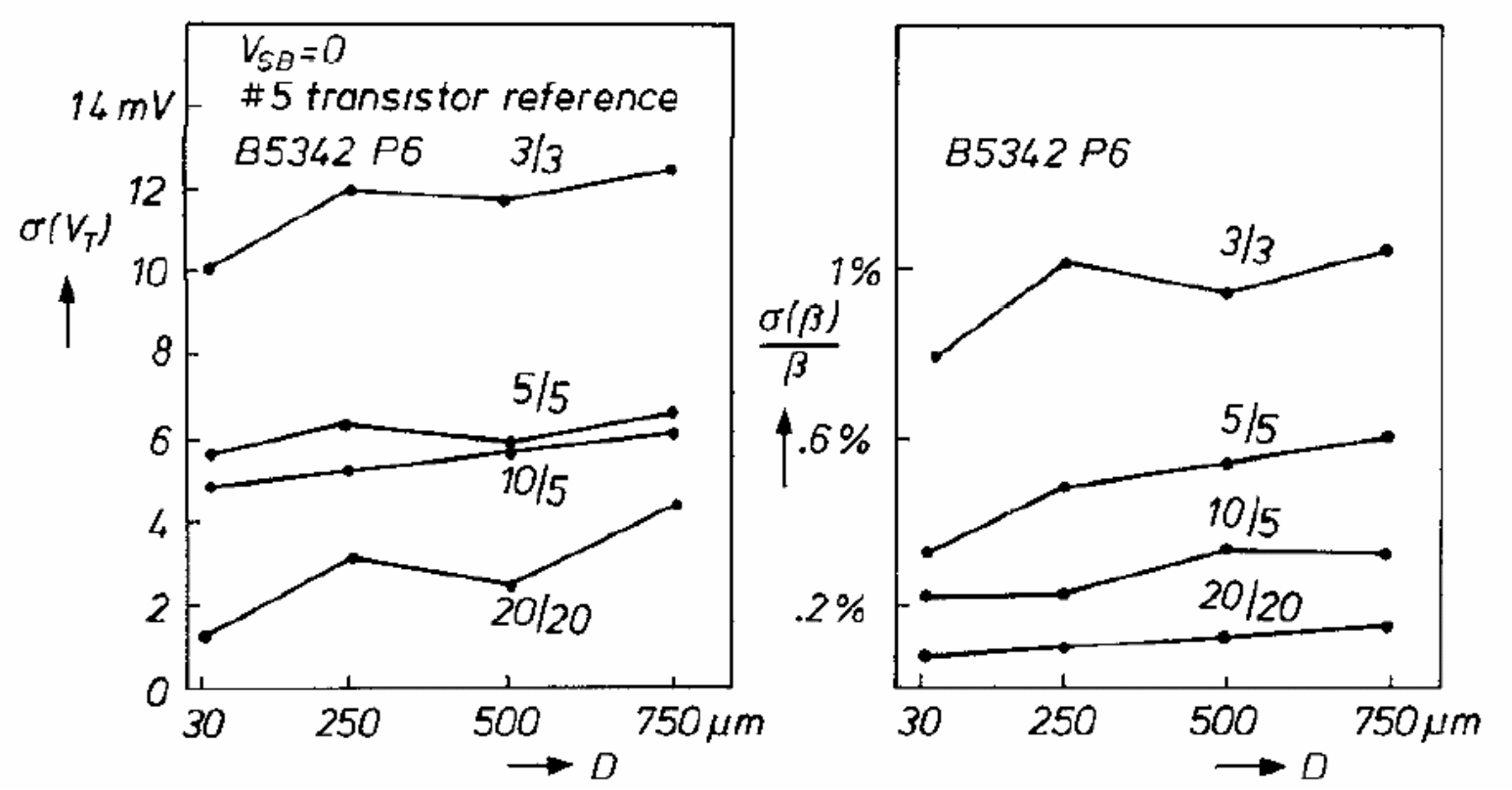


Orientation Effect



- Si and transistors are not (perfectly) isotropic
- → keep direction of current flow same!

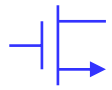
Distance Effect



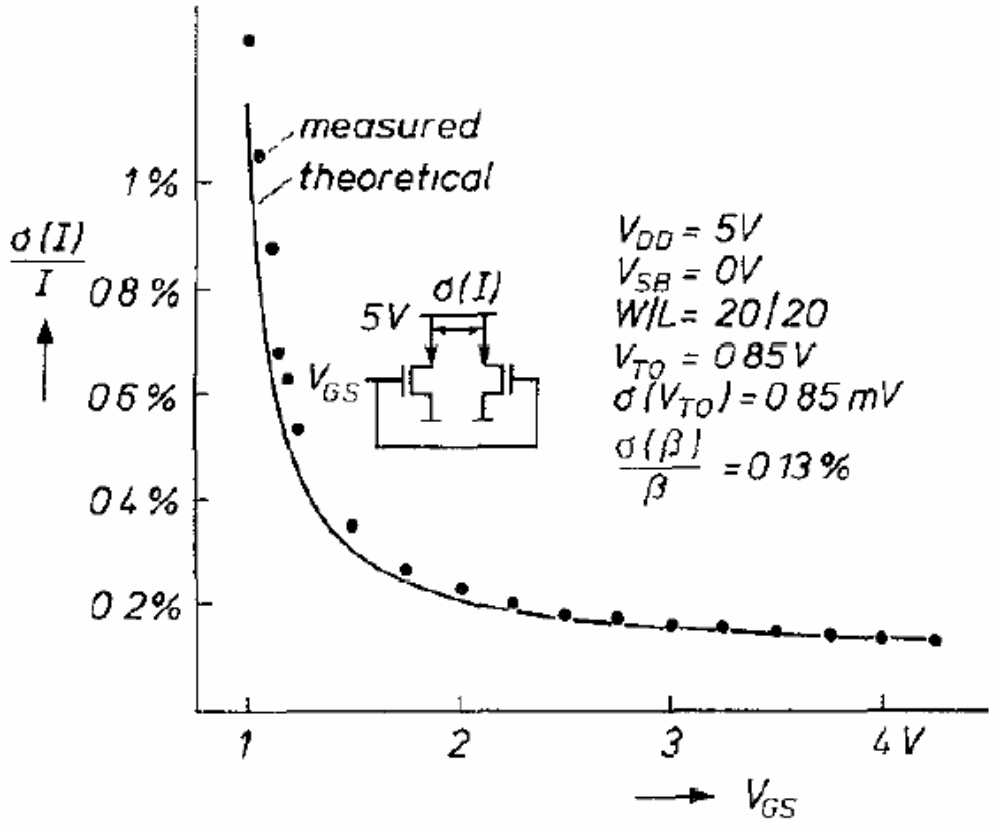
Model Summary

MATCHING DATA FOR NMOS AND PMOS TRANSISTOR PAIRS IN A 50-nm GATE OXIDE, 2.5-μm n-WELL PROCESS

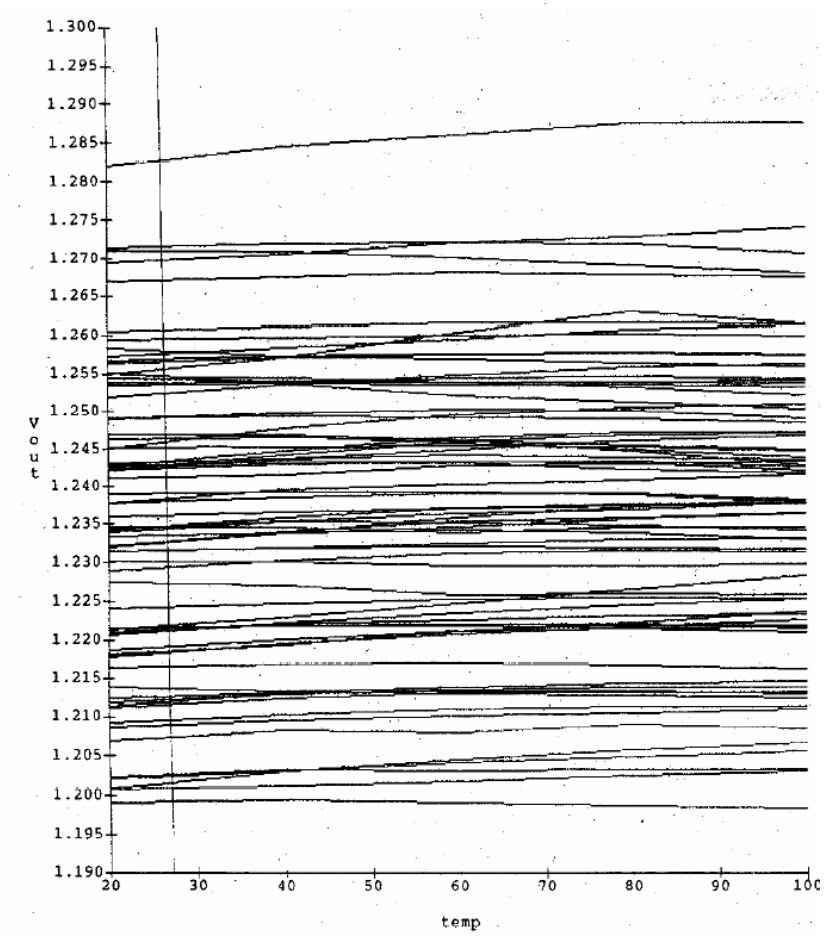
parameter	n-channel s.d.	p-channel s.d.	unit
A_{VT0}	30	35	mVμm
A_β	2.3	3.2	%μm
A_K	16×10^{-3}	12×10^{-3}	$V^{0.5}\mu$m
S_{VT0}	4	4	$\mu V/\mu$m
S_β	2	2	$10^{-6}/\mu$m
S_K	4	4	$10^{-6}V^{0.5}/\mu$m



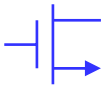
Example: Current Mirror



Example: Bandgap Reference



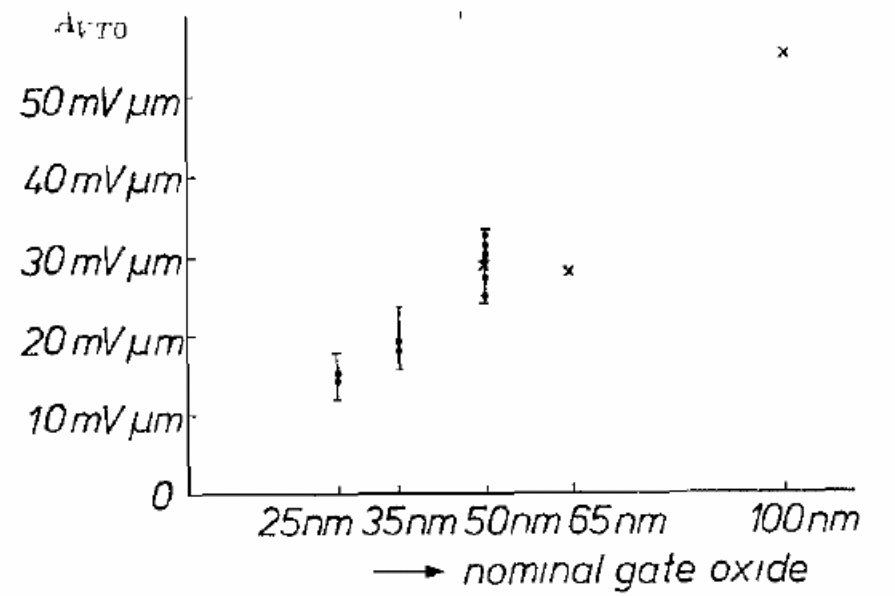
- $\sigma_{VBG} = 25$ mV
- Dominated by amplifier offset
- Area – offset tradeoff



Process Dependence

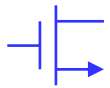
Example: ΔV_{TH} vs. t_{ox}

- V_{TH} matching appears strongly correlated with t_{ox}
- Reason?
  - t_{ox} is not only difference
  - Doping concentration?

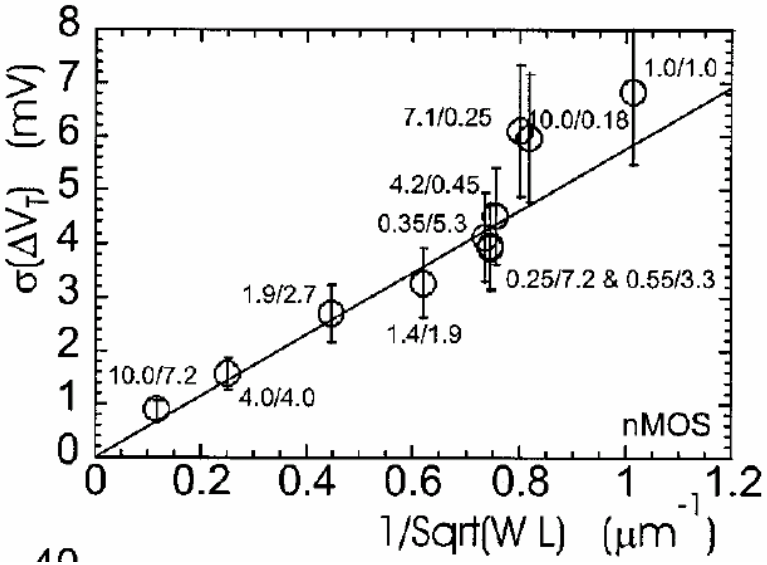


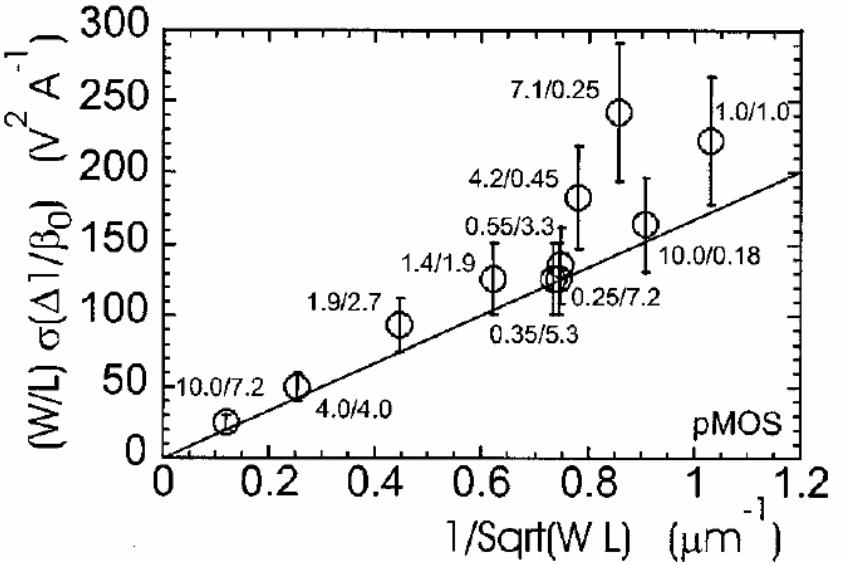
0.18 μm CMOS

	A_0	A_L	A_W
	nMOS		
$\sigma^2_{\Delta V_T}$	33.3e-6 ± 6.4e-6	0	0
$\sigma^2_{\Delta(1/\beta_0)}$	6.1e3 ± 2.1e3	0	-0.91e3 ± 0.66e3
$\sigma^2_{\Delta(1/\zeta_{sr})}$	0.91e3 ± 0.27e3	0	-0.148e3 ± 0.082e3
$\sigma^2_{\Delta(1/\zeta_{sat})}$	0.53e3 ± 0.20e3	0	0
$\rho_{\Delta V_T,\Delta(1/\beta_0)}$	0	0	0
$\rho_{\Delta V_T,\Delta(1/\zeta_{sr})}$	0	0	0
$\rho_{\Delta V_T,\Delta(1/\zeta_{sat})}$	-0.51 ± 0.22	0.048 ± 0.042	0
$\rho_{\Delta(1/\beta_0),\Delta(1/\zeta_{sr})}$	-0.95 ± 0.11	0.052 ± 0.025	0
$\rho_{\Delta(1/\beta_0),\Delta(1/\zeta_{sat})}$	0	0	0
$\rho_{\Delta(1/\zeta_{sr}),\Delta(1/\zeta_{sat})}$	0	0	0
	pMOS		
$\sigma^2_{\Delta V_T}$	15.7e-6 ± 3.2e-6	0	0
$\sigma^2_{\Delta(1/\beta_0)}$	28.3e3 ± 9.6e3	0	0
$\sigma^2_{\Delta(1/\zeta_{sr})}$	7.5e3 ± 2.3e3	0	-1.18e3 ± 0.71e3
$\sigma^2_{\Delta(1/\zeta_{sat})}$	5.2e3 ± 1.9e3	0	0
$\rho_{\Delta V_T,\Delta(1/\beta_0)}$	-0.26 ± 0.15	0	0
$\rho_{\Delta V_T,\Delta(1/\zeta_{sr})}$	0	-0.049 ± 0.034	0
$\rho_{\Delta V_T,\Delta(1/\zeta_{sat})}$	0	0.23 ± 0.13	0
$\rho_{\Delta(1/\beta_0),\Delta(1/\zeta_{sr})}$	-0.51 ± 0.19	0.124 ± 0.049	0
$\rho_{\Delta(1/\beta_0),\Delta(1/\zeta_{sat})}$	0	-0.154 ± 0.059	0
$\rho_{\Delta(1/\zeta_{sr}),\Delta(1/\zeta_{sat})}$	0	-0.072 ± 0.045	0



0.18 μm CMOS





Example: Current Mirror

$$\frac{\Delta I_D}{I_D} = \frac{g_m}{I_D}\Delta V_{TH} + \frac{\Delta\beta}{\beta}$$

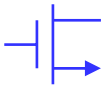
$$\sigma^2_{\Delta I_D/I_D} \cong \left(\frac{2}{V^*}\right)^2 \sigma^2_{\Delta V_{TH}} + \beta^2 \sigma^2_{\Delta(1/\beta)}$$

100µm/0.25µm NMOS

$$\sigma^2_{\Delta V_{TH}} \cong \frac{A_o}{WL} = \frac{33.3\times10^{-6}\,\mathrm{V^2\mu m^2}}{100\mu\mathrm{m}\times0.25\mu\mathrm{m}} = (1.15\mathrm{mV})^2$$

$$\left(\frac{W}{L}\right)^2 \sigma^2_{\Delta(1/\beta)} \cong \frac{A_o}{WL} + \frac{A_W}{W^2L} = \frac{6.1\times10^3\ \mathrm{V^4\mu m^2/A^2}}{100\mu\mathrm{m}\times0.25\mu\mathrm{m}} - \frac{0.91\times10^3\ \mathrm{V^4\mu m^3/A^2}}{(100\mu\mathrm{m})^2\times0.25\mu\mathrm{m}} = (15.6\ \mathrm{V^2/A})^2$$

$$\sigma^2_{\Delta I_D/I_D} \cong \left(\underbrace{\frac{1.15\mathrm{mV}}{200\mathrm{mV}}}_{0.58\%}\right)^2 + \left(\underbrace{200\frac{\mu\mathrm{A}}{\mathrm{V^2}}\times15.6\frac{\mathrm{V^2}}{\mathrm{A}}}_{0.31\%}\right)^2 = (0.66\%)^2$$



Example: Differential Pair

$$V_{os} = \Delta V_{TH} + \frac{V^*}{2}\frac{\Delta\beta}{\beta}$$

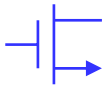
$$\sigma^2_{V_{os}} = \sigma^2_{V_{TH}} + \left(\frac{V^*}{2}\right)^2 \beta^2 \sigma^2_{\Delta\left(1/\beta\right)}$$

100µm/0.25µm NMOS

$$\sigma^2_{\Delta V_{TH}} \cong \frac{A_o}{WL} = \frac{33.3\times10^{-6}\,\mathrm{V^2\mu m^2}}{100\mu\mathrm{m}\times0.25\mu\mathrm{m}} = (1.15\mathrm{mV})^2$$

$$\left(\frac{W}{L}\right)^2 \sigma^2_{\Delta\left(1/\beta\right)} \cong \frac{A_o}{WL} + \frac{A_W}{W^2L} = \frac{6.1\times10^3\ \mathrm{V^4\mu m^2/A^2}}{100\mu\mathrm{m}\times0.25\mu\mathrm{m}} - \frac{0.91\times10^3\ \mathrm{V^4\mu m^3/A^2}}{(100\mu\mathrm{m})^2\times0.25\mu\mathrm{m}} = (15.6\ \mathrm{V^2/A})^2$$

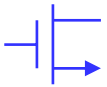
$$\sigma^2_{V_{os}} \cong (1.15\mathrm{mV})^2 + \left(\underbrace{\frac{120\mathrm{mV}}{2}\times200\frac{\mu\mathrm{A}}{\mathrm{V^2}}\times15.6\frac{\mathrm{V^2}}{\mathrm{A}}}_{0.19\mathrm{mV}}\right)^2 = (1.17\mathrm{mV})^2$$



"Careful" Layout

- Minimize systematic errors
  - Geometry
    - Proximity effects: diffusion, etch rate
    - Orientation
  - Gradients
    - Process
    - Temperature
    - Stress

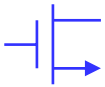
Ref: A. Hastings, "The art of analog layout," Prentice Hall, 2001



Layout Tradeoffs

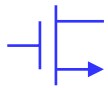
- Matching often involves tradeoffs:
  - Increased channel length
  - Increased circuit area
  - → increased power dissipation, reduced speed, …

- Determine required level of matching
  - Minimal:
    - $3\sigma_{Vos} > 10mV$, $3\sigma_{\Delta ID/ID} > 2\%$
    - Unit elements, matched orientation, compact layout
  - Moderate:
    - $3\sigma_{Vos} > 2mV$, $3\sigma_{\Delta ID/ID} > 0.1\%$
    - Apply most or all layout rules
  - Precise:
    - Trimming or self-calibration



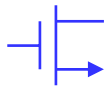
1. Unit elements

- Equal L
- Equal W (use M)



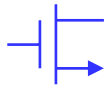
2. Large Active Areas

- Reduce random variations
- Use statistical analysis as a guide



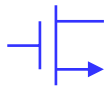
3. Bias Point

- Voltage matching (differential pair):
  - Small V*
  - Long L
- Current matching (mirror):
  - Large V*
  - Same V_{DS}



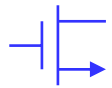
4. Same Orientation

- Transistors “look” symmetrical
- Actual devices are not:
  - Silicon is not isotropic
  - Implants are not isotropic
- What about ac?



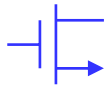
5. Compact Layout

- Minimize stress and temperature variations & random fluctuations
- Avoid poor MOSFET aspect ratio
  - E.g. W/L = 1000/0.35
  - Use fingers: 50/0.35, M=20
    → ~ square layout



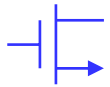
6. Common Centroid Layout

- Cancels linear gradients
- Required for moderate matching
- Common-centroid rules:
  - Coincidence
  - Symmetry
  - Dispersion
  - Compactness
  - Orientation



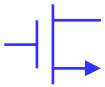
7. Dummy Segments

- Place dummy segments at ends of arrayed devices
- Protects from processing non-uniformity e.g. etch-rate



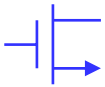
8. Stress Gradients

- Global: from package
  - Place devices in areas of low stress
  - Generally center of chip
  - At odds mixed-signal floor plans
- Local: metalization
  - Do not route metal across active area
  - If unavoidable: add dummies so that each device sees same amount of metal



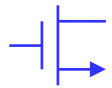
9. Contacts

- Do not place contacts on top of active area
  - Induce threshold mismatch
  - God knows why …
- Compromise: minimize the number and make each gate identical
- Beware of proximity effects when connecting multiple gates with poly
  - Use metal interconnects or
  - Use poly connectors on either side of transistor



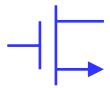
10. Junctions

- Keep all junctions and deep diffusions away from transistors (except S/D)
  - Extend well boundary at least 2x junction depth
  - Just because the layout rule permits it, minimum spacing is not always the best solution
    - Not all spaces are critical for overall layout area



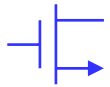
11. Oxide thickness

- Devices with thinner oxide usually exhibit better matching
  - Use minimum t_{ox} devices for best matching if the process offers a choice



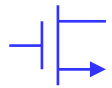
12. NMOS vs PMOS

- NMOS usually exhibit better matching than PMOS
  - Why?
  - Random matching, 0.18μm data:
    - V_{TH} of PMOS has better matching (2x)
    - β of NMOS matches better (4.5x !)



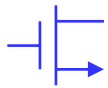
13. Power Devices

- Power devices create temperature gradients and inject carriers into the substrate
  - $dV_{TH} / dT = -2mV/^oC$!
- Keep matched devices away from power sources (>50mW)
- Beware of "Temperature Memory Effect": Use common-centroid layout for matched devices with different current density



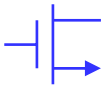
Common-Centroid Layout

- Determine groups of matched components
  - Depends on circuit function
  - E.g.
    - All transistors in a mirror
    - Diff-pair and load in an amplifier
      - Should they be matched individually or jointly?
- Divide into segments
  - Unity element
  - Avoid small (<70%) fractional elements if no GCD



Common-Centroid Patterns

- Coincidence:
  - Center of all matched devices co-incide
- Symmetry:
  - X- and Y-axis
  - R's and C's exhibit 1-axis symmetry
- Dispersion:
  - High dispersion reduces sensitivity to higher order (nonlinear) gradients
  - E.g.
    - ABBAABBA: 2 runs (ABBA) of 2 segments (AB, BA)
    - ABABBABA: 1 run of 2 segments (AB, BA)
    - → ABABBABA has higher dispersion (preferable)



Common-Centroid Patterns

- Compactness:
  - Approximately square layout
  - 2D patterns
    - Better approximation of square layout
    - Usually higher dispersion possible, e.g.

$_{D}A_{S}B_{D}$
$_{D}B_{S}A_{D}$

$_{D}A_{S}B_{D}B_{S}A_{D}$
$_{D}B_{S}A_{D}A_{S}B_{D}$

$_{D}A_{S}B_{D}B_{S}A_{D}$
$_{D}B_{S}A_{D}A_{S}B_{D}$
$_{D}A_{S}B_{D}B_{S}A_{D}$
$_{D}B_{S}A_{D}A_{S}B_{D}$

- Orientation:
  - Stress induced mobility variations: several percent error
  - Tilted wafers: ~5% error