EECS 240
Analog Integrated Circuits

Topic 16: Coupling Mechanisms

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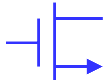
Department of Electrical Engineering and Computer Sciences

Coupling Mechanisms

- Interconnects
  - Mostly capacitive
  - Distance helps
  - Isolation in time
- Package (bond wires)
- Supply
- Substrate



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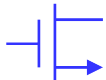
Package

- L, M (self and mutual inductance)
- dI/dt: beware of fast transients
  - Fast corner
  - Testing: cool chip!
- Differential circuits
- Orthogonal bond wires
- Isolation with time



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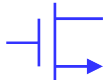
Power Supply

- Line / battery
- Regulator
- PCB Traces, decoupling
- IC package
- IC supply
- Circuit block



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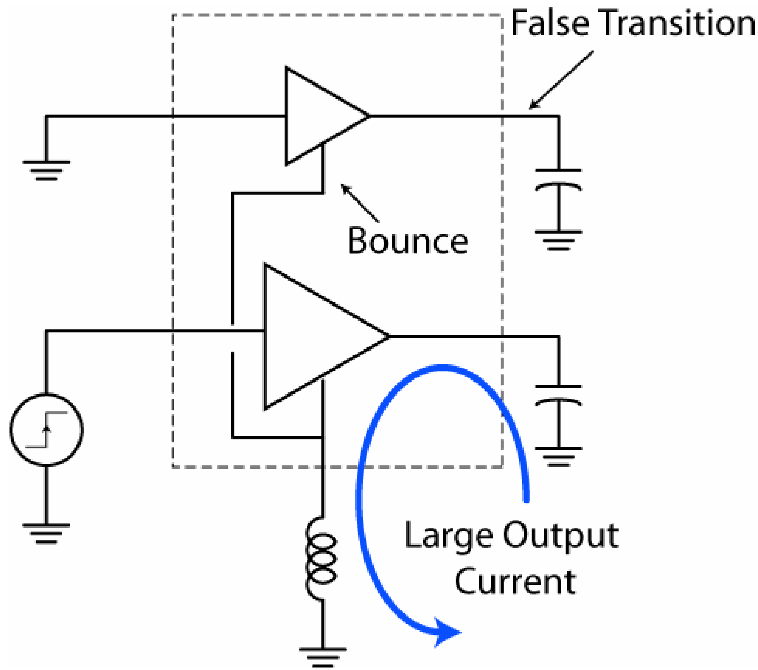
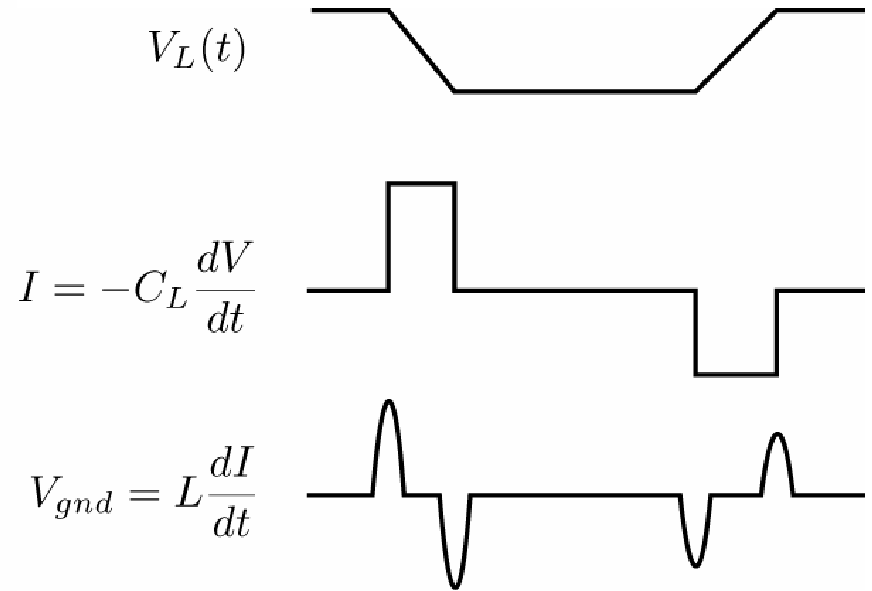
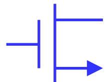
Source of "Noise"





- Large digital transitions draw current from supply and the pin inductance results in "noise".



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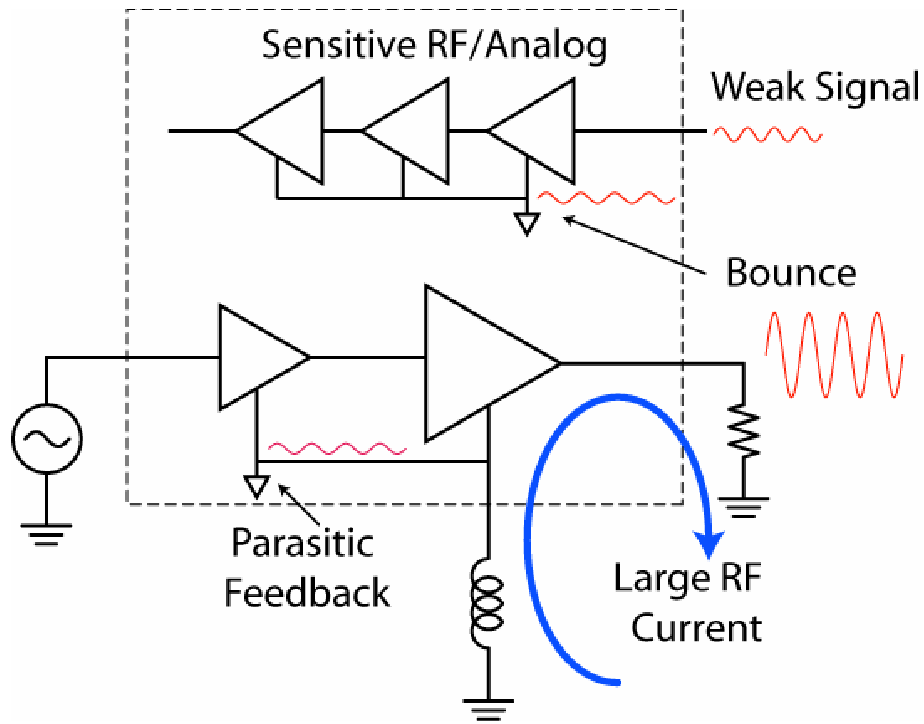
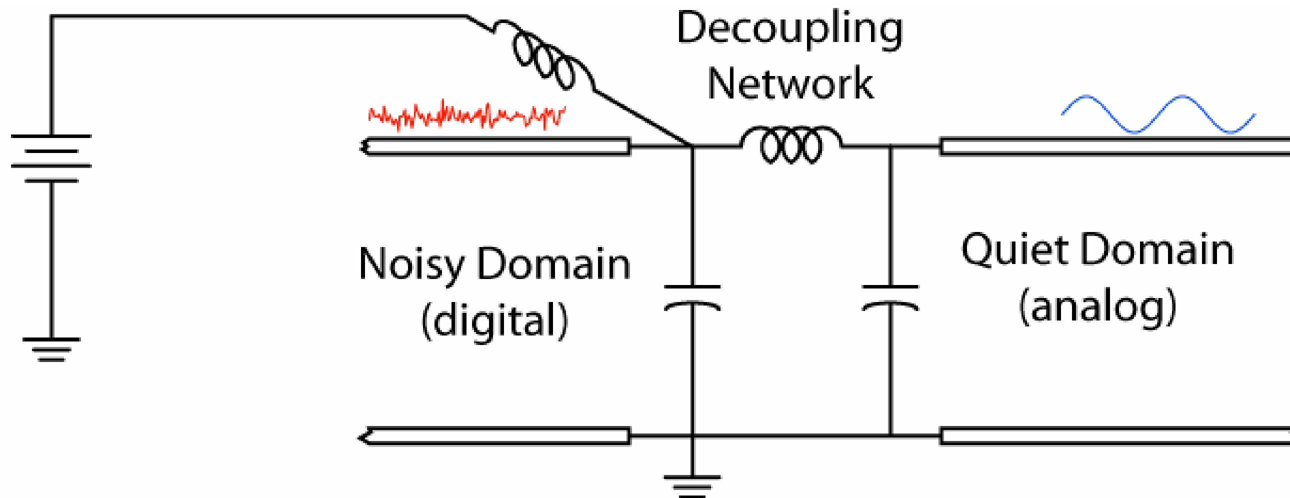
Analog "Noise"



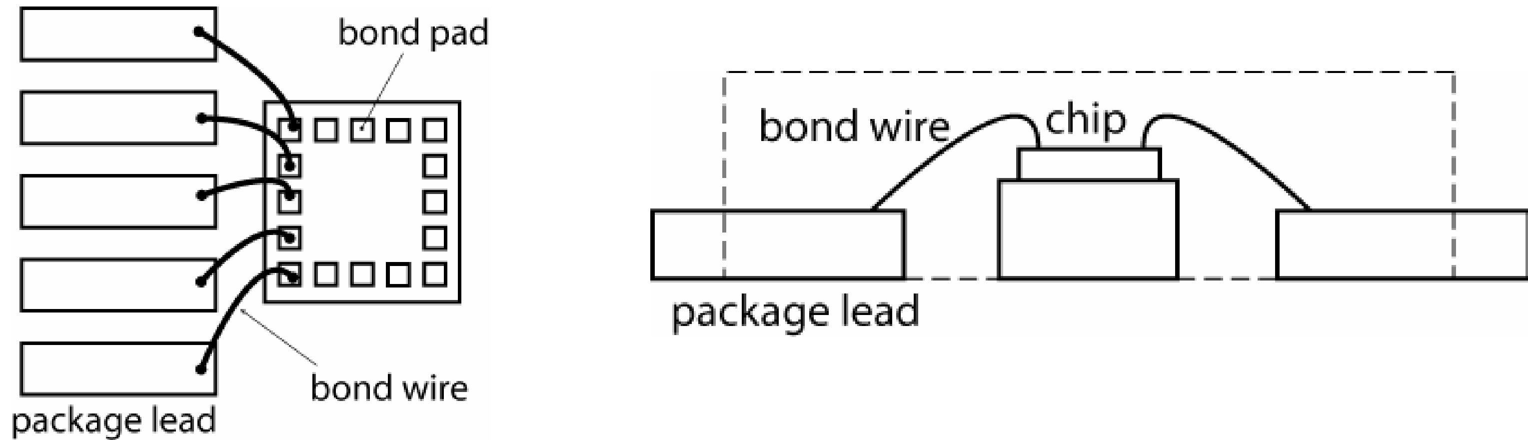
- Digital circuits are not the only culprits.
- Any circuit driving a large current off-chip generates "bounce".

Decoupling and Bypassing

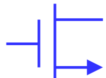


- Use bypass capacitors to minimize bounce.
- Use decoupling networks to isolate circuits.
- Use “beads” or resistors to de-Q the isolation networks.

Package Coupling



- Long bond-wires have large self-inductance and higher mutual coupling
- Inductance defined for a *closed loop*. Think of the entire current path, through the board, package, and board.



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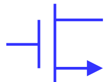
Pin Selection: Supply

- Adjacent pins good for low inductance power/ground.
- Orthogonal rectangular loops couple less. Think in terms of partial inductance.



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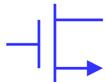
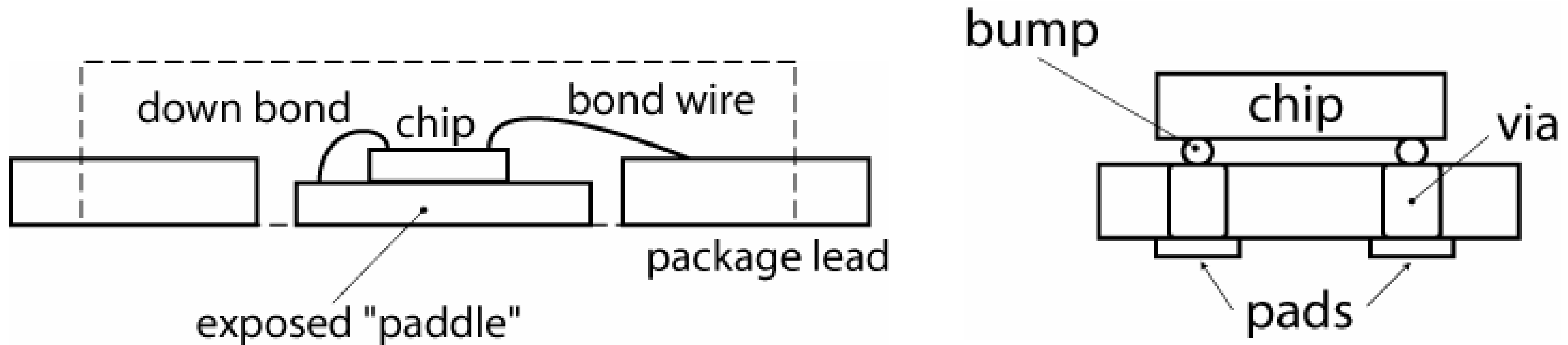
Pin Selection: I/O

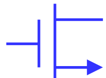
- Avoid noise pickup on analog inputs.
- Use signals pairs (not GND).
- Use common-mode cancellation techniques.



Advanced Packaging



- Downbonds used in an "exposed paddle" package for low inductance ground. Use many parallel bonds and thin the die if possible.
- In a flip-chip package, bumps form much lower inductance pins.



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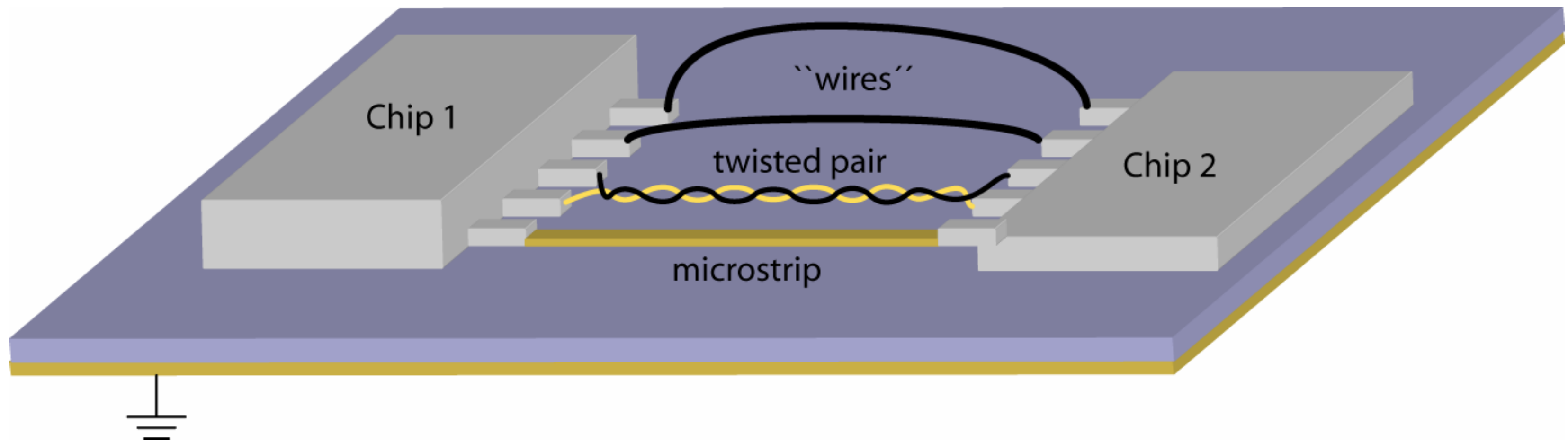
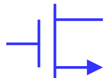
Long Signal Traces…



- Wires (or large traces) are bad since they form long loops with the "ground signal" (ground plane or another trace) and thus radiate and pick up much noise.
- Route signal + ground together to control and minimize the inductance loop. Better yet, go differential.
- Traces on the order of wavelength should be terminated. Microtrip transmission lines are good because they have a well defined Z0.



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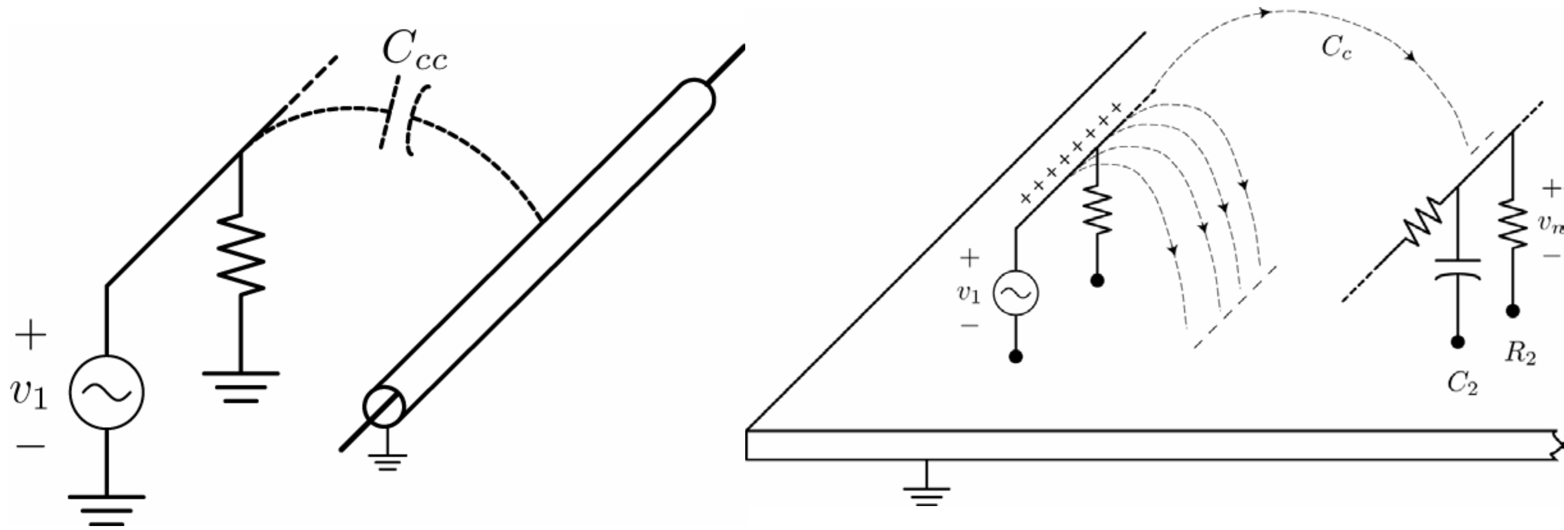
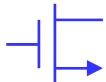
Electrical Coupling: Shield



- Shield only needs to be grounded at one point to shield electric field. Ground plane a good way to shield traces.



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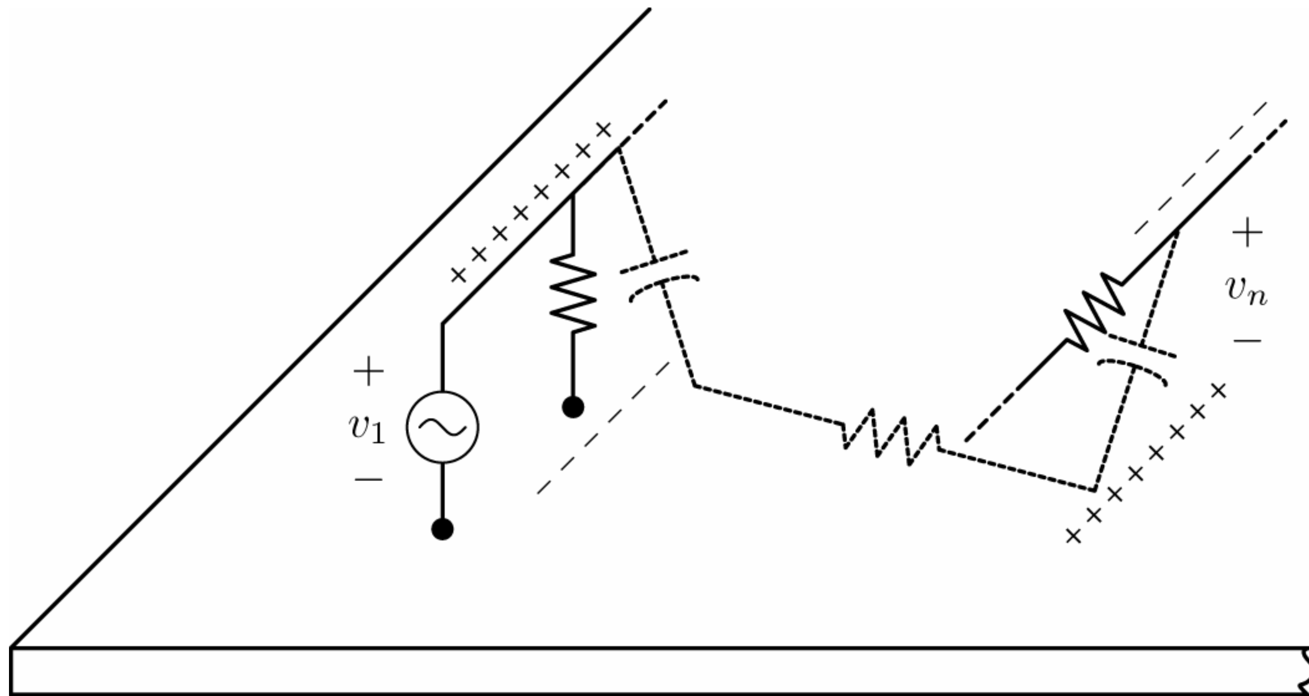
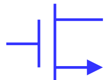
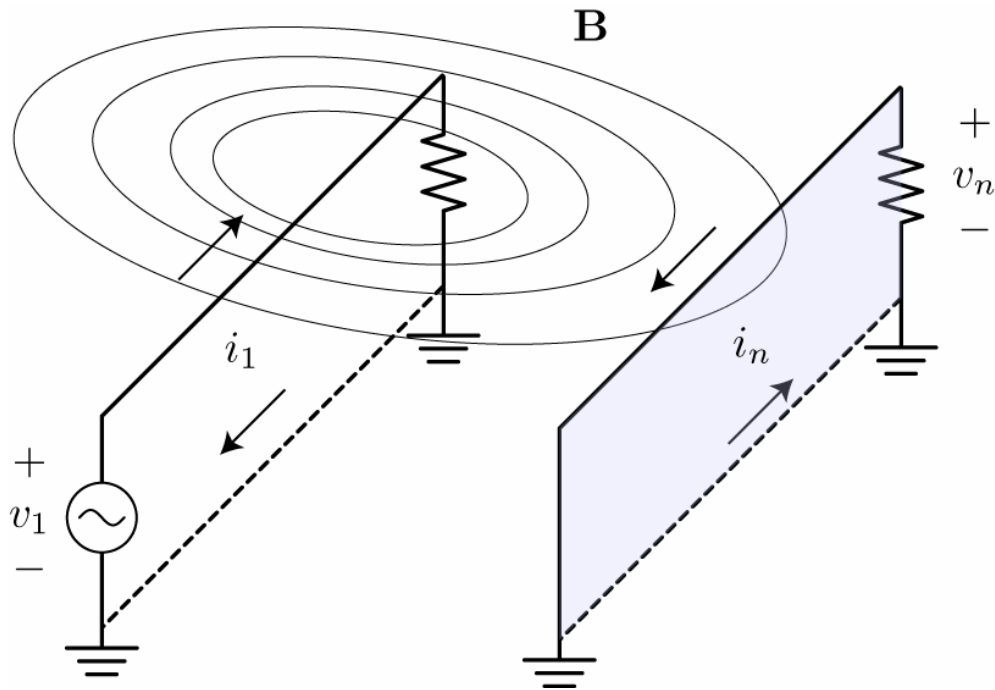
Ground the "Ground Plane"



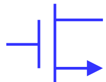
- An ungrounded floating "ground plane" can result in an unintended increase the electrical coupling from one circuit to another.



Magnetic Coupling



- Magnetic coupling occurs between wires or traces in a circuit due to magnetic flux leakage.
- Minimize both loops to minimize coupling!



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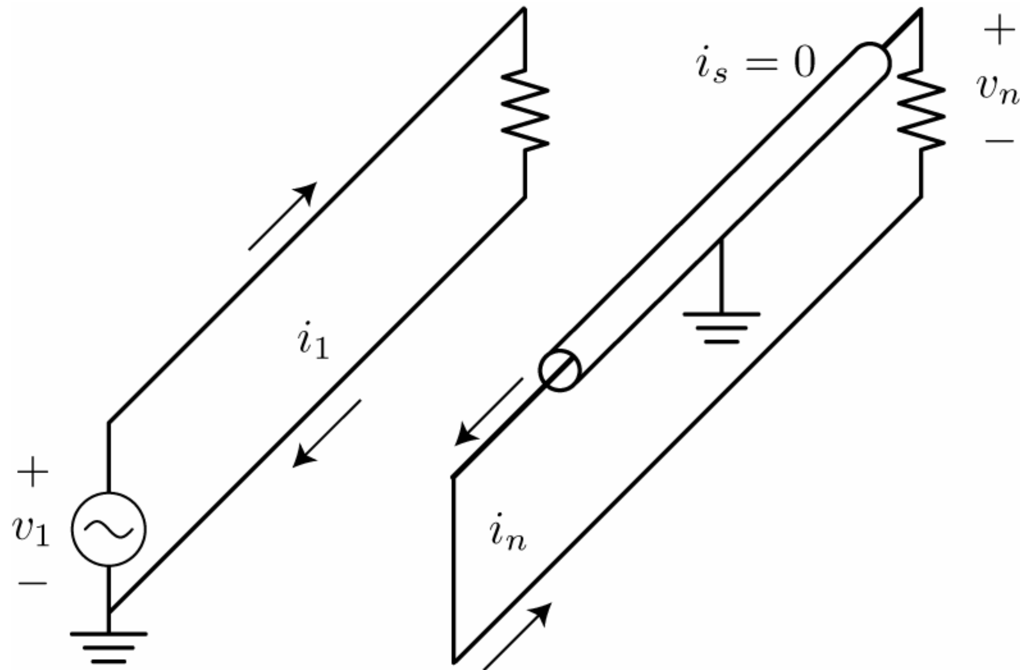
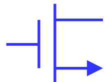
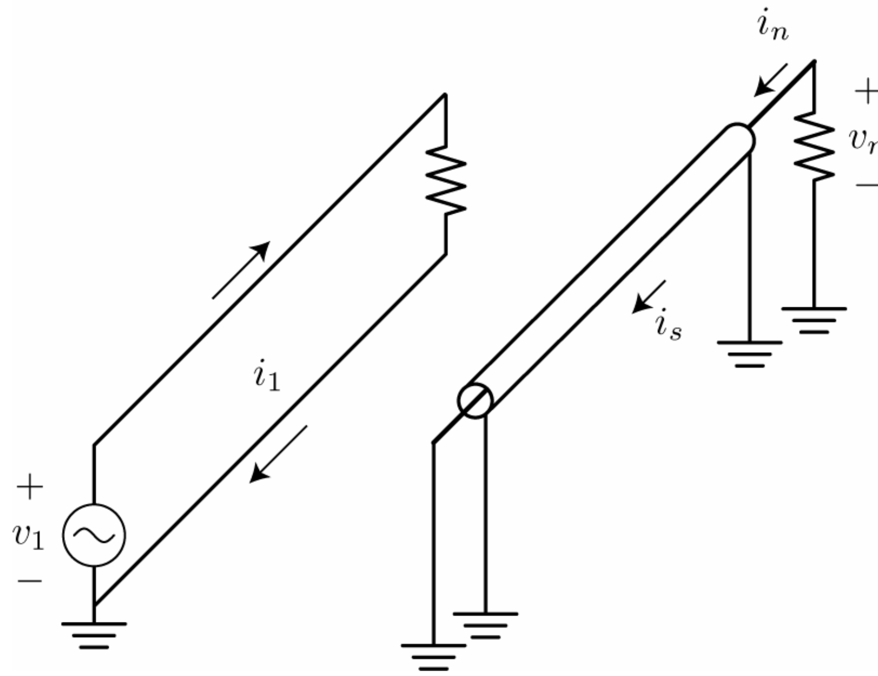
Magnetic Shielding?



- Will this work?

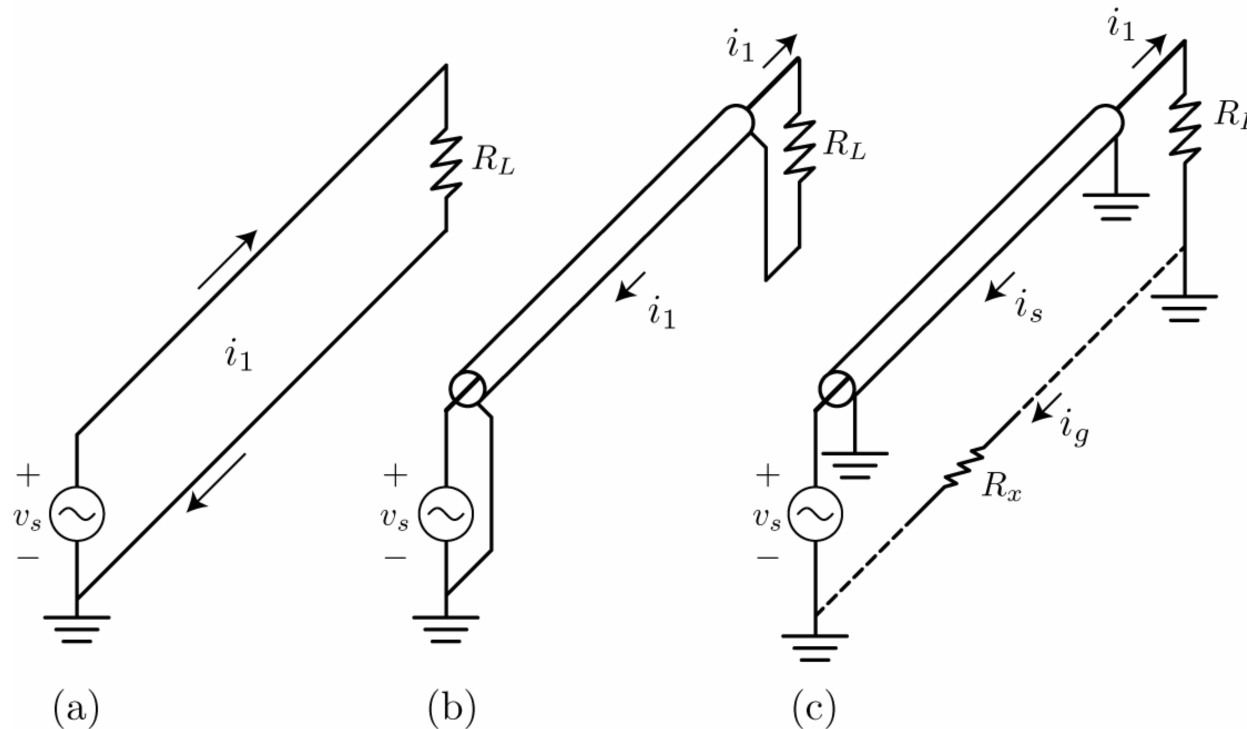


Magnetic Shielding

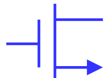


- The current must flow in the shield to be effective. The return current flows nearby reducing the loop area.

Harmful Ground Connections



- At low frequencies the current takes past of least resistance. So in (c) current will flow in ground plane and present a large capture area, like (a). (b) is best.



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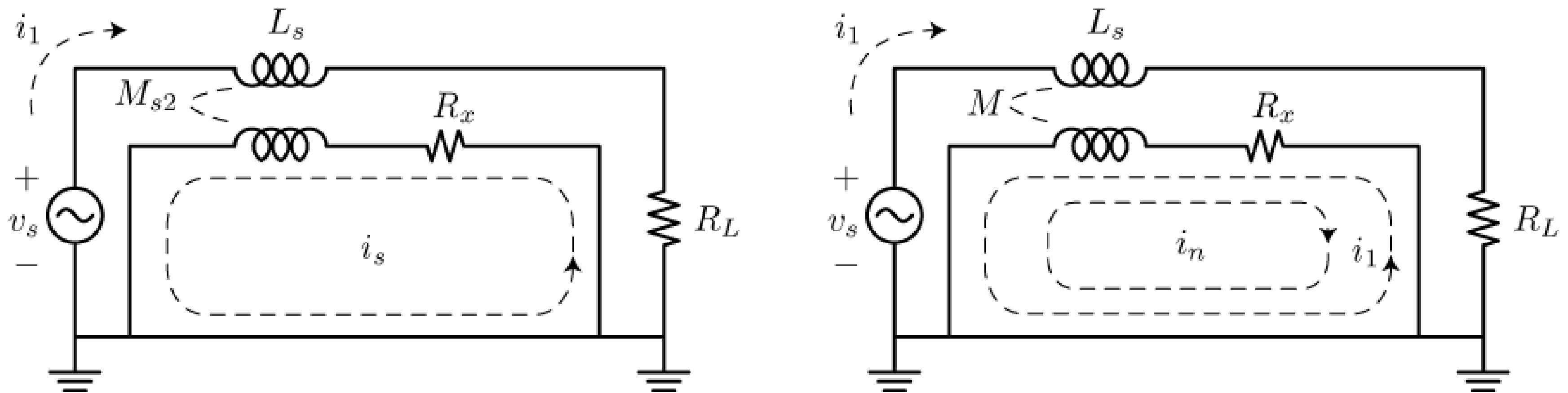
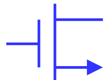
Ground Noise



- Model shows that if a ground loop is formed, noise currents can flow and create noisy signals due to "shield" resistance.



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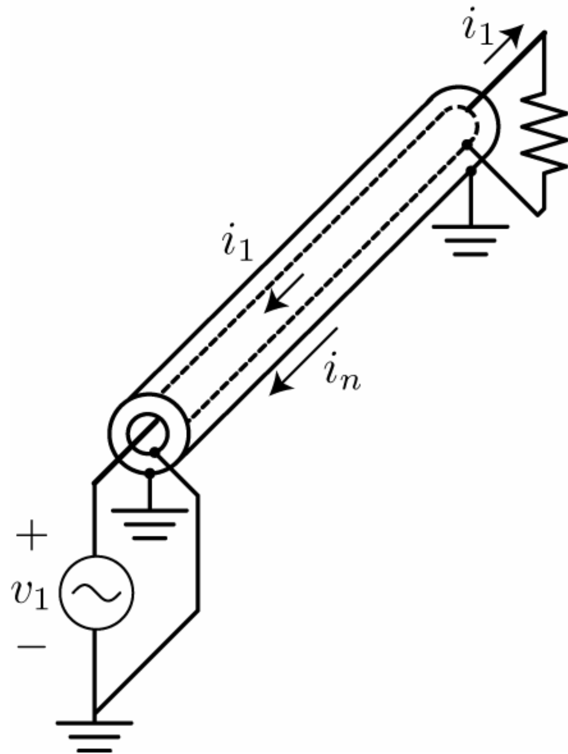
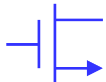
Why go Triax?



- A triaxial conductor structure is used to prevent the flow of ground loop currents inside the signal conductor.
- Coaxial structures acts as triaxial shields at very high frequencies due to skin effect.



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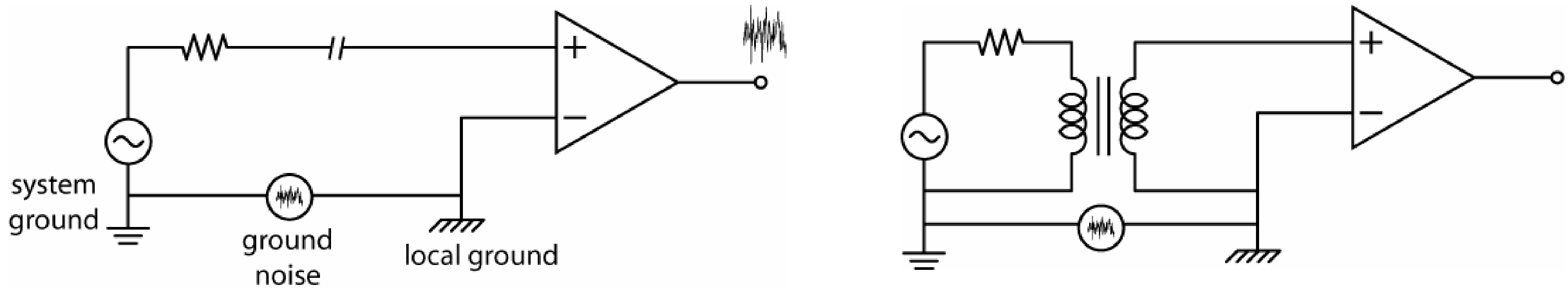
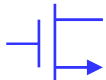
Balancing Act



- Ground noise models the fact that the ground potential is not constant but varies from point to point.
- Don't want to amplify ground noise!



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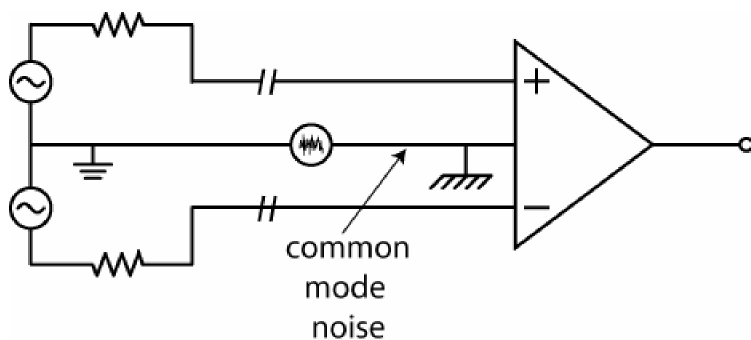
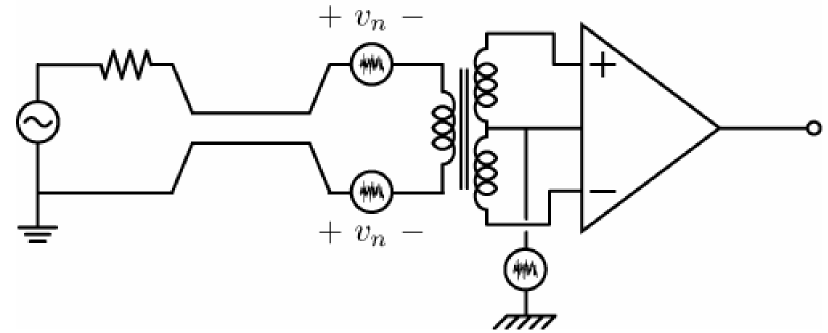
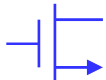
Common Mode Rejection





- Differential circuits reject ground noise since it's a common mode signal.
- Use a balun if your source isn't differential.



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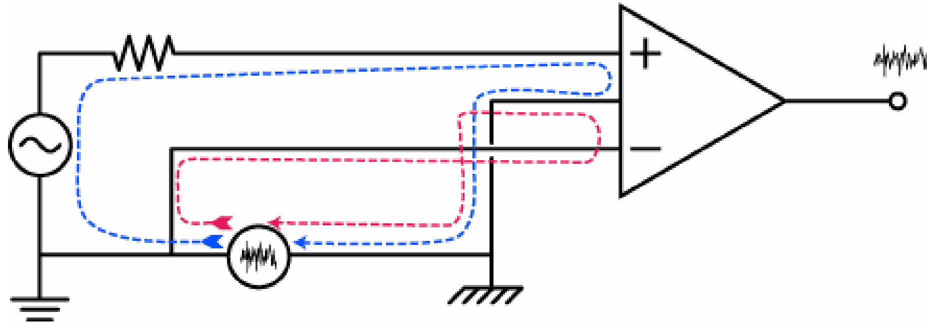
Keep Your Balance



- Any imbalance in a circuit can lead to a noisy differential input voltage.
- Since the path through the source includes the source resistance, it has a different impedance than the return current path.
- A fully balanced source has a symmetric impedance to ground from either terminal.

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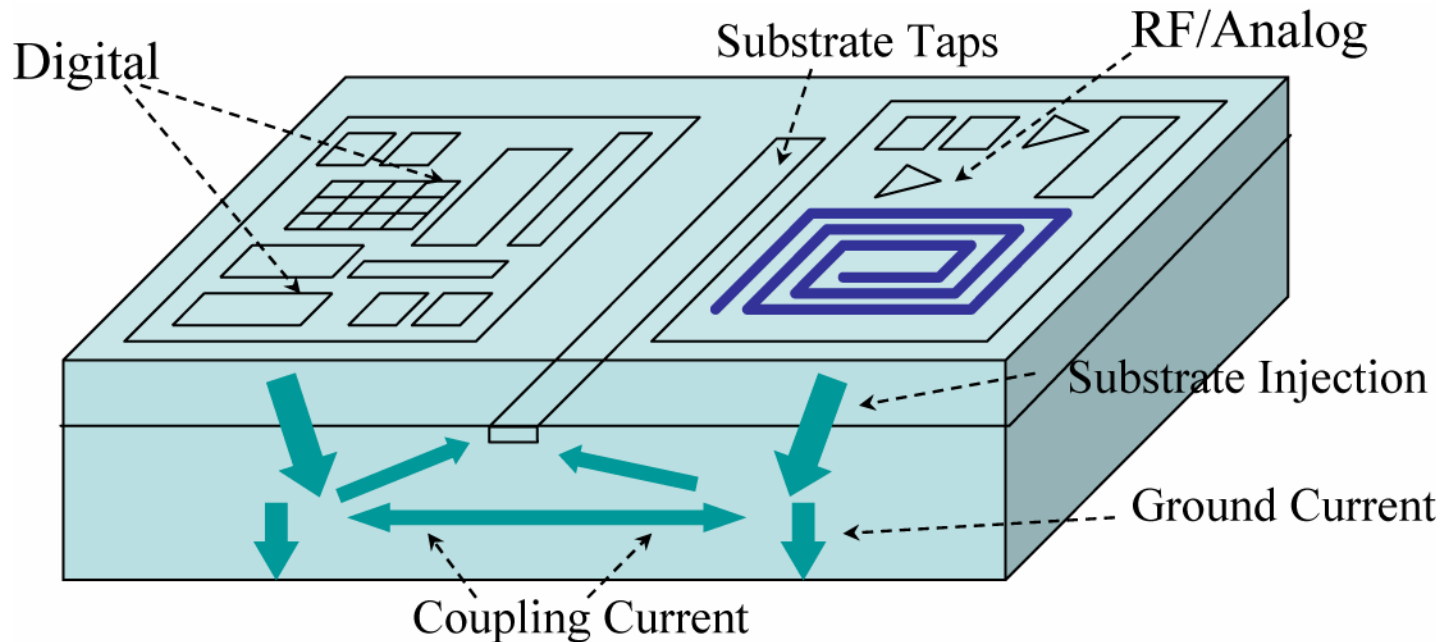
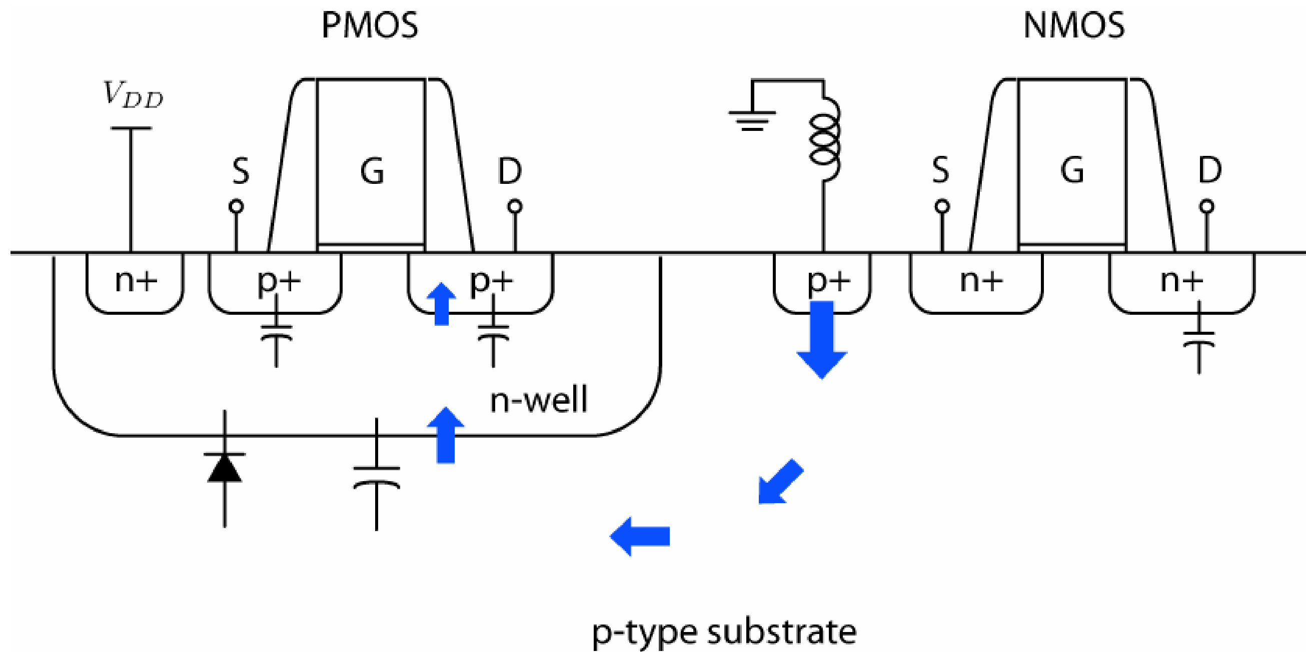
Substrate

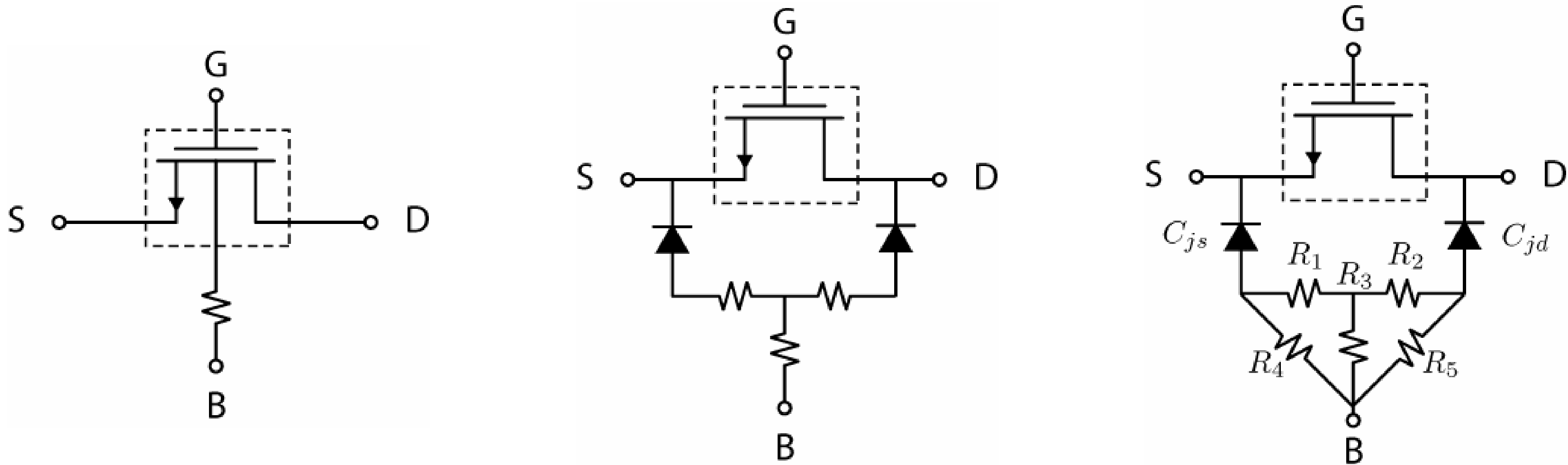


- Every node in your circuit is connected to every other node through the substrate!

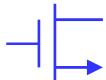
Typical Injection/Reception



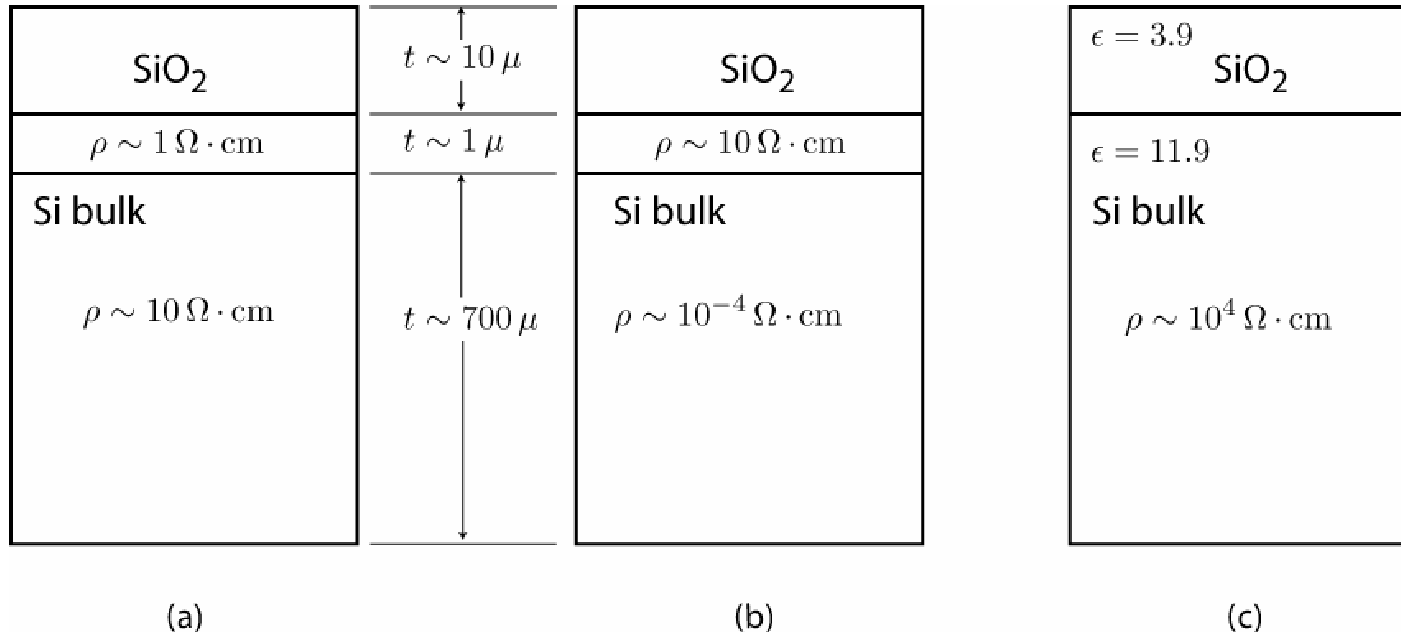
FET Substrate Network



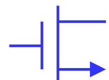
- FETs couple to substrate through their body contact. For well isolated devices, the coupling occurs through well capacitance.



Substrate Profiles



- Undoped substrate is special order. Typically the substrate is moderately conductive or heavily conductive (epi-substrate).



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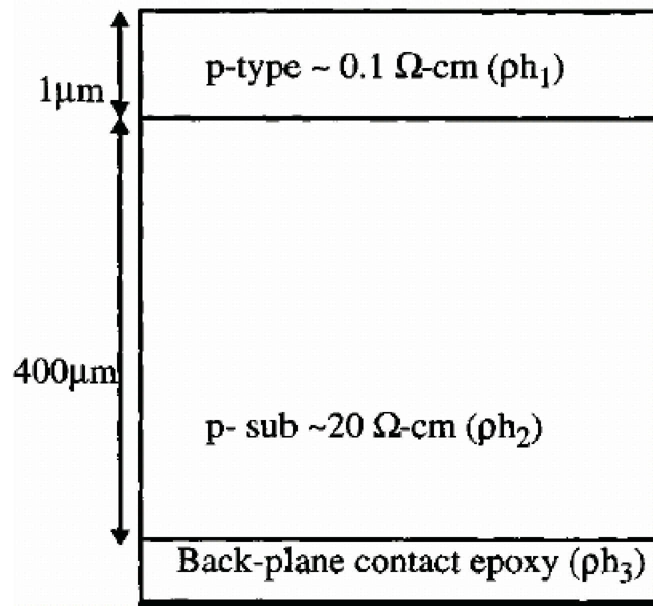
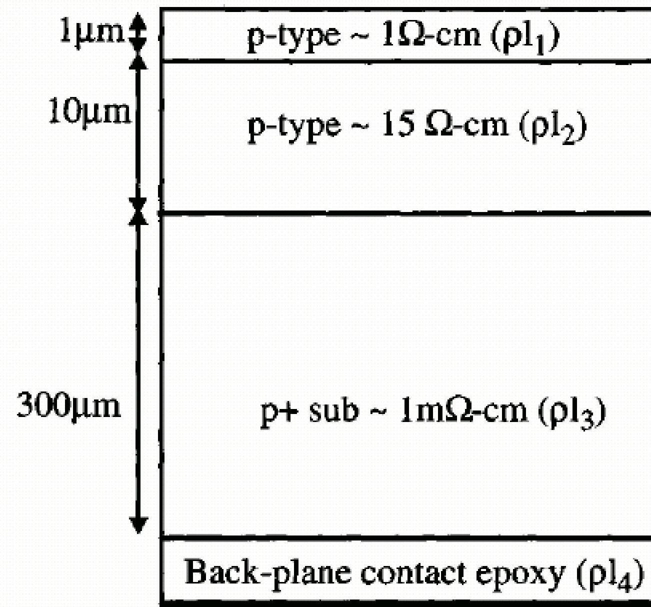
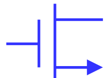
Common Substrate Types







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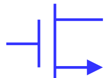
Epitaxial Substrate

Oscilloscope
50 Ω
Ring Oscillator (on chip)
–5 V
–3 V
–5 V
RG 174
Switching Noise Source
Source
Gate
Drain
0.2 pF
N+
N+
P+
7 μm
Current Source Transistor
Substrate Contact
P⁻ Epitaxial Layer (15 Ω-cm)
P+ Channel Stop Implant (1 Ω-cm)
300 μm
P+ Bulk (0.05 Ω-cm)

Note:
Lack of backside wafer contact substantially increases coupling!

D. K. Su, M. J. Loinaz, S. Masui, and B. A. Wooley, "Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits," *IEEE Journal of Solid-State Circuits,* vol. 28, pp. 420 - 430, April 1993.



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Observed Waveforms

-0.434
-0.436
-0.438
-0.440
-0.442
-0.444
-0.446

V_{out} (V)

V_{P-P} = 10.7 mV

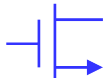
Settling Time
to within 0.5 mV

= 6.8 ns

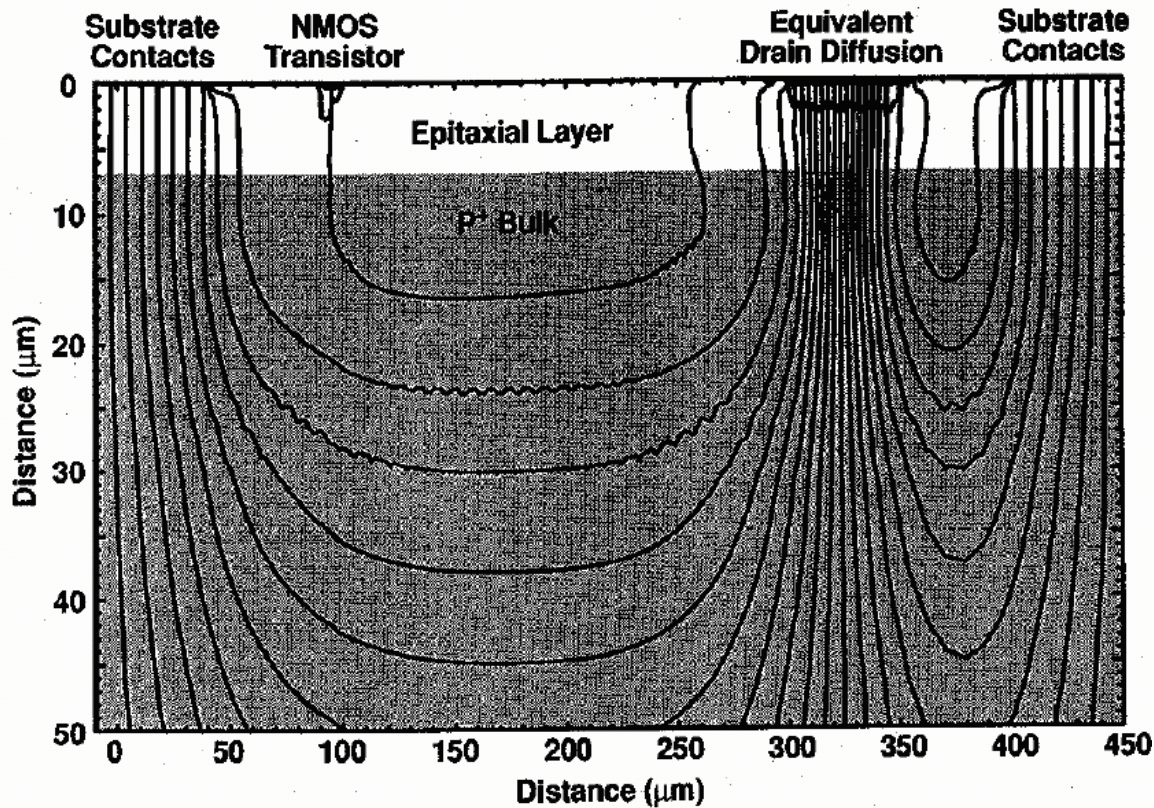
1 mV

0 20 40 60 80 100 120 140 160

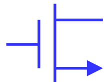
Time (ns)



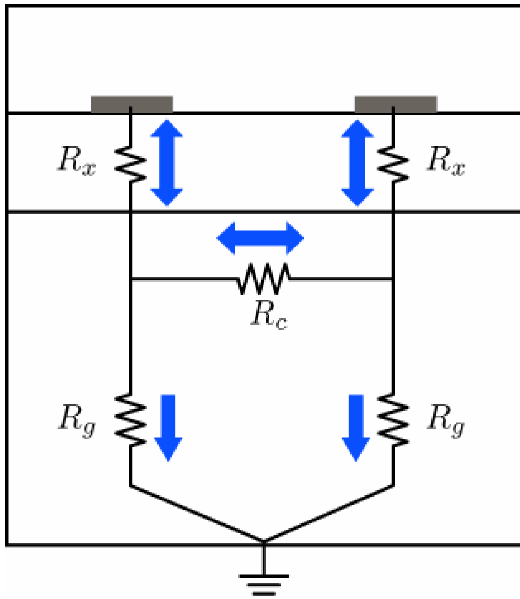
Current Flow in Epi-Substrate



- Majority of current flows in low-resistivity wafer
- Coupling is very weak function of distance



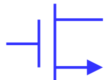
Model for Cross-Talk



$$f_r = \frac{\rho}{\epsilon}$$

$$f_r = \frac{10}{11.9 \times 8.854 10^{-12}} \sim 94\text{GHz}$$

- Below the dielectric relaxation frequency, the coupling is resistive.



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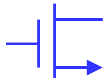
Cross-Talk versus Distance



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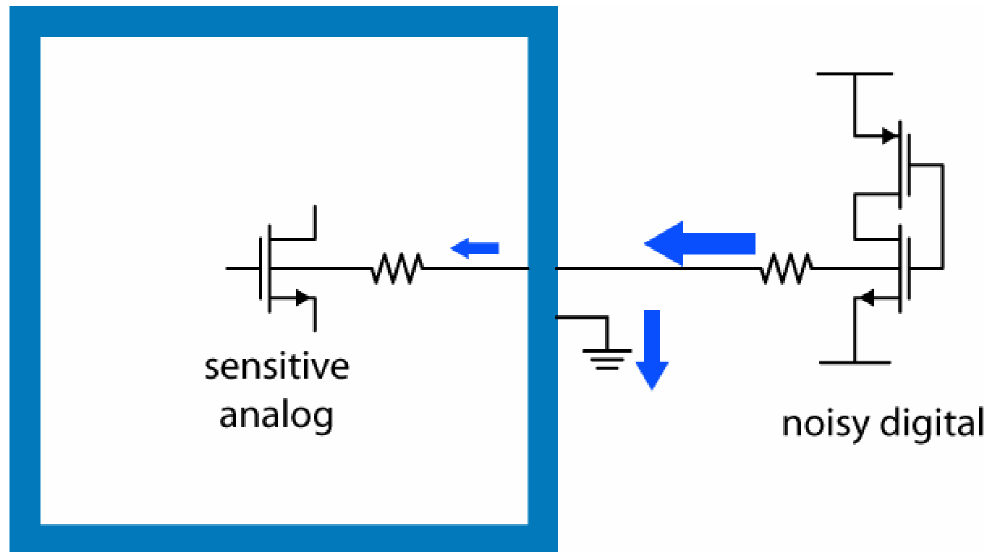
Guard Ring



- Can we build a shield with a guard ring?

Effect of Guard Ring

No P^+ Guard Ring
With P^+ Guard Ring

Peak-to-Peak Noise (mV)

16
14
12
10
8
6
4
2
0

6-μm distance
22-μm distance
(dedicated package pin)

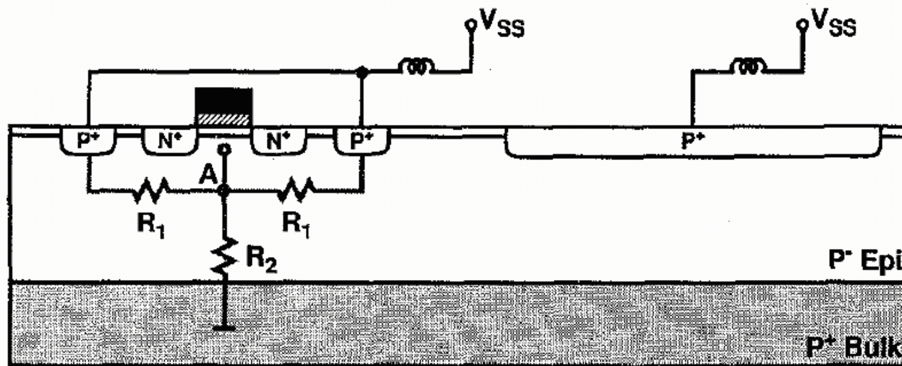
6-μm distance
22-μm distance
(connected to large substrate contact)

Guard Ring Configuration

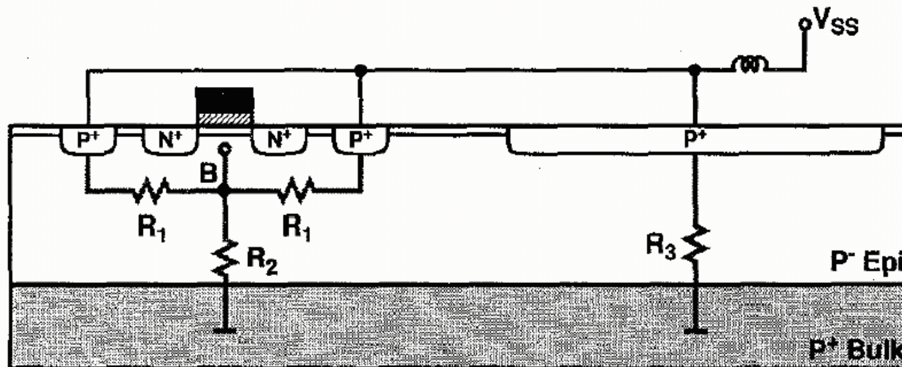
Large guard rings increase coupling!

Epi substrate

Model for Guard Ring

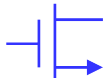


(a)



(b)

Shared guard ring contact reduces isolation!



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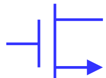
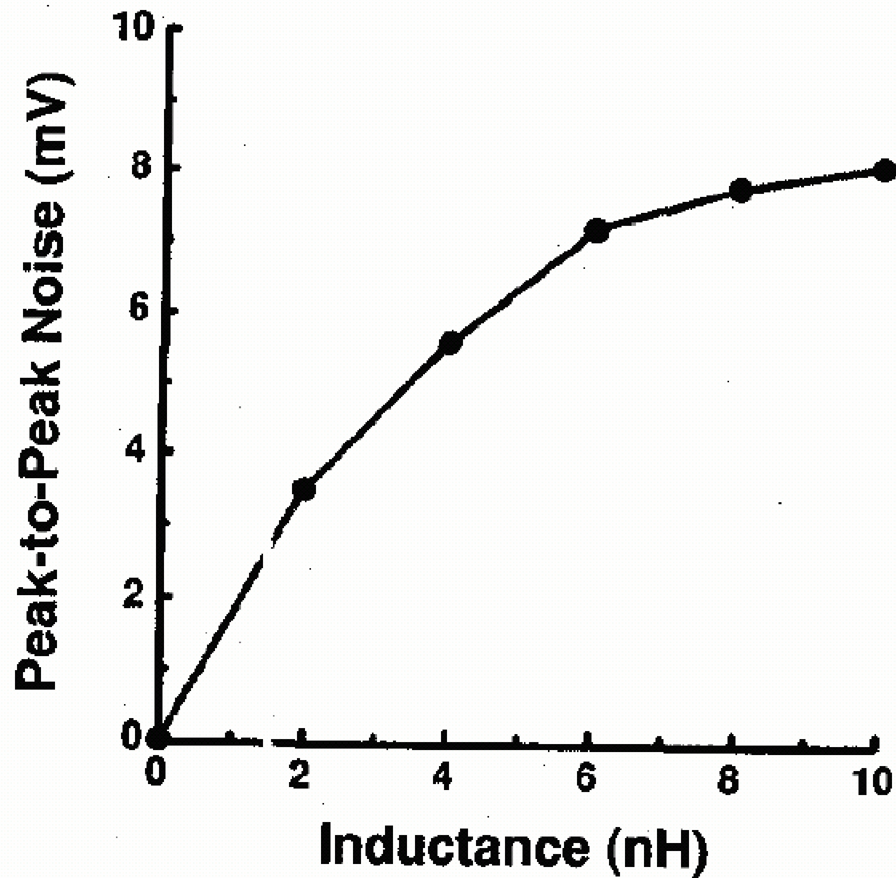
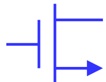
Backside Contact

–3 V
–5 V
L_1
1-ns edge
50Ω
+
V_{out}
-
L_2
L_3
–5 V
(200 μm)
P+
N+
N+
N+
P+
50 μm
d
50 μm
50 μm
Device Structure
P– Epitaxial Layer
P+ Channel Stop Implant
(90 μm)
P+ Bulk
C_1
L_4 (for backside contact only)
–5 V
–5 V



Noise vs L_4



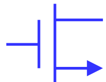


Current in High Resistivity Substrate

Substrate Contact
NMOS Transistor
Equivalent Drain Diffusion
Substrate Contact

Distance (μm)
0
10
20
30
40
50

0
50
100
150
200
250
300
350
400
450
Distance (μm)



Simulation / Analysis

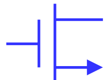
R. Gharpurey and R. G. Meyer, "Modeling and analysis of substrate coupling in integrated circuits," *IEEE Journal of Solid-State Circuits,* vol. 31, pp. 344 - 353, March 1996.

Balsha R. Stanisic, Nishath Verghese, Rob A. Rutenbar, L. Richard Carley, David J. Allstot; *Addressing substrate coupling in mixed-mode ICs: Simulation and power distribution synthesis*, IEEE Journal of Solid-State Circuits, vol. 29, pp. 226 - 238, March 1994.

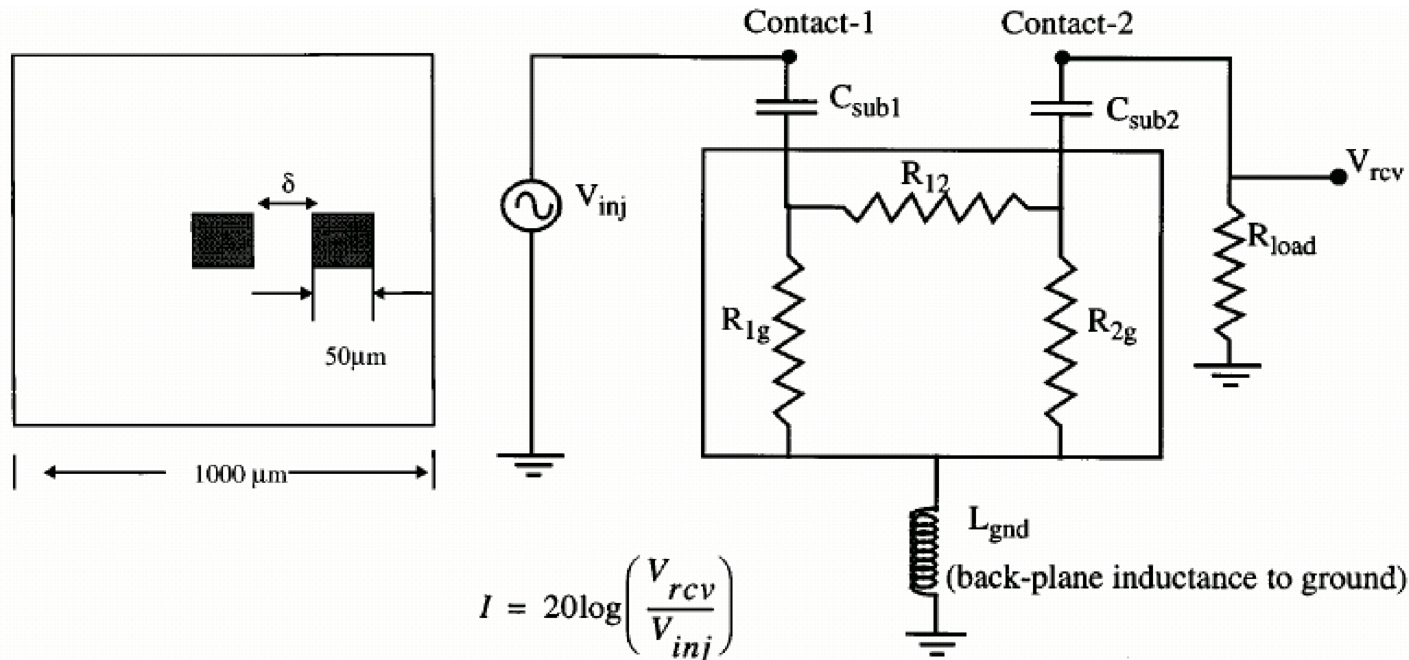
Kuntal Joardar; *A simple approach to modeling cross-talk in integrated circuits*, IEEE Journal of Solid-State Circuits, vol. 29, pp. 1212 - 1219, October 1994.

Nishath Verghese, David J. Allstot; *Computer-aided design considerations for mixed-signal coupling in RF integrated circuits*, IEEE Journal of Solid-State Circuits, vol. 33, pp. 314 - 323, March 1998.

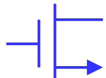
A. Samavedam, A. Sadate, K. Mayaram, and T. S. Fiez, "A scalable substrate noise coupling model for design of mixed-signal IC's," *IEEE Journal of Solid-State Circuits,* vol. 35, pp. 895 - 904, June 2000.



Epi Substrate Coupling



R. Gharpurey and R. G. Meyer, "Modeling and analysis of substrate coupling in integrated circuits," *IEEE Journal of Solid-State Circuits,* vol. 31, pp. 344 - 353, March 1996.



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Low Resistivity Substrate

Isolation (dB)

-42
-44
-46
-48
-50
-52
-54
-56
-58
-60

L_{gnd}=5nH

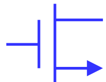
L_{gnd}=3nH

L_{gnd}=1nH

Extraction Time (20 Distance Values)
~4s (excluding FFT)
21.73 s (with FFT)
Frequency = 1GHz

0 100 200 300 400

Distance between contacts (µm)



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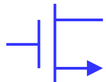
High Resistivity Substrate

Extraction Time (20 Distance Values)
19.66 s (with FFT)
~4s (excluding FFT)
Frequency = 1GHz

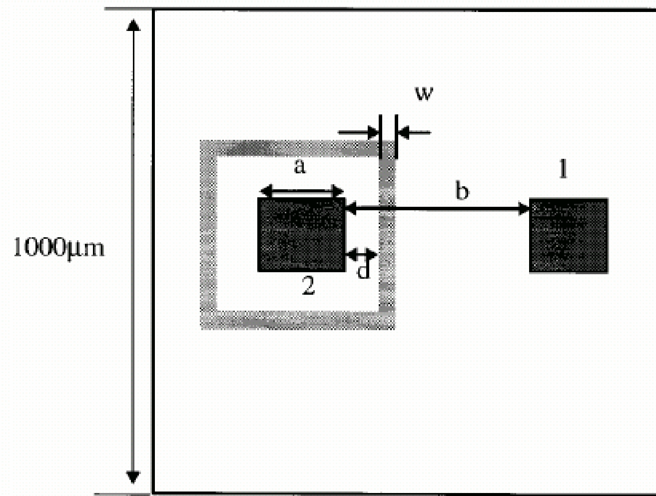
L_{gnd}=5nH
L_{gnd}=3nH
L_{gnd}=1nH

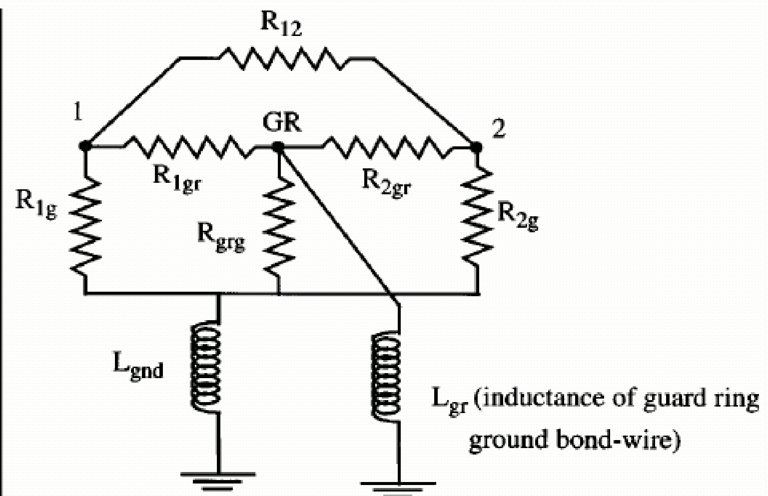
Isolation (dB)
-30
-35
-40
-45
-50
-55

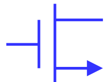
0
100
200
300
400
Distance between contacts (μm)



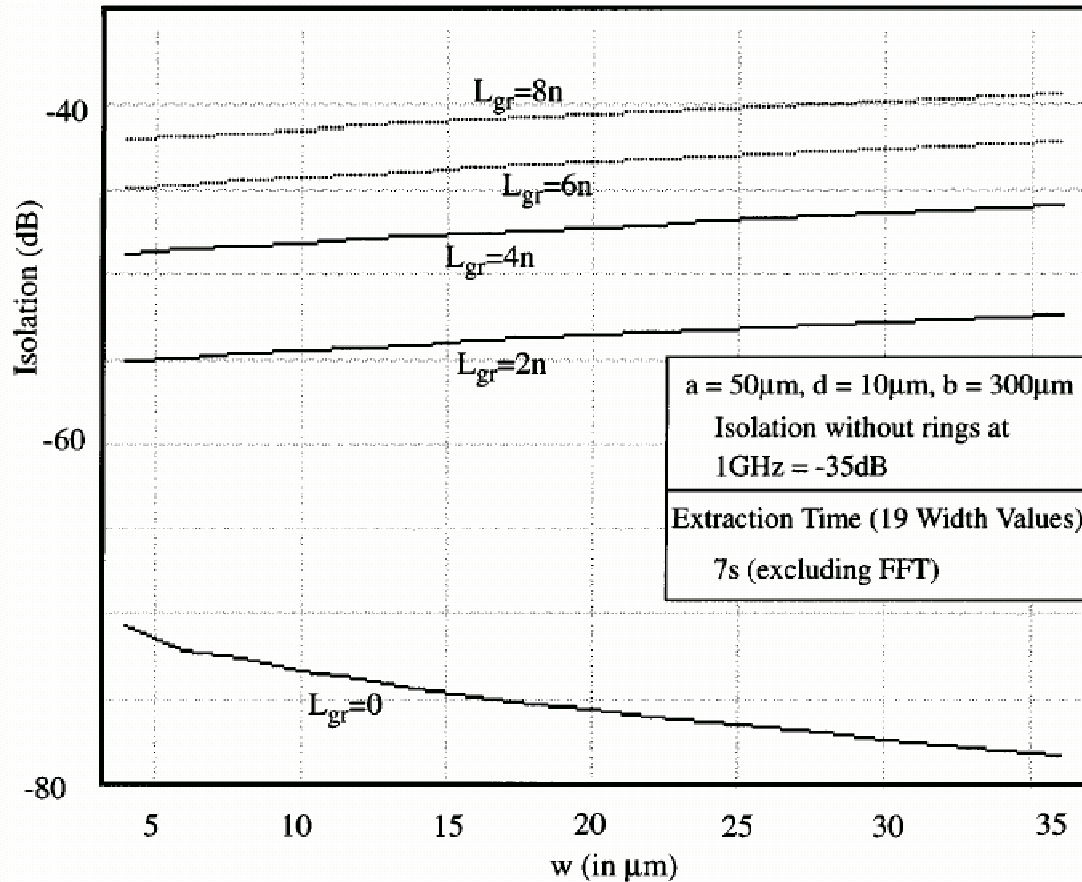
Guard Ring



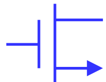




Guard Ring

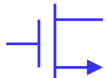


High resistivity substrate

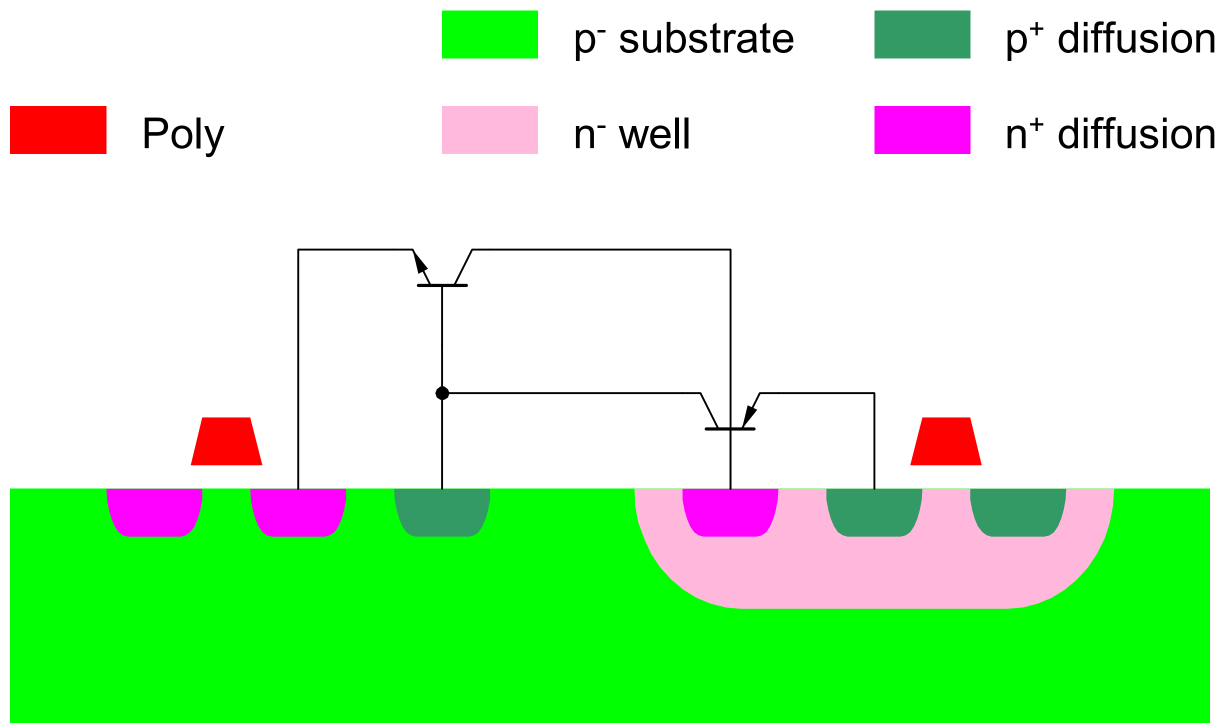


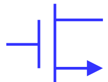
Guard Ring Guidelines

- Marginal improvement of isolation on heavily doped substrates
  - May still be needed to prevent latchup
- Dedicated grounds
- Keep guard ground bondwire away from signals
- Excessively wide / close guard rings reduce isolation
- Place guard ring close to sensitive node
- Use in analog and digital regions, analog being more important

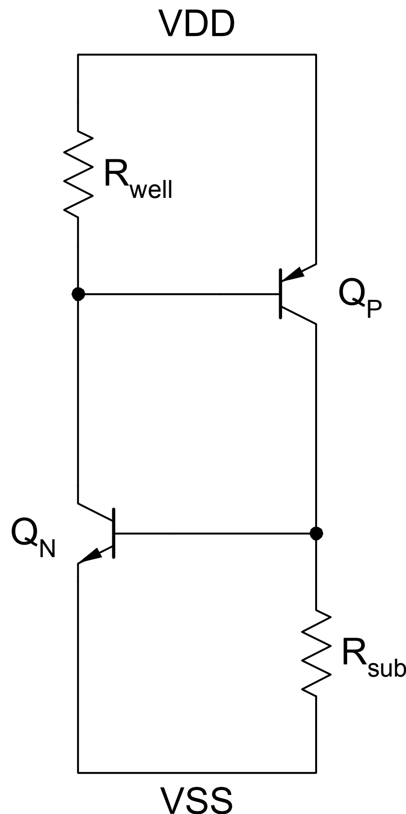


Latchup

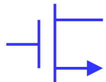




Latchup Circuit



- Latchup:
  - Forward biased junction → minority carrier injection
  - Q_N or Q_P turns on
  - Supplies I_B to Q_P or Q_N
  - Positive feedback if $\beta_N \beta_P > 1$
  - SCR: "silicon controlled rectifier"
- Preventing latchup:
  - $\beta_N \beta_P < 1$



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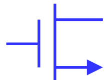
Preventing Latchup

- $\beta_N \beta_P < 1$
  - Increased layout spacing
    → increased parasitic base width
  - Increased doping
    → increased carrier recombination in base

- Prevent minority carrier injection
  - no forward biased junctions

- Minority carrier collectors



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