EECS 240
Analog Integrated Circuits

Topic 15: Comparators

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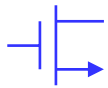
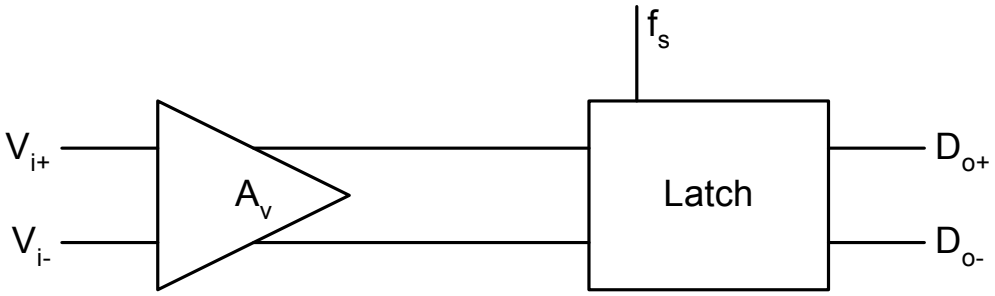


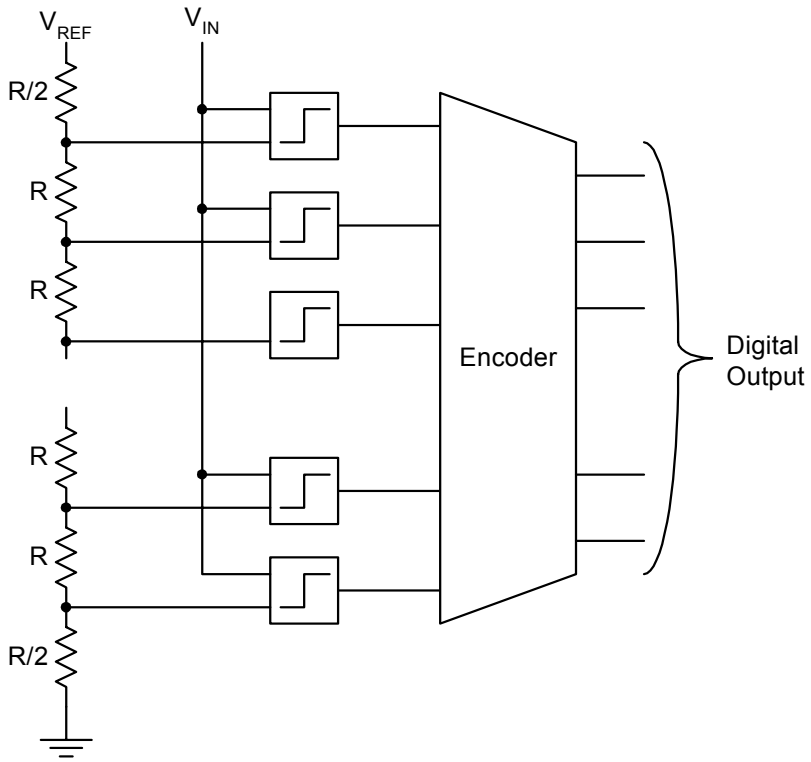
Comparator



- Clock rate f_s
- Offset
- Resolution
- Overload Recovery
- Input capacitance (and linearity!)
- Power dissipation
- Common-mode rejection
- Kickback noise
- …

Flash Converter

- Very fast: only 1 clock cycle per conversion
- High complexity: 2^B-1 comparators
- High input capacitance



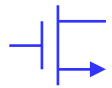
Comparator Gain

Example:

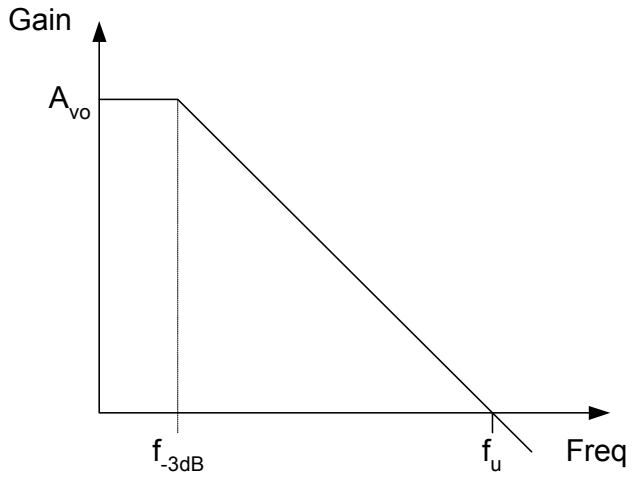
- 12-Bit / 100MS/s ADC
- 1V full-scale input

→ 1 LSB = 1V / 2^{12} = 240μV

→ A_v > 1V / 120μV = 8000 in 5ns!



Operational Amplifier?

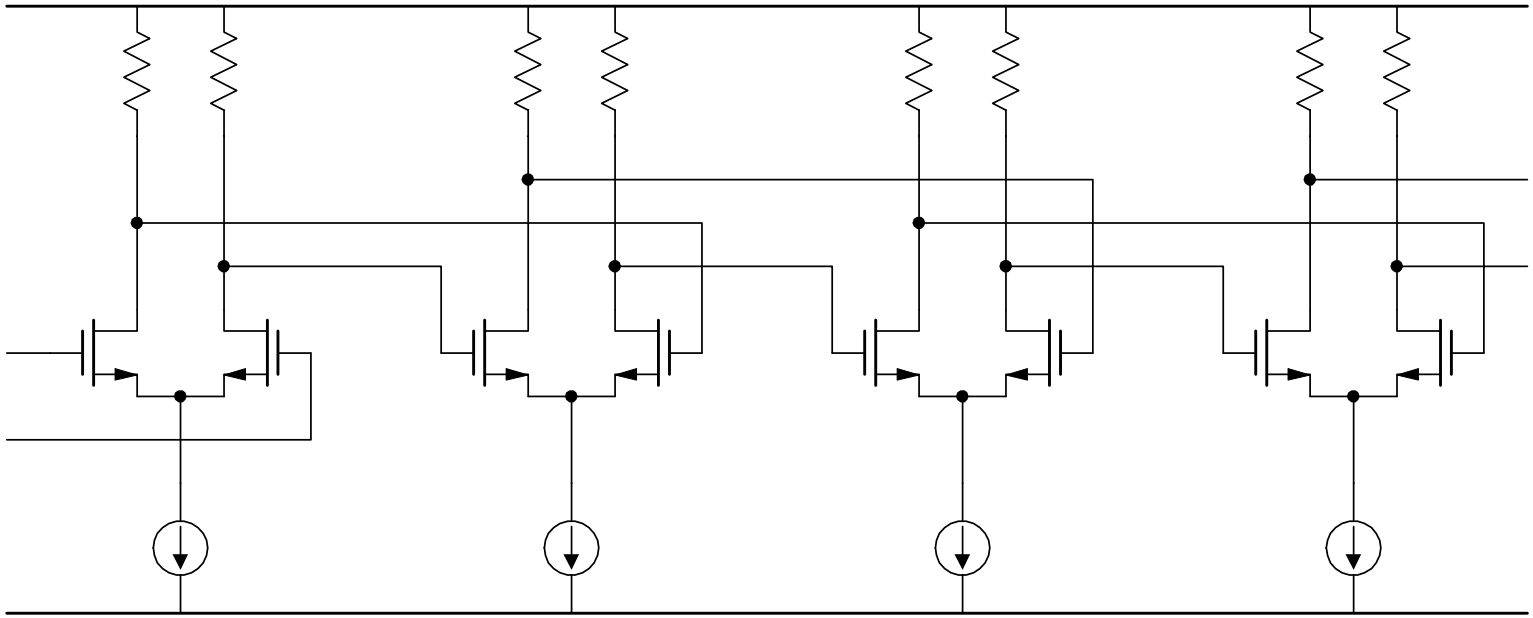


$$f_{-3dB} = \frac{f_u}{A_{vo}} \quad \rightarrow \quad \tau = \frac{1}{2\pi f_{-3dB}}$$

$$f_u = \frac{A_{vo}}{2\pi\tau}$$

$$= \frac{8000}{2\pi \times 1\text{ns}} = \underline{1.3\text{THz}}$$

Open-Loop Amplifier Cascade



Cascaded Amplifier

- Step response:

$$v_{o1}(t) = \frac{1}{C}\int_o^{T_d} g_m V_{in}\,dt = \frac{g_m}{C} T_d V_{in}$$

$$v_{o2}(t) = \frac{1}{C}\int_o^{T_d} g_m v_{o1}(t)\,dt = \frac{1}{2}\left(\frac{g_m}{C}\right)^2 T_d{}^2 V_{in}$$

$$v_{o2}(t) = \frac{1}{C}\int_o^{T_d} g_m v_{o1}(t)\,dt = \frac{1}{2}\frac{1}{3}\left(\frac{g_m}{C}\right)^3 T_d{}^3 V_{in}$$

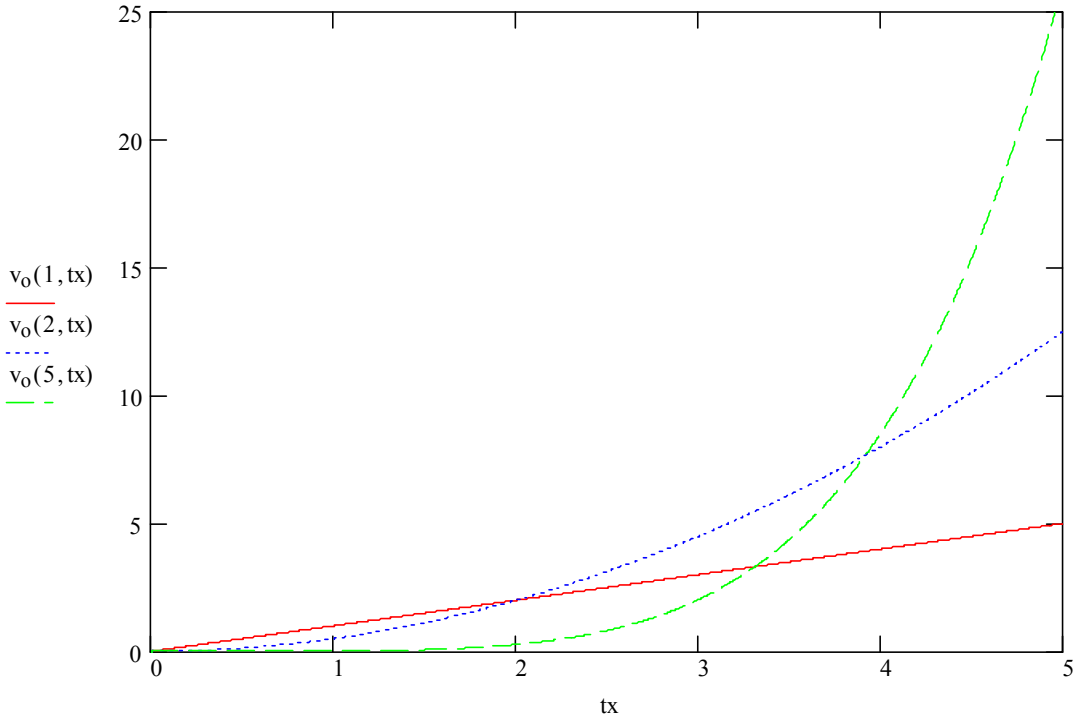
$$\vdots$$

$$v_{oN}(t) = \left(\underbrace{\frac{g_m}{C}}_{\sim\omega_T}\right)^N \left(\frac{T_d{}^N}{N!}\right) V_{in}$$

$$T_d = \left(\frac{g_m}{C}\right)^{-1} \sqrt[N]{N!\underbrace{\frac{V_{out}}{V_{in}}}_{A_{vN}}}$$

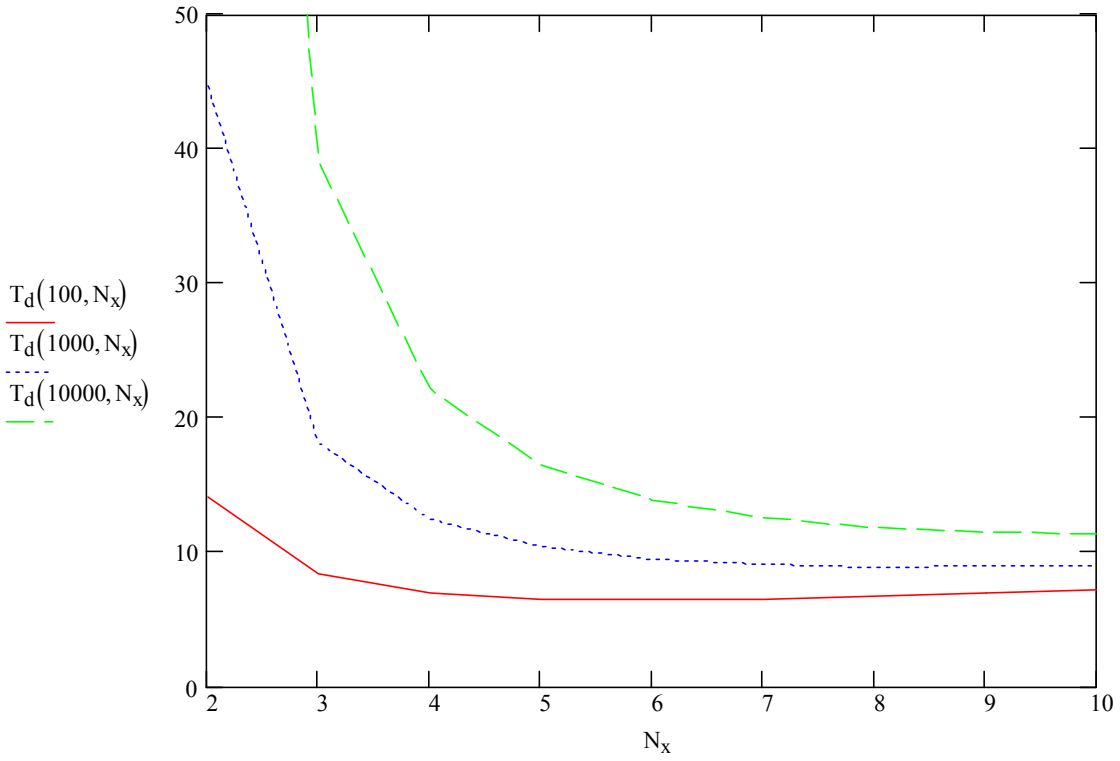
Gain versus Delay

$$v_o(N,t) := \frac{1}{N!} \cdot t^N$$



Optimum Number of Stages

$$T_d(A_{vN}, N) := \left[A_{vN} \cdot (N!)\right]^{\frac{1}{N}} \qquad N_x := 2 .. 10$$



Shallow minimum!

Optimum

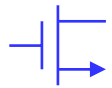
$$\frac{dT_d}{dN} = 0 \rightarrow$$

$$N_{opt} \cong 1.2 \ln A_{vN}$$

$$T_{d,opt} \cong 1.2\tau \ln A_{vN}$$

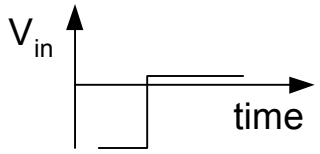
$$\text{optimum gain/stage}: \quad \sqrt{10} \cong 3.2$$

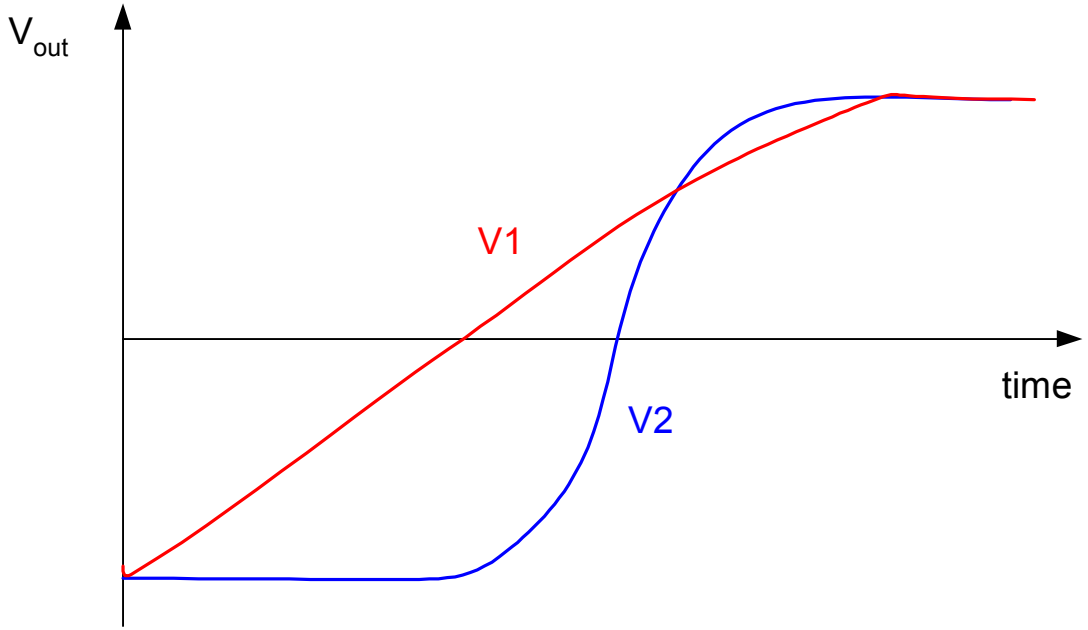
- Shallow optimum!
- In practice, limit to 4 … 6 gain stages (area, power, parasitics)
- Can get same speed with single latch … but higher offset



Practical Considerations

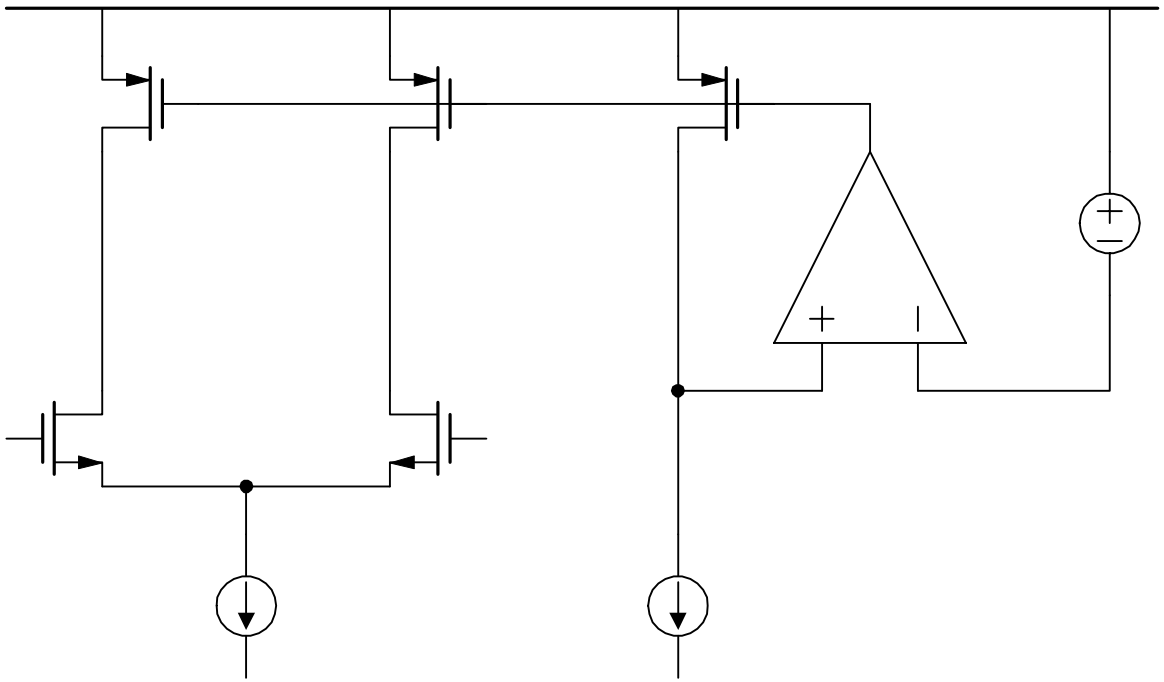
- Overload recovery:



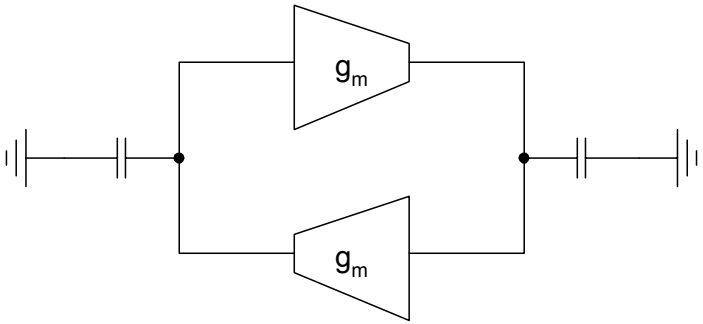


Solutions:
- Clamps
- Reset

Output Common-Mode



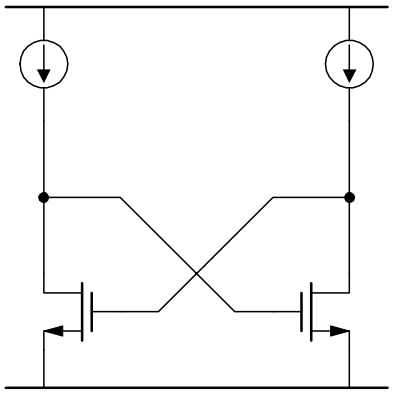
Latch



$t < 0$: initialize C to V_{id}

$t \geq 0$: positive feedback

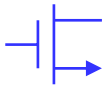
$$\frac{dv_1}{dt} = \frac{i_1(t)}{C} = \frac{g_m v_2(t)}{C}$$
$$\frac{dv_2}{dt} = \frac{i_2(t)}{C} = \frac{g_m v_1(t)}{C}$$



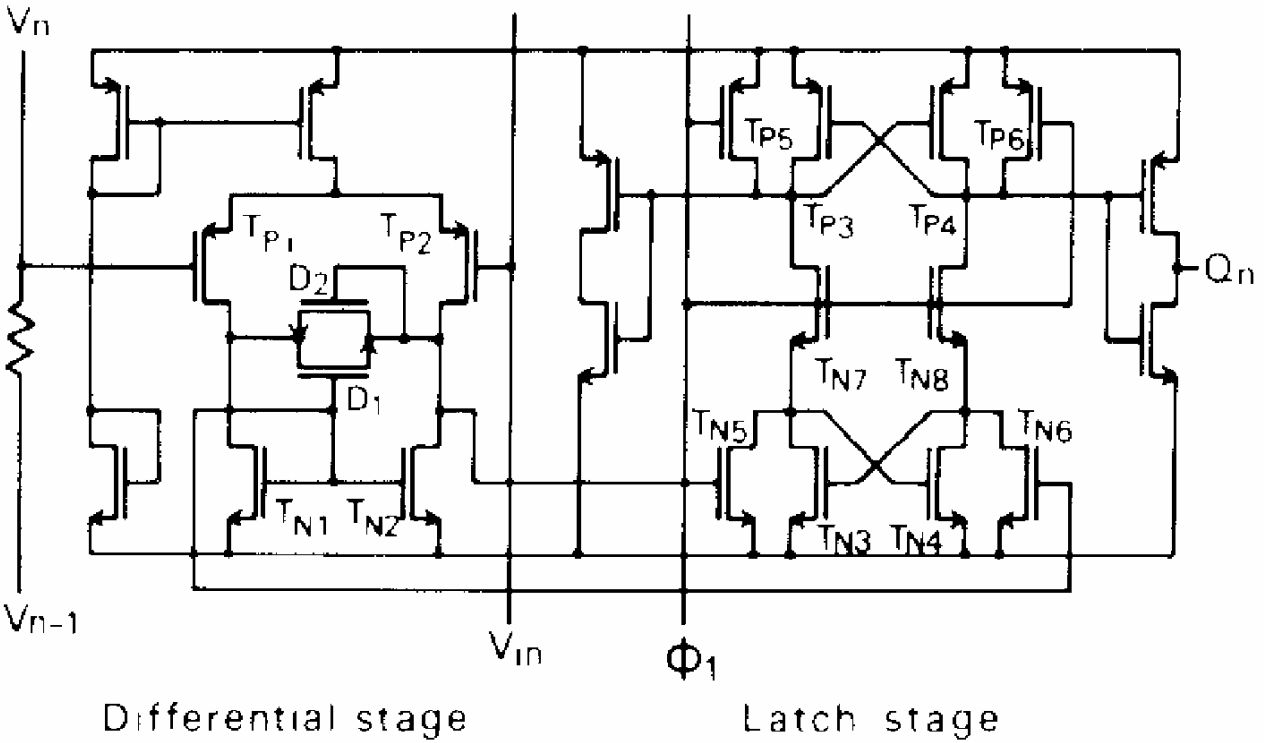
$$T_d = \frac{C}{g_m} \ln \frac{V_{od}}{V_{id}}$$
$$= \tau \ln A_v$$

compare: optimal cascade of amplifiers

$$T_{d,opt} \cong 1.2\tau \ln A_{vN}$$

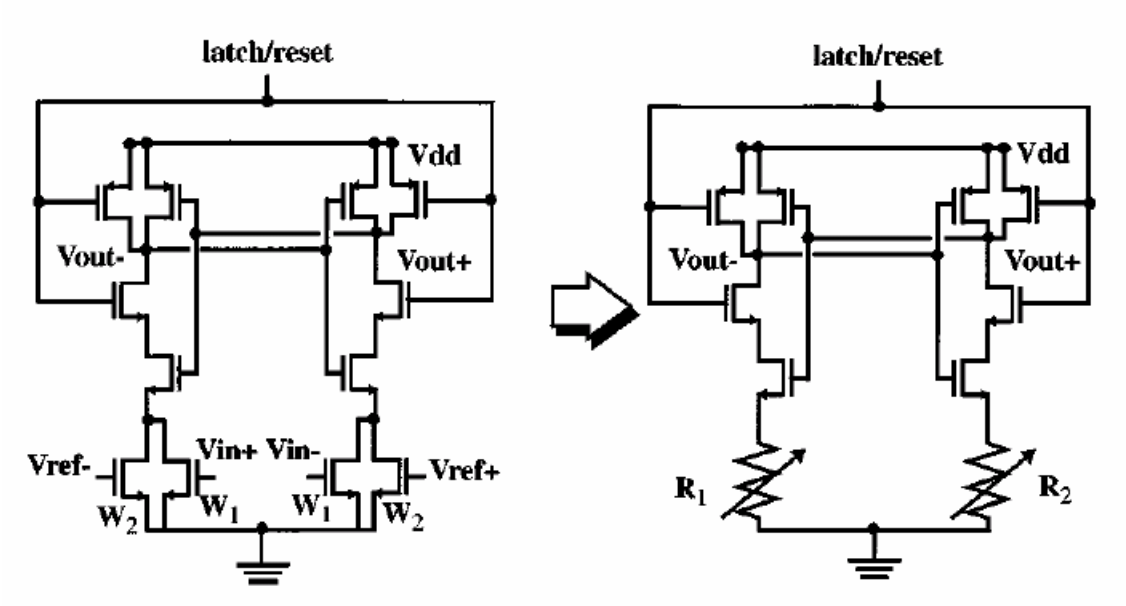


CMOS Comparator Example



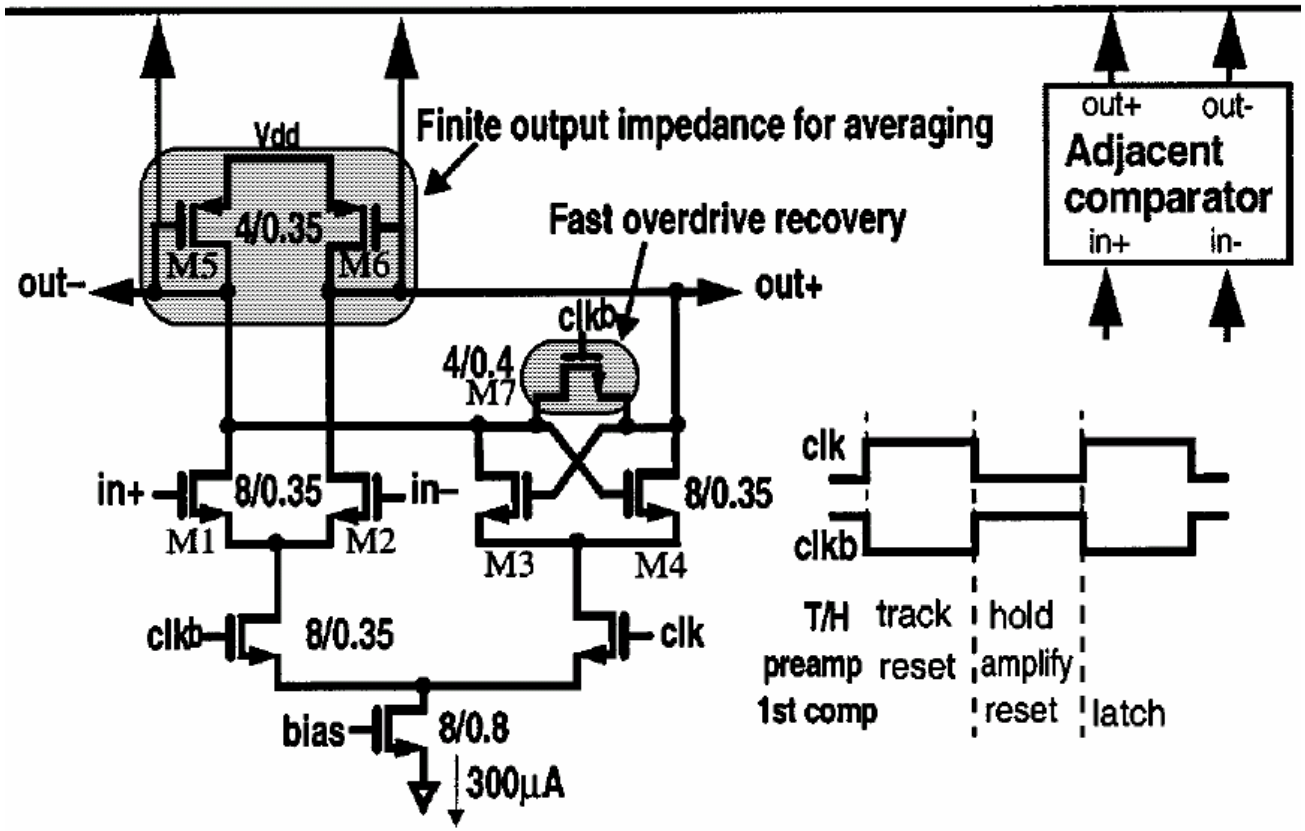
A. Yukawa, "A CMOS 8-Bit High-Speed A/D Converter IC," JSSC June 1985, pp. 775-9.

Dynamic Latch



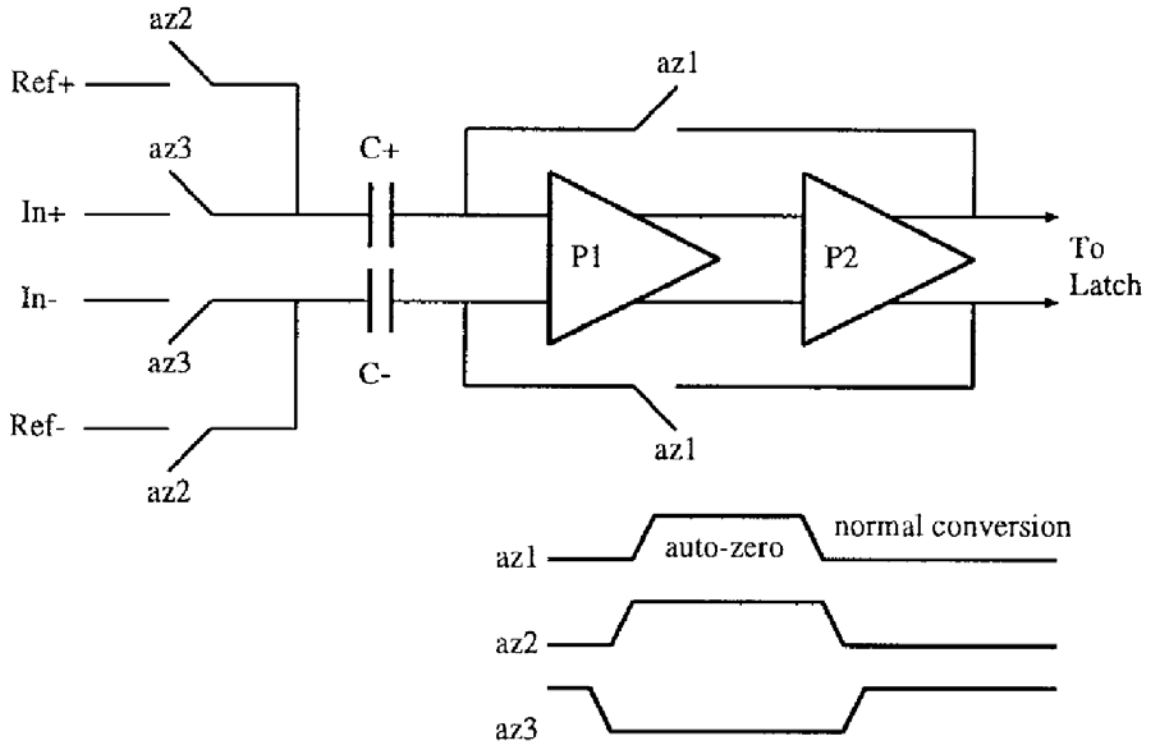
T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," *IEEE Journal of Solid-State Circuits,* vol. 30, pp. 166 - 172, March 1995.

Latch with Preamp



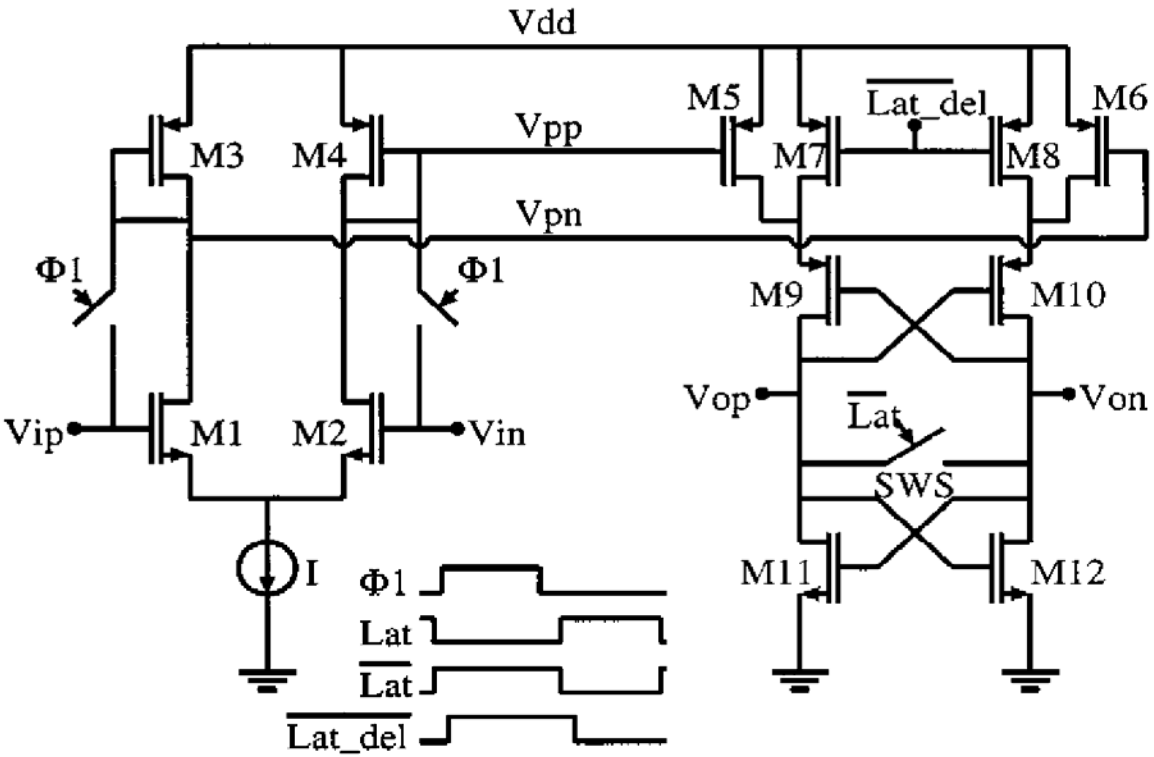
M. Choi and A. A. Abidi, "A 6-b 1.3-Gsample/s A/D converter in 0.35-µm CMOS," *IEEE Journal of Solid-State Circuits,* vol. 36, pp. 1847 - 1858, December 2001 and many others …

Comparator with Auto-Zero



I. Mehr and L. Singer, "A 500-Msample/s, 6-Bit Nyquist-Rate ADC for Disk-Drive Read-Channel Applications," JSSC July 1999, pp. 912-20.

Auto-Zero Implementation



I. Mehr and L. Singer, "A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC," JSSC March 2000, pp. 318-25.