

EECS 240

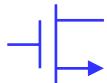
Analog Integrated Circuits

Lecture 8: References

Ali M. Niknejad and Bernhard E. Boser

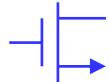
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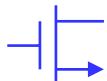
Outline

- Objectives
- CMOS implementations
- Startup circuits
- Typical performance
- Constant XXX references

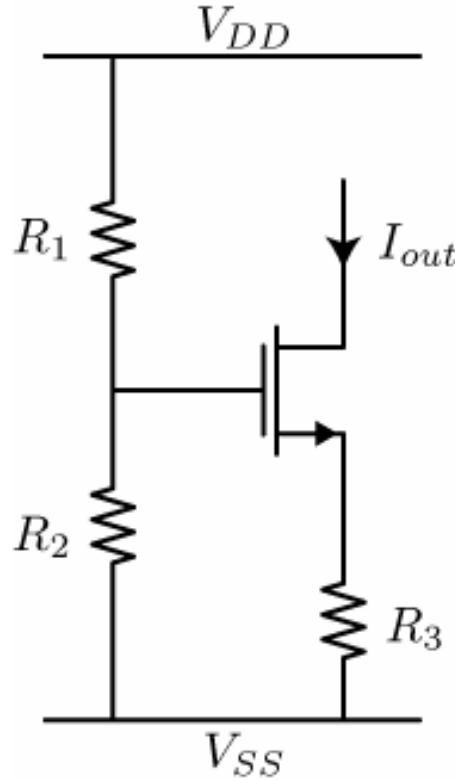


References

- Applications
 - Bias current
 - ADC / DAC references
- Solutions
 - Voltage references:
 - PTAT ($V_t = kT/q$)
 - Bandgap
 - Threshold voltage, V_{TH} , ΔV_{TH}
 - Special purpose:
 - Constant g_m
 - No “direct” current reference
- Specifications
 - Accuracy: σ of $\Delta V_{out}/V_{out}$
 - Temperature coefficient, TC_F
 - Power rejection ratio, PSRR
 - Trimming
 - Supply voltage
 - Power dissipation



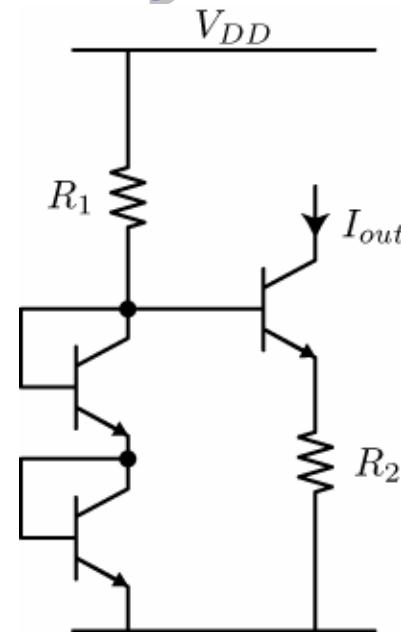
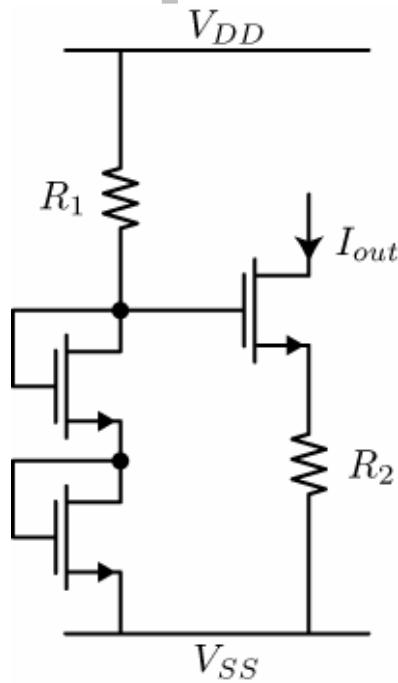
Supply Dependent Biasing



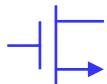
- Okay for test circuits, especially if resistors are off-chip. But output current is inaccurate and varies with supply/temperature.
- Realization of small (nA) currents requires big resistors (too much area).



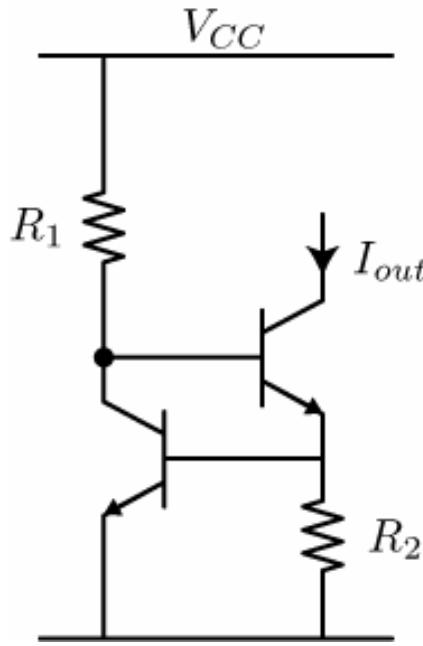
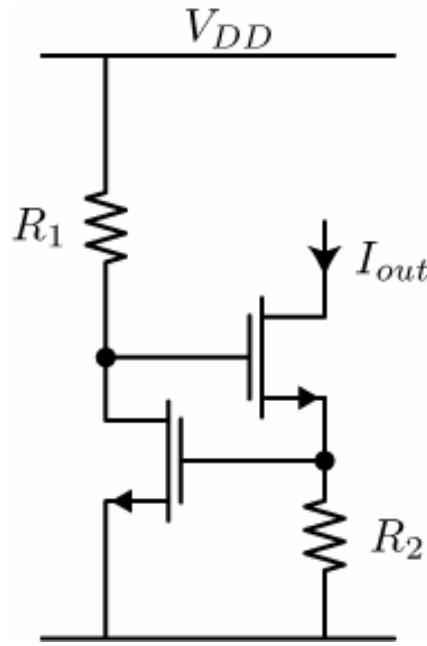
Simple Supply Rejection



- Use a V_{GS} or even better a V_{BE} as a reference. V_{BE} is very insensitive (logarithmically) to current variations.



Improved V_{GS}/V_{BE} Reference



- Now we have only one V_{BE} (V_{GS}) as the reference. If the overdrive of the MOS is small relative to V_T , this is a threshold reference.



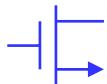
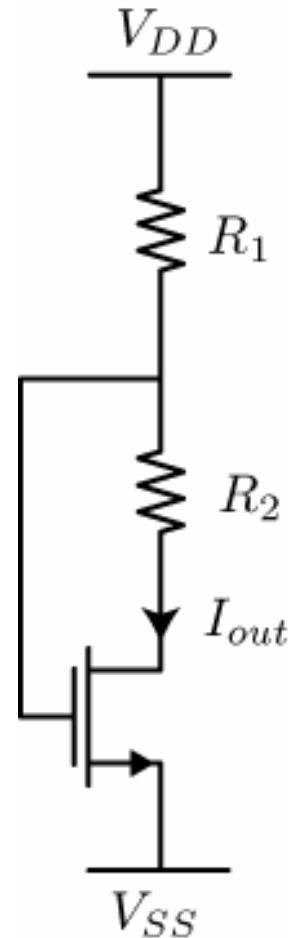
Peaking Current Source

$$V_o = V_{GS} - IR_2$$

$$\frac{dV_o}{dI} = \frac{dV_{GS}}{dI} - R_2$$

$$\frac{dV_o}{dI} = \frac{1}{g_m} - R_2 = 0 \quad R_2 = \frac{1}{g_m}$$

- Useful for very small (nA) current levels.
- Can compensate for variations in V_{GS} with a resistor to produce first order supply independent.

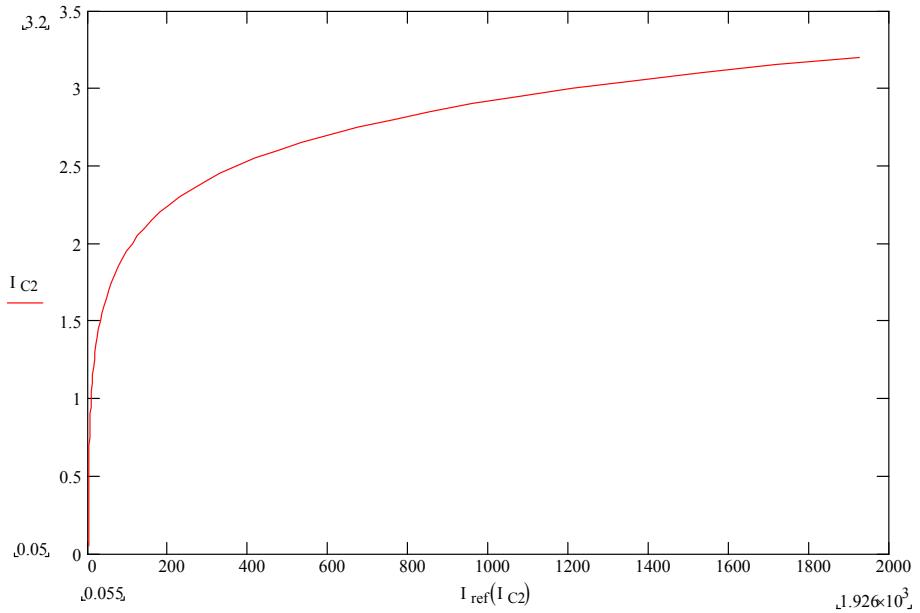
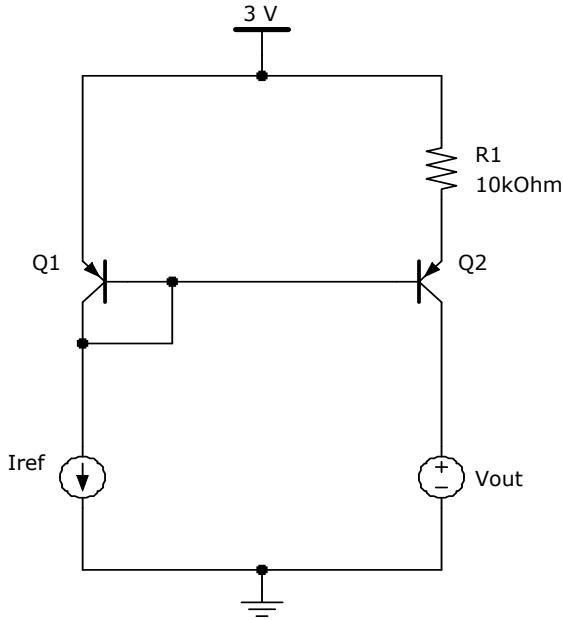


Widlar Reference

DC Analysis DC1

Device Iref

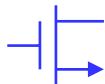
sweep from 0 to 300u (200 steps)



$$V_{BE1} = V_{BE2} + R_1 I_{C2}$$

$$V_t \ln\left(\frac{I_{ref}}{I_{s1}}\right) = V_t \ln\left(\frac{I_{C2}}{I_{s2}}\right) + R_1 I_{C2}$$

- I_{C2} is “relatively” insensitive to I_{ref}
- → first order supply independence

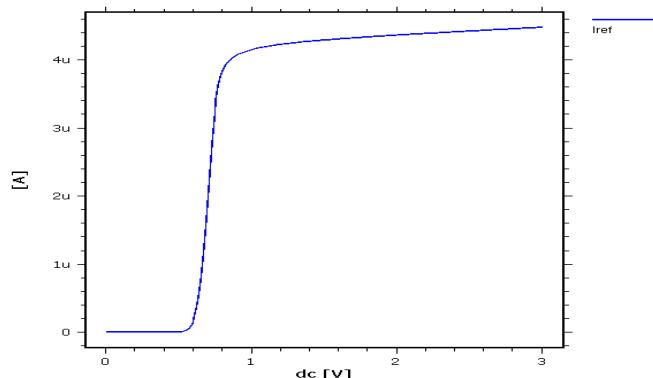
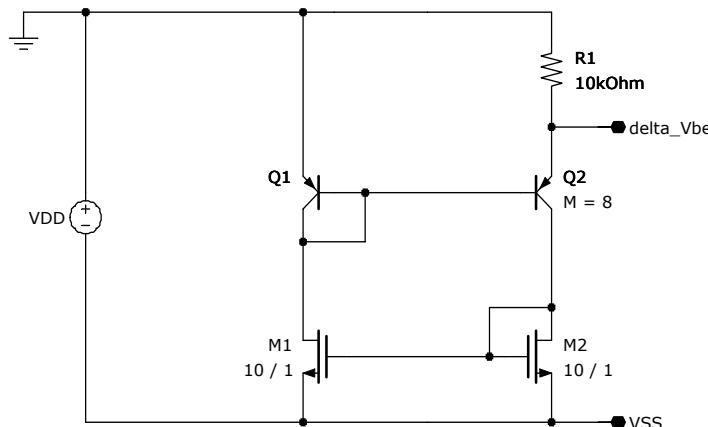


PTAT Reference

DC Analysis DC1

Device VDD

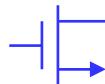
sweep from 10m to 3 (199 steps)



$$\begin{aligned}\Delta V_{BE} &= V_t \ln\left(\frac{I_{s2}}{I_{s1}} \frac{I_{C1}}{I_{C2}}\right) \\ &= V_t \ln\left(M \frac{I_{C1}}{I_{C2}}\right) \\ &\propto T\end{aligned}$$

Issues:

- Cascoding
- Self-biasing
- Temperature Coefficient
- Vertical BJT
- Startup



Temperature Coefficient

TC of Reference Voltage:

$$\begin{aligned} TC_F &= \frac{1}{\Delta V_{BE}} \frac{d\Delta V_{BE}}{dT} \\ &= \frac{1}{\Delta V_{BE}} \frac{\Delta V_{BE}}{T} \\ &= \frac{1}{T} \\ &\approx 3300 \text{ ppm/K} \quad \text{at room temperature (300°K)} \end{aligned}$$

TC of Reference Current:

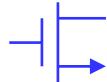
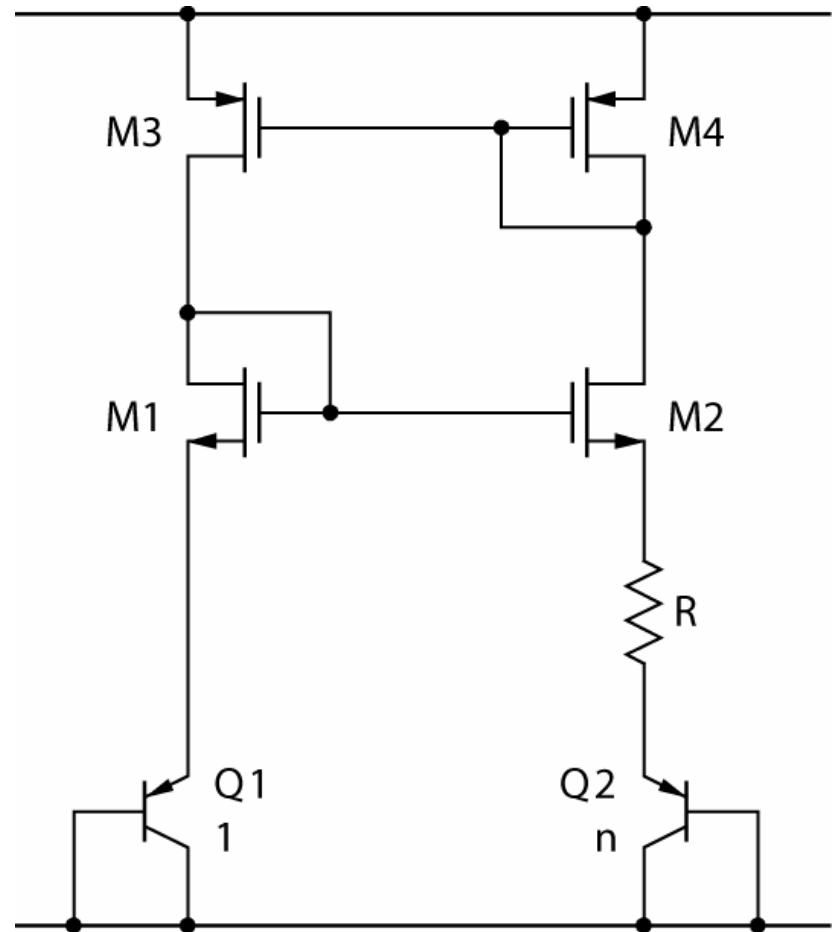
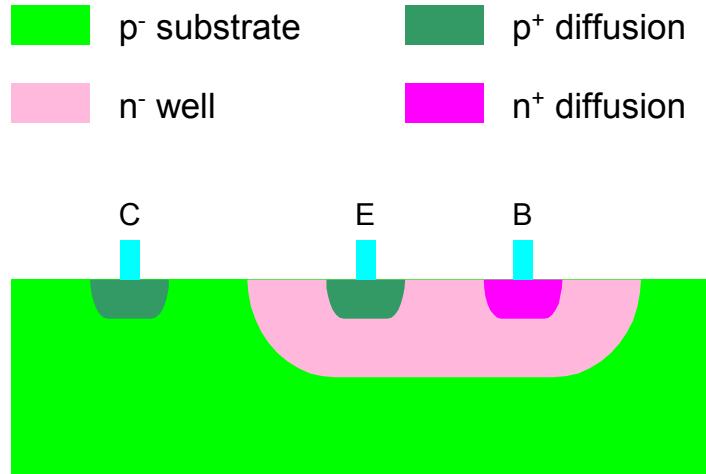
$$\begin{aligned} I_{out} &= \frac{\Delta V_{BE}}{R_1} \\ TC_F &= \frac{1}{I_{out}} \frac{dI_{out}}{dT} \\ &= \frac{1}{\Delta V_{BE}} \frac{d\Delta V_{BE}}{dT} - \frac{1}{R_1} \frac{dR_1}{dT} \\ &= 3300 \text{ ppm/K} - 1500 \text{ ppm/K} = 1800 \text{ ppm/K} \end{aligned}$$

for n+ diffusion resistor

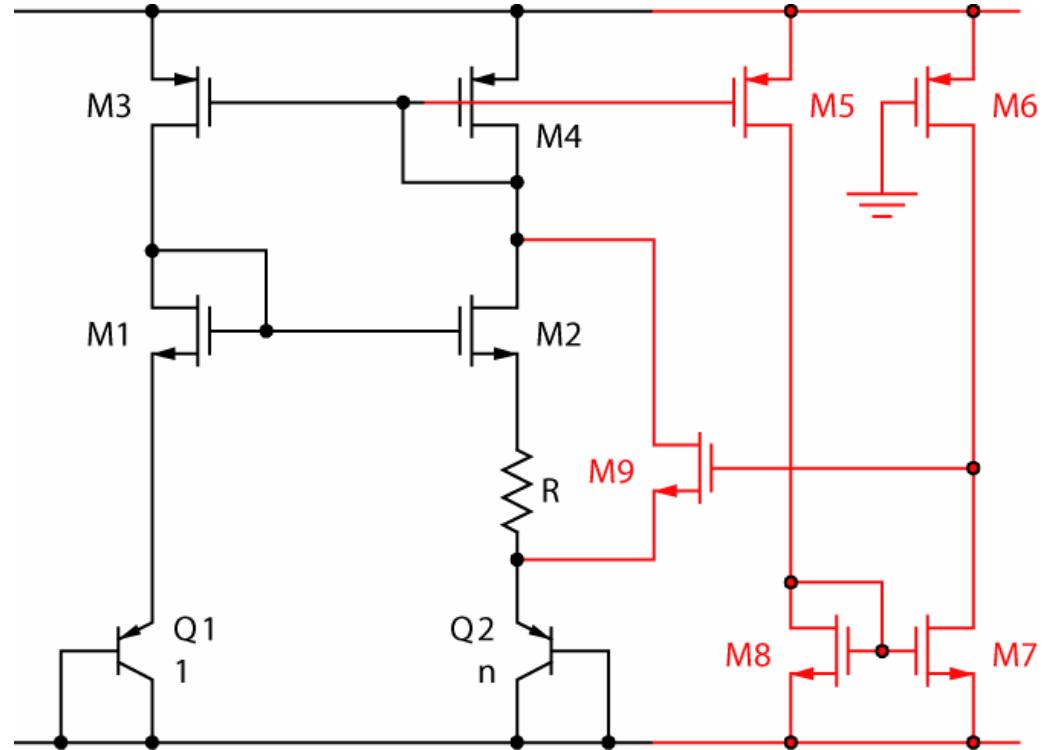
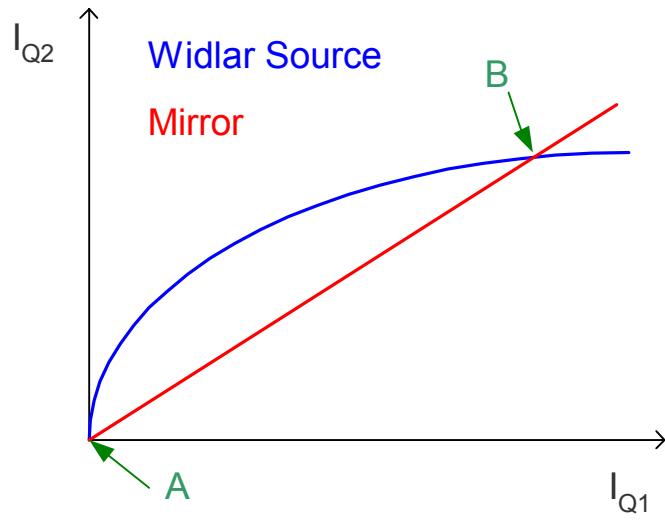


CMOS PTAT Reference

Vertical PNP

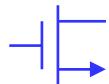


Startup Circuit



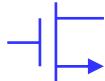
Parasitic operating point A:

- Positive feedback → unstable
- Noise drives circuit away from A (and to B)
- Problem: gain at A too small ($I_Q = 0$)

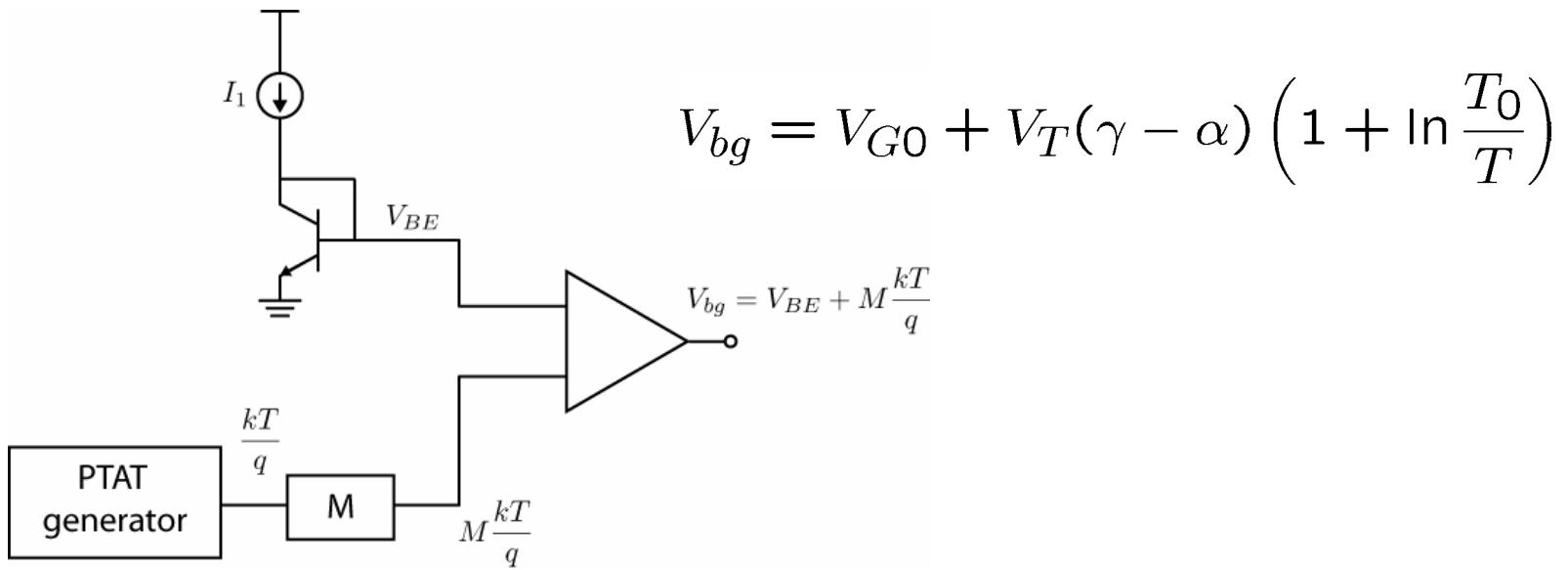


Bandgap Reference

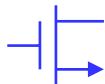
- Supply and temperature insensitive
- $V_{BG,Si} = 1.205V$
- Curvature correction
- References:
 - R. Widlar, JSSC 2/1971, pp. 2
first report
 - G. Nicollini, JSSC 1/1991, pp. 41
offset compensated amplifier
 - K. Tham, JSSC 5/1995, pp. 586
self-regulated supply for improved PSRR
 - A. Boni, JSSC 10/2002, pp. 1339
bandgap reference for $V_{DD} < V_{BG}$
 - P. Malcovati, JSSC 7/2001, pp. 1076
curvature corrected CMOS bandgap reference



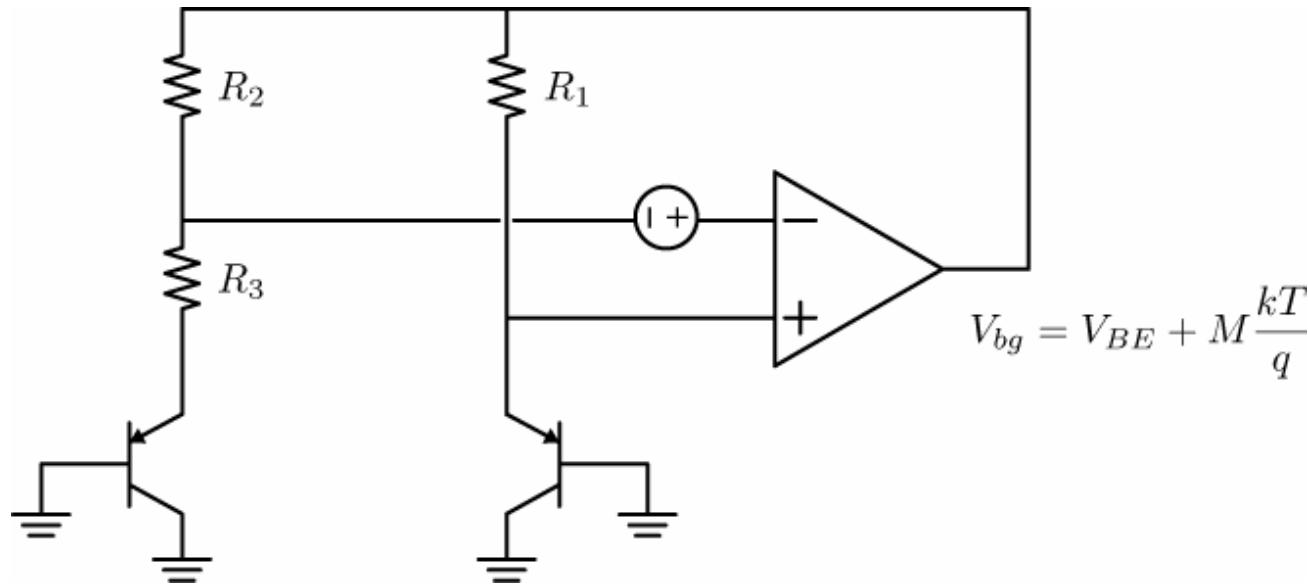
Hypothetical Band-Gap



- V_{BE} has a tempco of $-2 \text{ mV/}^\circ\text{C}$. If we add this to a multiple of the thermal voltage with positive tempco of $0.085 \text{ mV/}^\circ\text{C}$, we can achieve temperature independence.



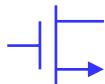
“CMOS” Bandgap



$$V_{R3} = V_{EB1} - V_{EB2} + V_{OS} = \Delta V_{EB} + V_{OS}$$

$$V_{R2} = \frac{R_2}{R_3} V_{R3} = \frac{R_2}{R_3} (\Delta V_{EB} + V_{OS})$$

$$V_{BG} = \left(1 + \frac{R_2}{R_3}\right) (\Delta V_{EB} + V_{OS}) + V_{EB2}$$

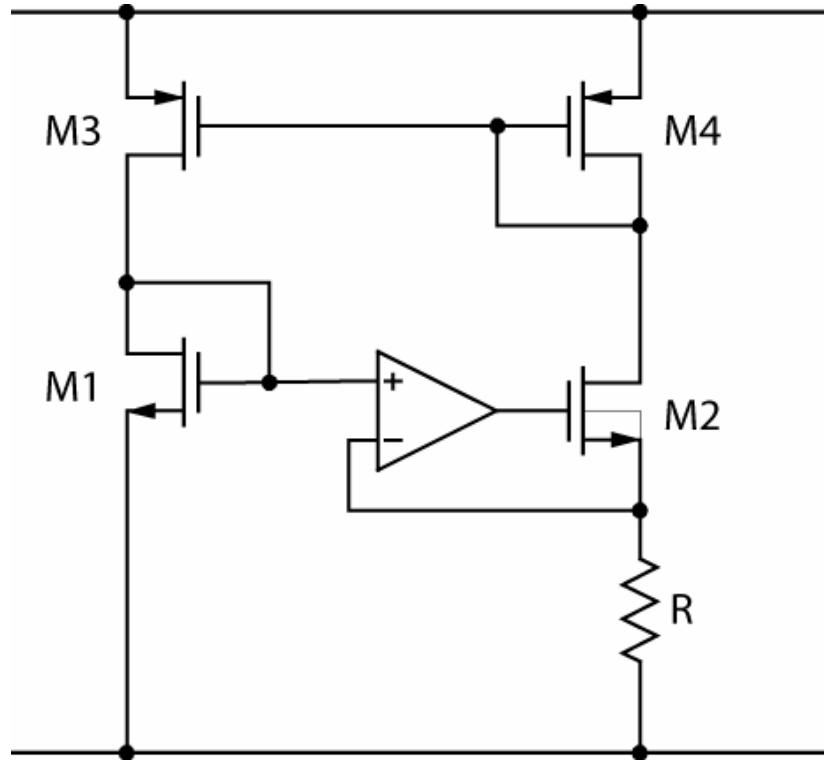


Bandgap Performance

	[Nicollini]	[Tham]	[Malcovati]
Supply	+/- 5V	3V	1V
Output voltage	6.2V	1.24V	0.54V
Accuracy (σ)	24mV	20mV	
TC _F	15ppm/°C	85ppm/°C	7.5ppm/°C
PSRR	86dB 40dB @ 500kHz	80dB @ 10kHz 40dB @ 500kHz	212ppm/V at DC
Power dissipation	4.8mW	1mW	92μW



Constant g_m Reference



$$\omega_u \propto \frac{g_m}{C_L}$$

$$g_{m1} = \frac{1}{R}$$



Reference Distribution

- Single shared reference
- Current distribution:
 - Many wires
 - Increase power dissipation
- Voltage distribution:
 - Susceptible to mismatch
 - → use large V_{GS} in distribution network
 - Careful supply routing to avoid poor PSRR
 - Avoid loops in analog supply

