EECS 240
Analog Integrated Circuits

Lecture 4: Small-Signal Models for Analog Design

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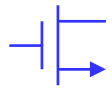
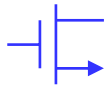


MOSFET Models for Design

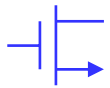
- SPICE (BSIM)
  - For verification
  - Device variations
- Hand analysis
  - Square law model
  - Small-signal model
- Challenge
  - Complexity / accuracy tradeoff
  - How can we accurately design when large signal models suitable for hand analysis are off by 50% and more?



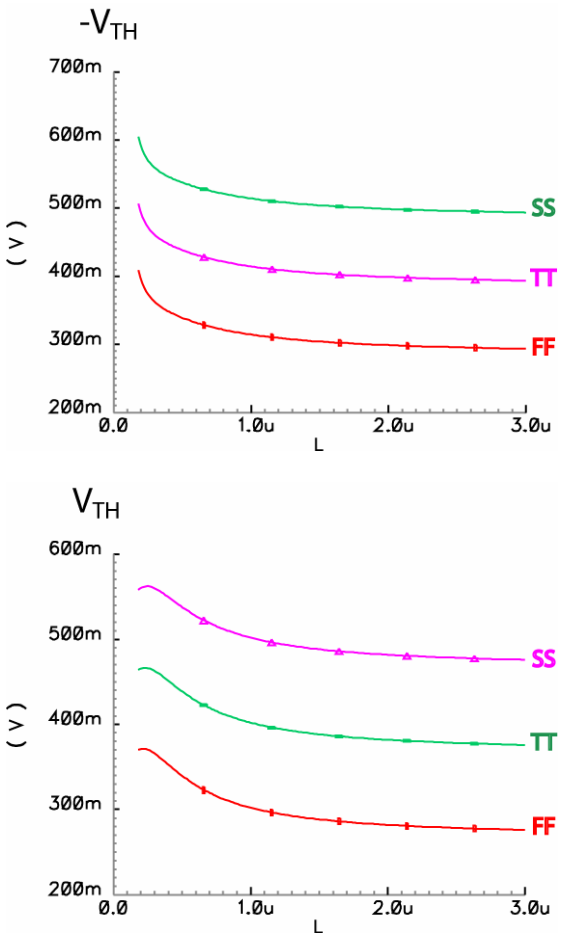
Device Variations

- Run-to-run parameter variations:
  - E.g. implant doses, layer thickness
  - Affect V_{TH}, μ, C_{ox}, $R_{\square}$, …
  - How model in SPICE?

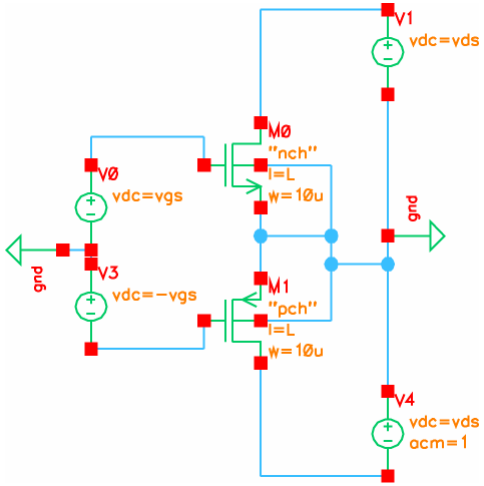
- Nominal / slow / fast parameters
  - E.g. fast: low V_{TH}, high μ, high C_{ox}, low $R_{\square}$
  - Combine with supply extremes
  - Pessimistic but numerically tractable
    → improves chances for working Silicon



Threshold Voltage V_{TH}



- Strong function of L
- Use long channel for V_{TH} matching
- Process variations
  - Run-to-run
  - How characterize?
  - Slow/nominal/fast
  - Both worst-case & optimistic



V_{TH} Design Considerations

- Approximate Values (L = 0.5μm)

  V_{THN} = 600mV γ_n=0.5 rt-V

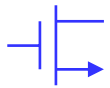
  V_{THP} = -700mV γ_p=0.4 rt-V

- Back-Gate Bias

$$V_T = V_{T0} + \gamma\left(\sqrt{\psi_0 + V_{SB}} - \sqrt{\phi_0}\right) \qquad \phi_0 \approx 2\phi_F$$

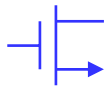
  e.g. V_{SB} = 400mV → ΔV_{THN} = 110mV

- Variations:
  - Run-to-run: +/- 50mV (very process dependent)
  - Device-to-device: σ = 2mV (L > 1μm, common-centroid)
  - Use insensitive designs
    - diff pairs, current mirrors
    - → value of V_{TH} unimportant (if < V_{DD})



Device Parameters for Design

- Region: moderate or strong inversion / saturation
  - Most common region of operation in analog circuits
  - XTR behaves like transconductor: voltage controlled current source
- Key design parameters
  - Large signal
    - Current I_D → power dissipation
    - Minimum V_{DS} → available signal swing
  - Small signal
    - Transconductance g_m → speed / voltage gain
    - Capacitances C_{GS}, C_{GD}, … → speed
    - Output impedance r_o → voltage gain



Low Frequency Model

- A Taylor series expansion of small signal current gives (neglect higher order derivatives)

$$i_{ds} = \frac{\partial I_{ds}}{\partial V_{gs}} v_{gs} + \frac{\partial I_{ds}}{\partial V_{bs}} v_{bs} + \frac{\partial I_{ds}}{\partial V_{ds}} v_{ds}$$

$$i_{ds} = g_m V_{gs} + g_{mb} V_{bs} + g_{ds} V_{ds}$$

- Square law model:

$$g_{m,triode} = \mu C_{ox} \frac{W}{L} \frac{V_{ds}}{\alpha} \qquad g_m = \mu C_{ox} \frac{W}{L} \frac{(V_{gs} - V_T)}{\alpha}$$

$$g_{ds} = \frac{1}{r_o} = \lambda I_{ds}$$

Transconductance

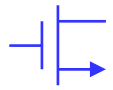
- Using the square law model we have three equivalent forms for g_m in saturation

$$g_m = \mu C_{ox} \frac{W}{L} \sqrt{\frac{2I_{ds}}{\mu C_{ox} \frac{W}{L}}}$$

$$g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_{ds}} \propto \sqrt{I_{ds}}$$

$$g_m = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{gs} - V_T)^2 \frac{1}{\frac{1}{2}(V_{gs} - V_T)}$$

$$g_m = \frac{2I_{ds}}{V_{gs} - V_T} = \frac{2I_{ds}}{V_{dsat}}$$



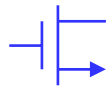
Weak Invesion g_m

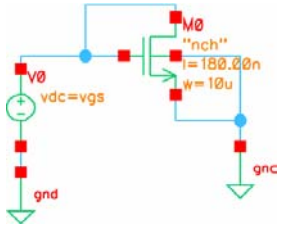
- In weak inversion we have bipolar behavior

$$I_{ds} \approx \frac{W}{L} I_{ds,0} e^{\frac{q(V_{gs}-V_T)}{nkT}}$$

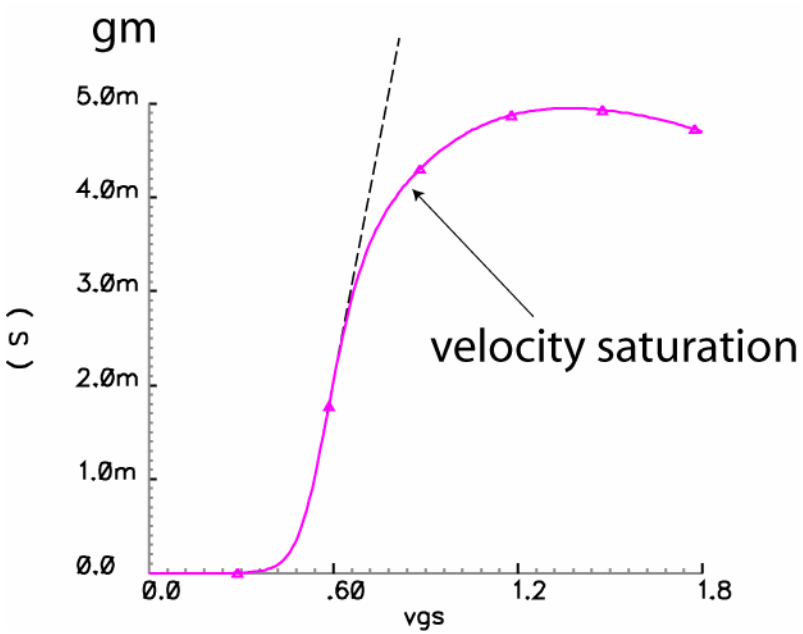
$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{\frac{W}{L} I_{ds,0} e^{\frac{q(V_{gs}-V_T)}{nkT}}}{n\frac{kT}{q}}$$

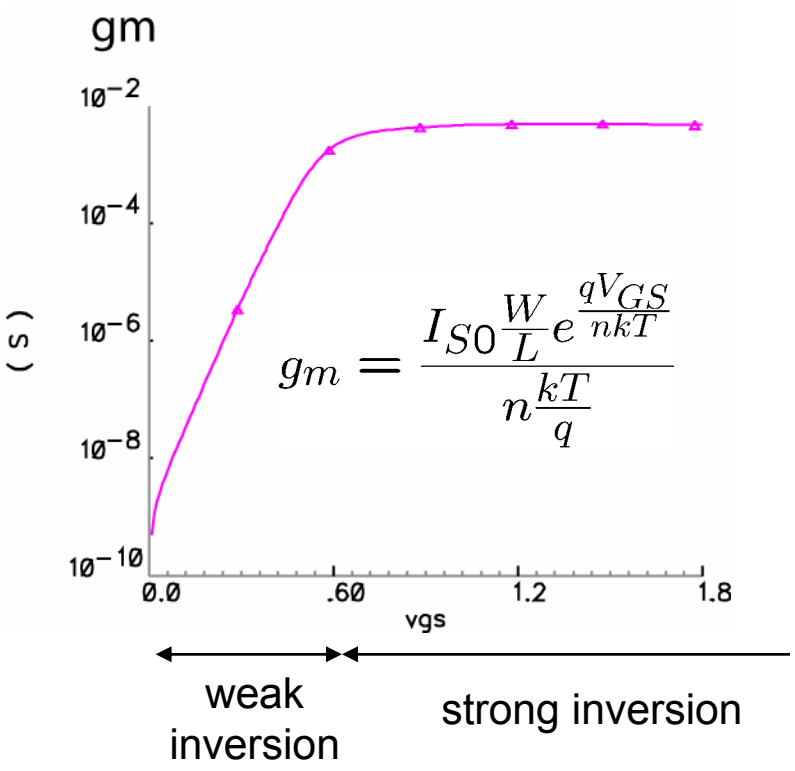
$$g_m = \frac{I_{DS}}{n\frac{kT}{q}} \propto I_{DS}$$



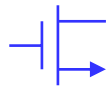


Transconductance





$$g_{m(sat)} \approx \mu C_{ox}\frac{W}{L}(V_{GS} - V_T)$$

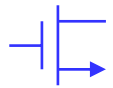


Transconductance (cont)

- The transconductance increases linearly with $V_{gs} - V_T$ but only as the square root of I_{ds}. Compare this to a BJT that has transconductance proportional to current.
- In fact, we have very similar forms for g_m

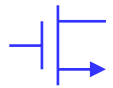
$$g_m^{\text{FET}} = \frac{2I_{ds}}{V_{dsat}} \qquad g_m^{\text{BJT}} = \frac{I_C}{V_t}$$

- Since $V_{dsat} >> V_t$, the BJT has larger transconductance for equal current.
- Why can't we make $V_{dsat} \sim V_t$?

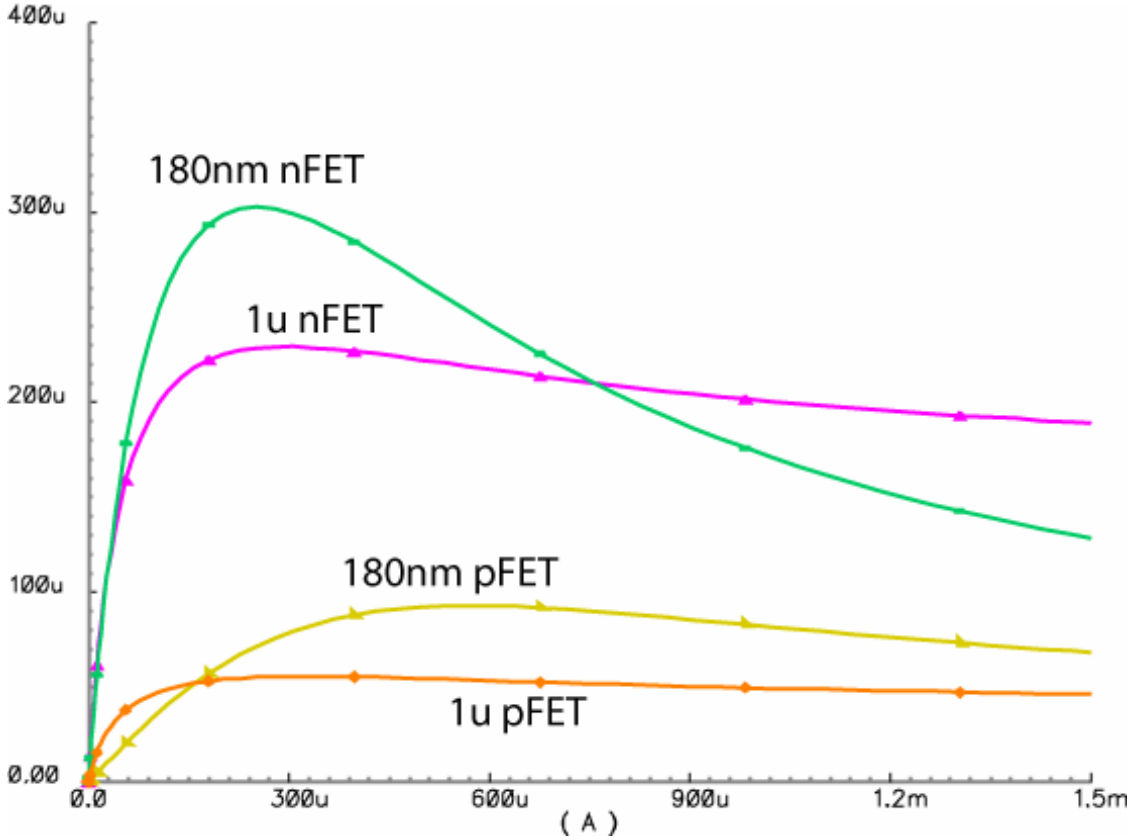


Subthreshold Again…

- In fact, we can make $V_{gs} - V_t$ very small and operate in the sub-threshold region. Then the transconductance is the same as a BJT (except the non-ideality n factor).
- But as we shall see, the transistor f_T drops dramatically if we operate in this region. Thus we typically prefer moderate or strong inversion for high-speed applications.



μC_{ox}



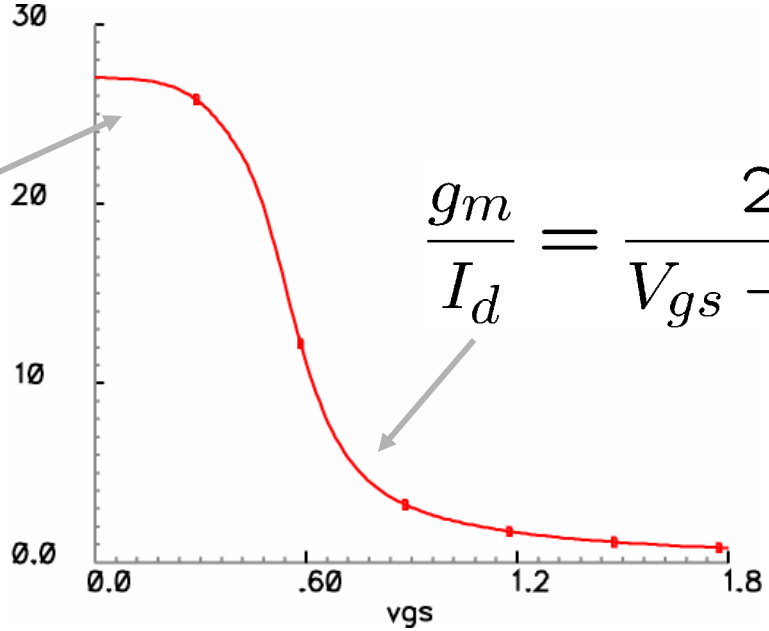
- Square law:

$$\mu C_{ox} = \frac{g_m^2}{2\frac{W}{L} I_D}$$

- Extracted values strong function of I_D
  - Low I_D → weak inversion
  - Large I_D → mobility reduction
- Do not use μC_{ox} for design!

Transconductor Efficiency

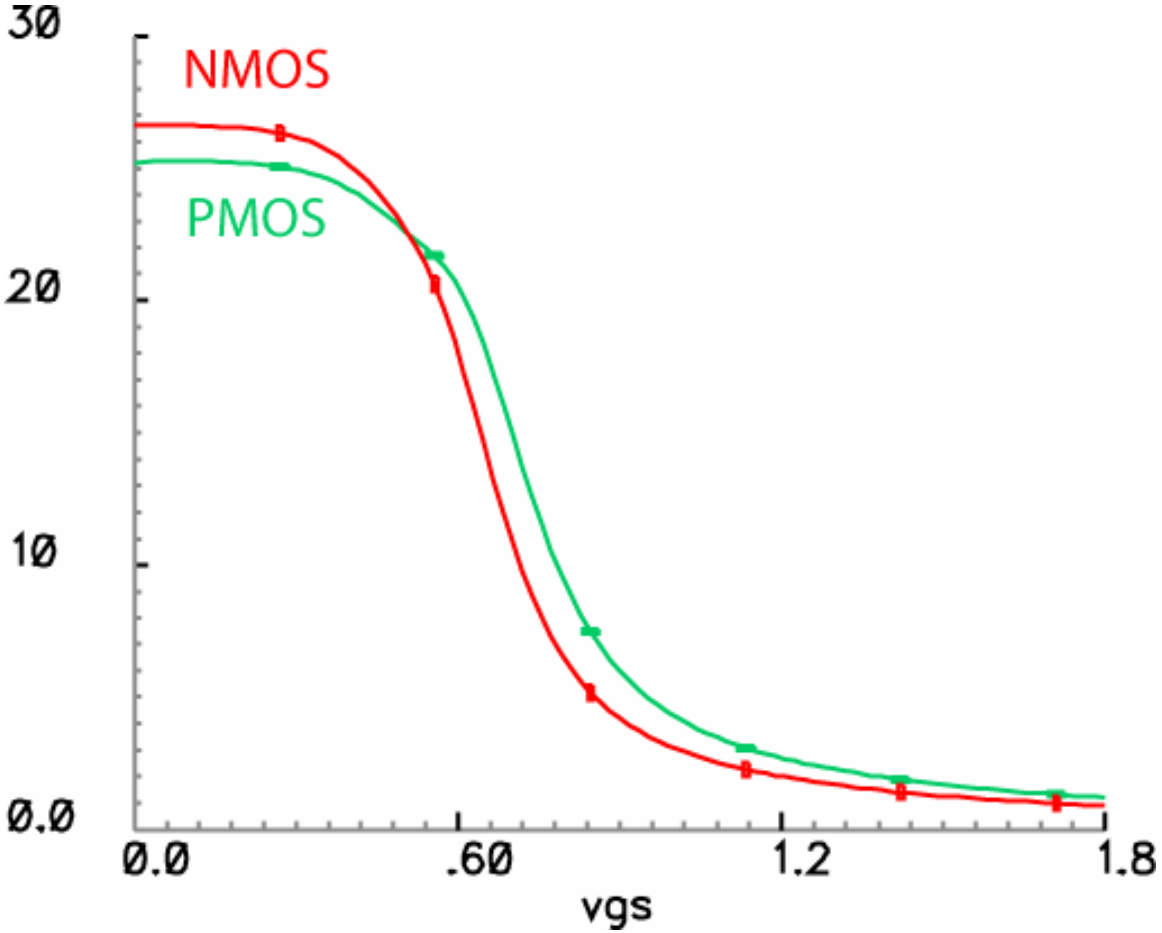
$$\frac{g_m}{I_d} = \frac{1}{n\frac{kT}{q}}$$



$$\frac{g_m}{I_d} = \frac{2}{V_{gs} - V_T} = \frac{2}{V_{dsat}}$$

- A good metric for a transistor is the transconductance normalized to the DC current. Since the power dissipation is determined by and large by the DC current, we'd like to get the most "bang" for the "buck".
- From this perspective, the weak and moderate inversion region is the optimal place to operate.

Efficiency g_m/I_D



- High efficiency is good for low power
- Higher g_m/I_D at low V_{GS}
- Approaches BJT for $V_{GS} < V_{TH}$

  $g_m/I_C = 1/V_t \sim 40\ V^{-1}$
- NMOS / PMOS about same

Efficiency g_m/I_D

- Let's define

$$V^* = \frac{2I_D}{g_m} \quad \Leftrightarrow \quad \frac{g_m}{I_D} = \frac{2}{V^*}$$

e.g. V* = 200mV → $g_m/I_D = 10\ V^{-1}$

- Square-law devices: $V^* = V_{GS}-V_{TH} = V_{dsat}$

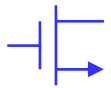
Square law : $$g_m = \frac{2I_D}{V_{GS}-V_{TH}} = \frac{2I_D}{V^*}$$

SPICE Charge Model

- Charge conservation

- MOSFET:
  - 4 terminals: S, G, D, B
  - 4 charges: $Q_S + Q_G + Q_D + Q_B = 0$ (3 free variables)
  - 3 independent voltages: V_{GS}, V_{DS}, V_{SB}
  - 9 derivatives: $C_{ij} = dQ_i / dV_j$, e.g. $C_{G,GS} \sim C_{GS}$
  - C_{ij} != C_{ji}

Ref: HSPICE manual, "Introduction to Transcapacitance", pp. 15:42, Metasoft, 1996.



Small Signal Capacitances

	Weak inversion	Strong inversion linear	Strong inversion saturation
C_{GS}	C_{ol}	$C_{GC}/2 + C_{ol}$	$2/3\ C_{GC} + C_{ol}$
C_{GD}	C_{ol}	$C_{GC}/2 + C_{ol}$	C_{ol}
C_{GB}	C_{GC} // C_{CB}	0	0
C_{SB}	C_{jSB}	$C_{jsB} + C_{CB}/2$	$C_{jsB} + 2/3\ C_{CB}$
C_{DB}	C_{jDB}	$C_{jDB} + C_{CB}/2$	C_{jDB}

$$C_{GC} = C_{ox}WL$$

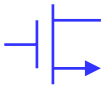
$$C_{CB} = \frac{\varepsilon_{Si}}{x_d}WL$$

0.35u Process

$$C_{ox} = 5.3\ \text{fF}/\mu\text{m}^2$$

$$C_{olN} = 0.24\ \text{fF}/\mu\text{m}$$

$$C_{olP} = 0.48\ \text{fF}/\mu\text{m}$$



MOS Capacitance Example

$$\frac{W}{L} = \frac{100}{0.5}$$

$$C_{ox} = \varepsilon_o \frac{\varepsilon_{SiO_2}}{t_{ox}} = 5.3 \frac{\text{fF}}{\mu\text{m}^2}$$

$$C_{gc} = C_{ox} WL = 265\text{fF}$$

$$C_{ol} = C_{olN} W = 24\text{fF}$$

subthreshold :

$$C_{gs} = C_{ol} = 24\text{fF}$$

$$C_{gd} = C_{ol} = 24\text{fF}$$

triode :

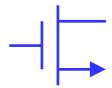
$$C_{gs} = \tfrac{1}{2} C_{gc} + C_{ol} = 157\text{fF}$$

$$C_{gd} = \tfrac{1}{2} C_{gc} + C_{ol} = 157\text{fF}$$

saturation :

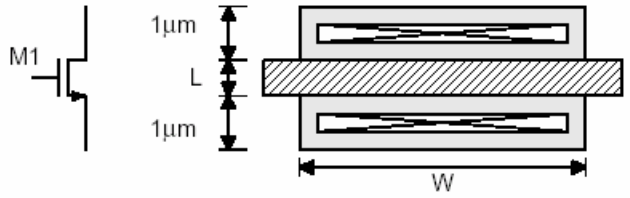
$$C_{gs} = \tfrac{2}{3} C_{gc} + C_{ol} = 201\text{fF}$$

$$C_{gd} = C_{ol} = 24\text{fF}$$



Layout

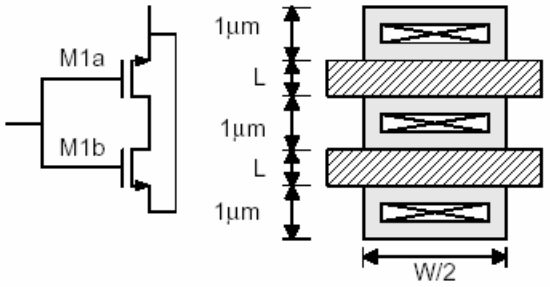
Individual devices:



AS = AD =1µm * W
PS = PD = 2µm + W
e.g. NMOS, W=20µm, V_{sb}=0V
$C_{sb} = C_{db}$ = 28fF

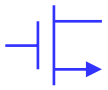
HSPICE geo = 0 (default)

Wide devices consisting of multiple individual ones wired in parallel:



AS = 1µm * W
PS = 4µm + W
AD = 1µm * W/2
PD = 2µm
e.g. NMOS, W=20µm, V_{sb}=0V
C_{sb} = 29fF
C_{db} = 10fF

HSPICE geo = 3



Extrinsic MOS Capacitances

- Source/drain diffusion junction capacitance:

$$C_j(V) \cong \frac{C_{j0}}{\left(1+\frac{V}{V_b}\right)^m} \quad \text{and} \quad C_{jsw}(V) \cong \frac{C_{jsw0}}{\left(1+\frac{V}{V_b}\right)^m}$$

$$C_{bc0} = \frac{\varepsilon_{Si}\varepsilon_0}{x_{j0}} \quad \text{with} \quad x_{j0} = \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0}{q_e N_{sub}}|\Phi_{bi}|}$$

$C_{jn0} = 0.85\frac{\text{fF}}{\mu\text{m}^2}$	$C_{jn0} = 1.1\frac{\text{fF}}{\mu\text{m}^2}$
$C_{jswn0} = 0.49\frac{\text{fF}}{\mu\text{m}^2}$	$C_{jswn0} = 0.48\frac{\text{fF}}{\mu\text{m}^2}$
$V_{bn} = 0.51\text{V}$	$V_{bn} = 0.93\text{V}$
$m_n = 0.39$	$m_n = 0.48$

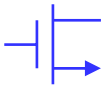
- Example: W/L = 100/0.5, $V_{SB} = V_{DB} = 0$V, $L_{diff} = 1\mu$m

AS = AD = 100μm^2, PS = PD = 102μm

C_{jn} = 85fF C_{jswn} = 50fF C_{bc} = 58fF

Strong Inversion –

Saturation:	C_{sb} = 173fF	C_{db} = 135fF
Linear region:	C_{sb} = 164fF	C_{db} = 164fF



High Frequency Figures of Merit

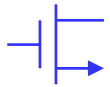
- Unity current-gain bandwidth

$$\omega_T = \frac{g_m}{C_{gs} + C_{gd}}$$

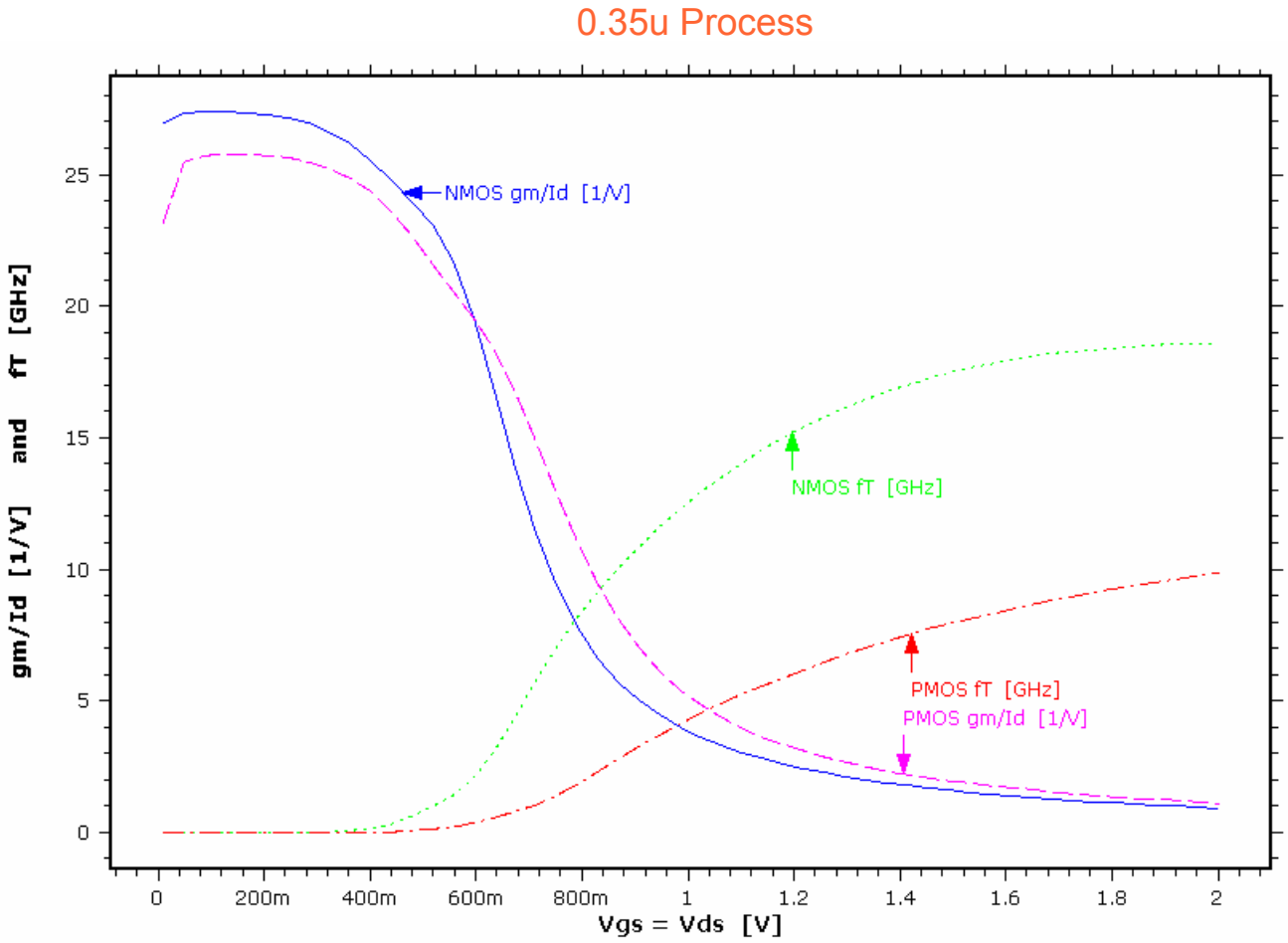
$$\omega_T = \frac{3}{2}\frac{\mu V_{dsat}}{L^2} = \frac{3}{2}\omega_0 \qquad \text{(Long channel model)}$$

- This is related to the channel transit time: $\tau_0 = 1/\omega_0$
- For degenerate short channel device

$$\omega_T = \frac{3}{2}\frac{\nu_{sat}}{L} = \frac{3}{2}\frac{1}{\tau_{sat}}$$



Efficiency g_m/I_D versus f_T



Speed-Efficiency Tradeoff

NMOS faster than PMOS

Weak Inversion Frequency Response

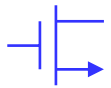
- The gate capacitance in weak inversion is given by

$$C_{gb} = C_{ox}\frac{\gamma}{2\sqrt{\gamma^2/4 + V_{GB} - V_{FB}}}$$

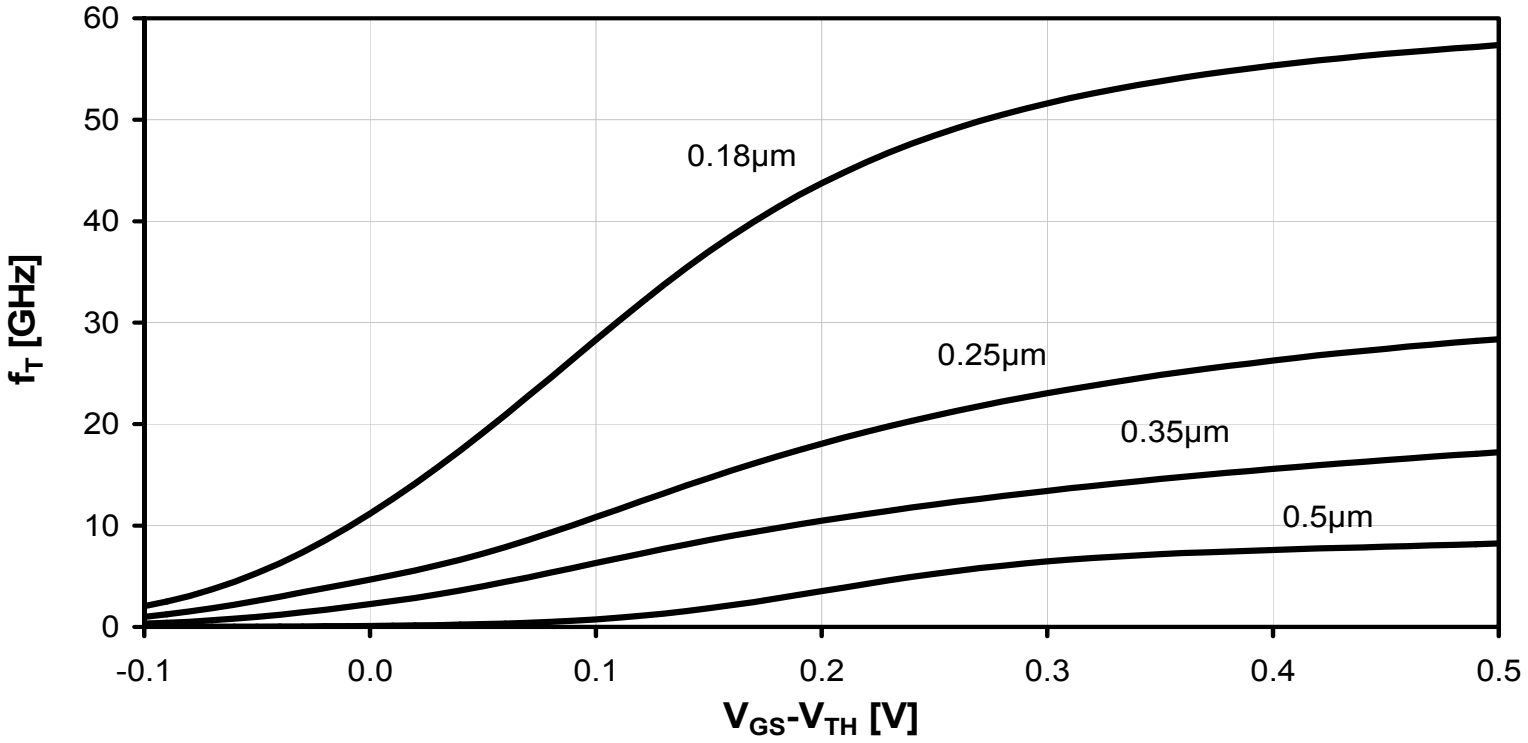
$$\omega_T = \frac{\mu\frac{kT}{q}}{L^2}\left(\frac{I_{DS}}{I_M}\right)$$

- I_M is the maximum achievable current in weak inversion so the factor ( ) < 1

Ref: Tsividis, *Operation and Modeling of the MOS Transistor*

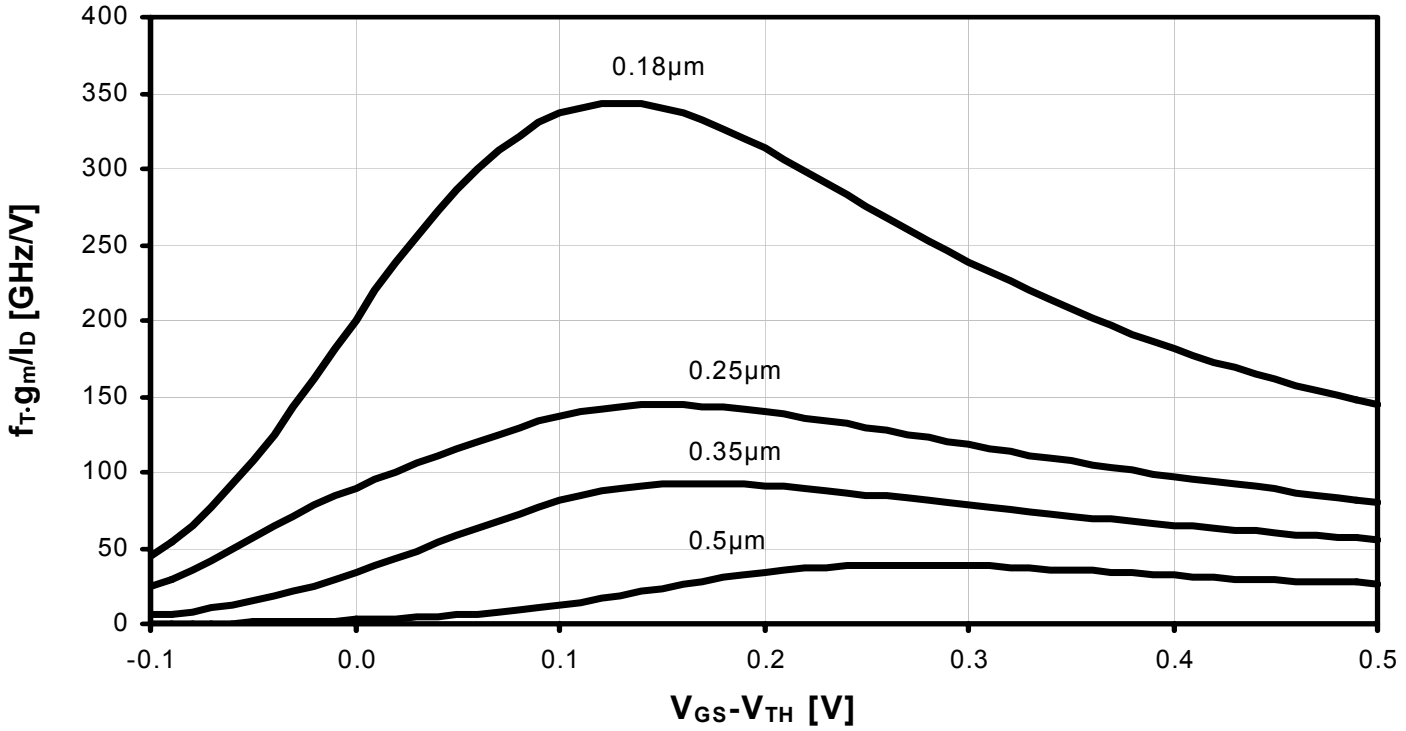


Device Scaling



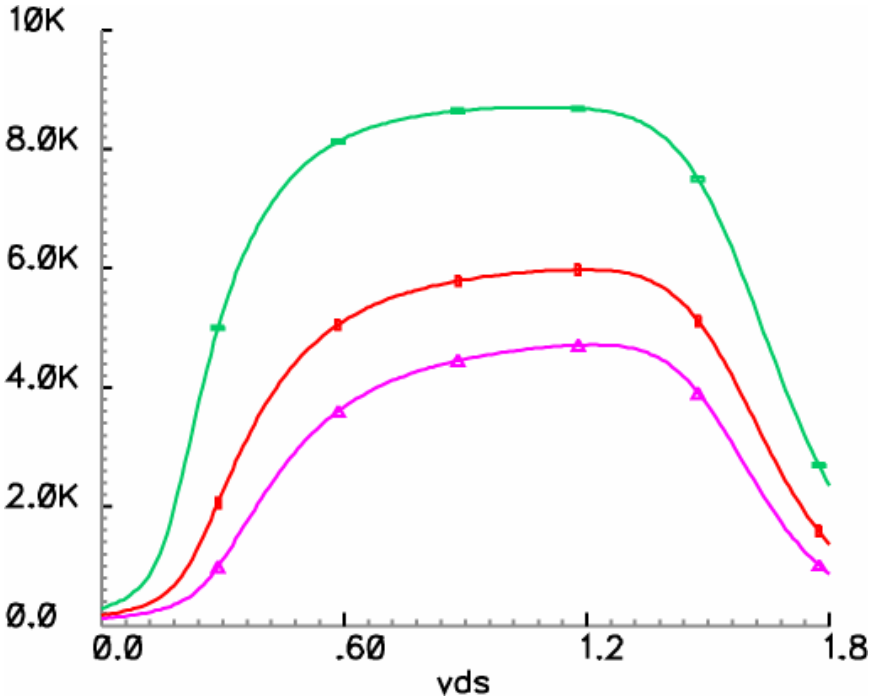
Short channel devices are significantly faster!

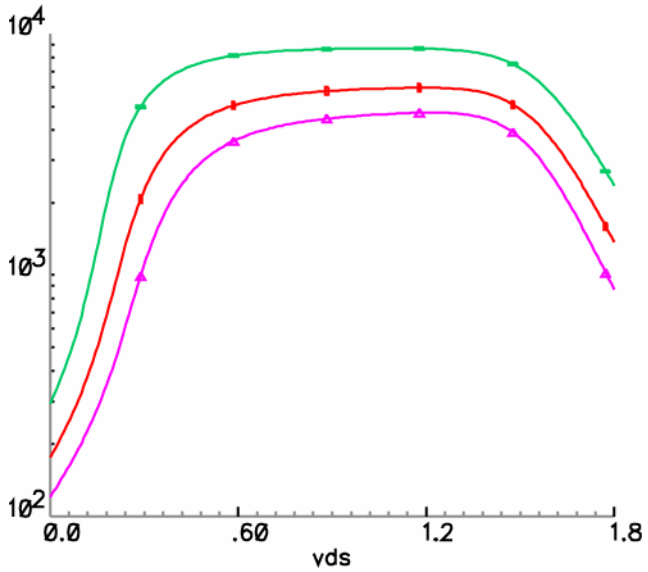
Device Figure-of-Merit



Peak performance for low $V_{GS}-V_{TH}$ (V*)

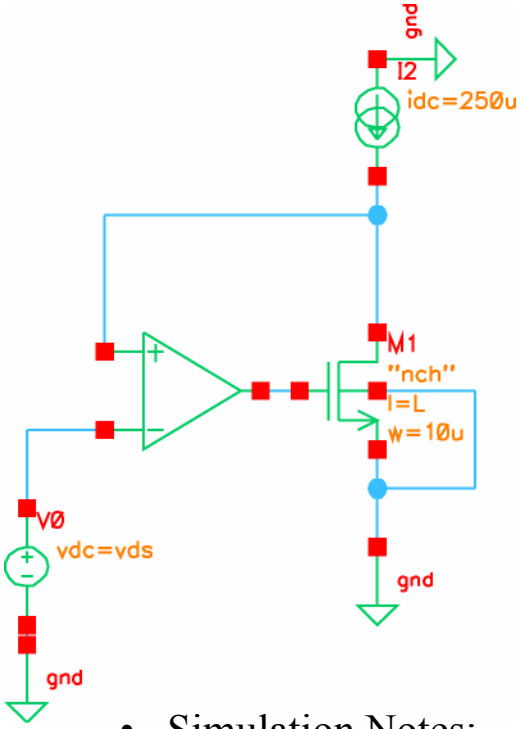
Output Resistance r_o





Hopeless to model this with a simple equation
(e.g. $g_{ds} = \lambda I_D$)

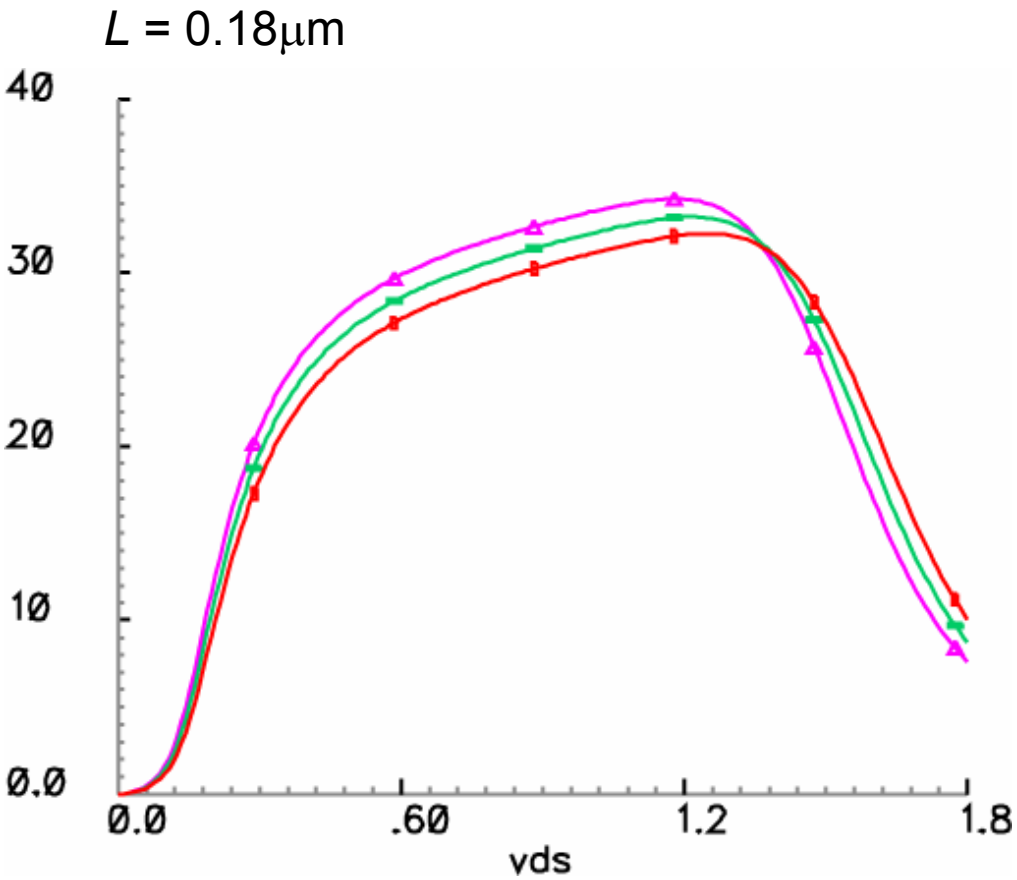
Open-loop Gain a_{v0}



- More useful than r_o
- Represents maximum attainable gain from a transistor

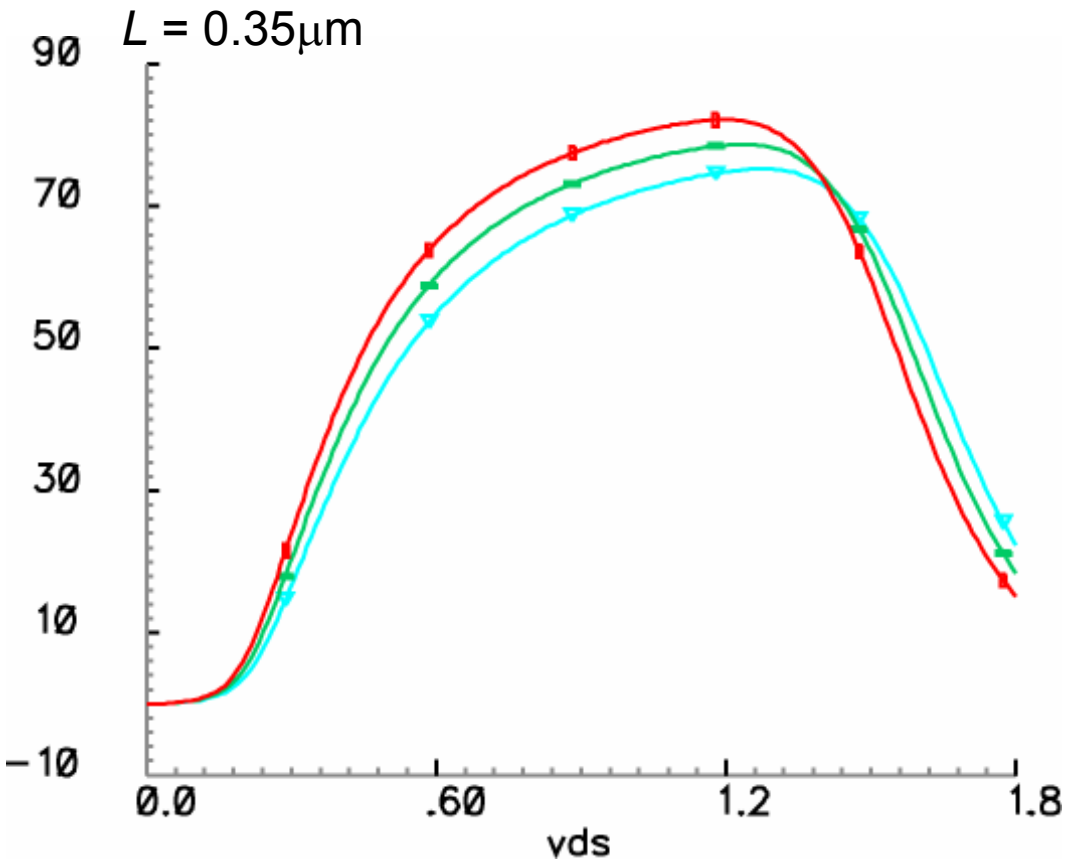
- Simulation Notes:
- Use feedback to bias $V_{ds} = V_{gs}$
- Use relatively small gain (100) for
- Fast DC conversgence

Gain, $a_{v0} = g_m r_o$



- Strong tradeoff: a_{v0} versus V_{DS} range
- ***Create such plots for several device length' for design reference***

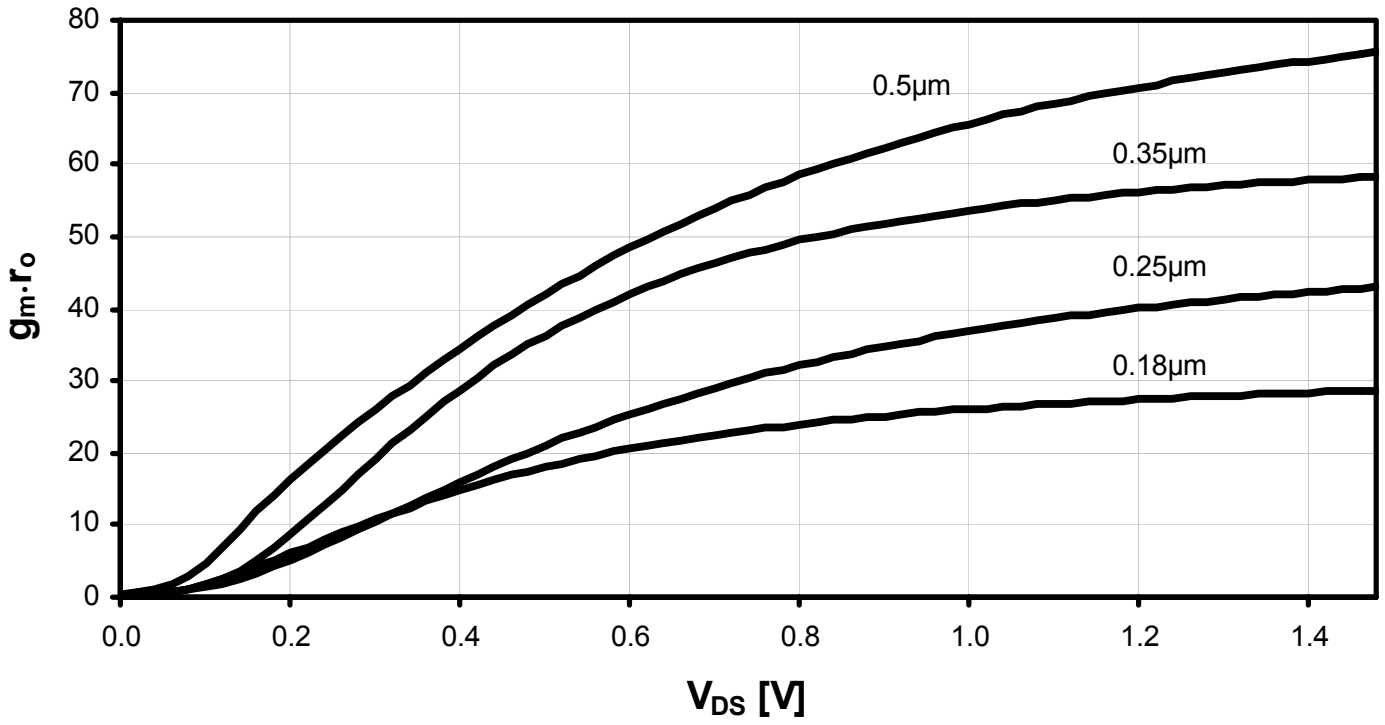
Long Channel Gain



L ↑ → a_{v0} ↑

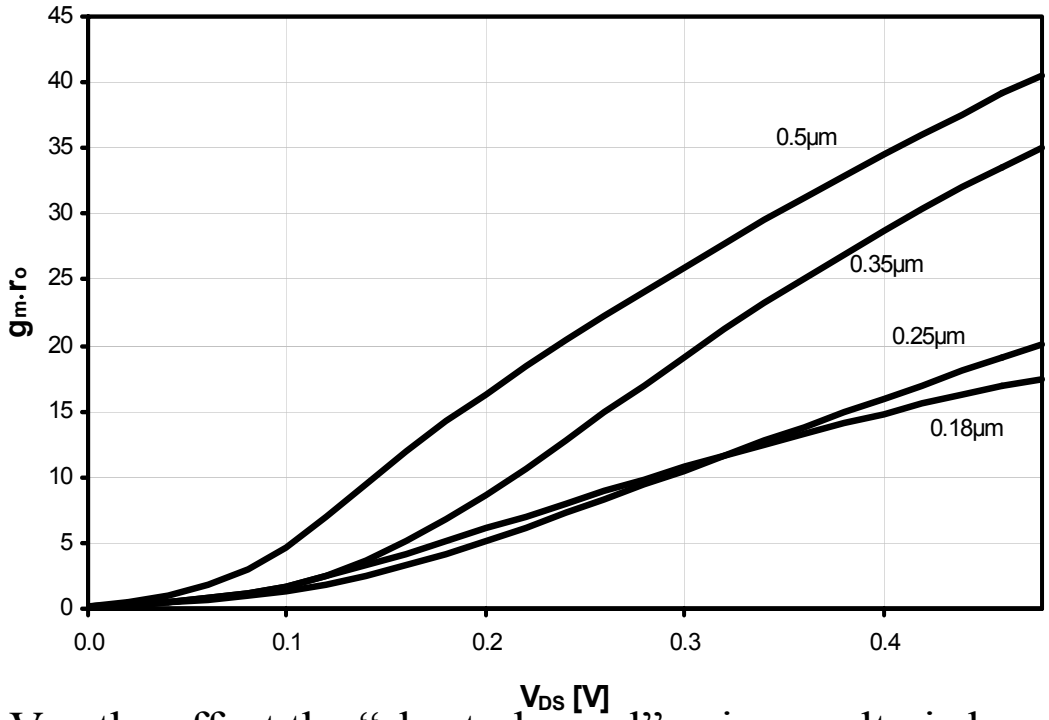
like long channel device

Technology Trend

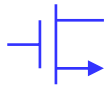


Short channel devices suffer from reduced per transistor gain

Transistor Gain Detail



For practical V_{DS} the effect the "short-channel" gain penalty is less severe (remember: worst case V_{DS} is what matters!)

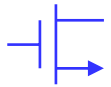


Saturation Voltage vs V*

- Saturation voltage
  - Minimum V_{DS} for "high" output resistance
  - Poorly defined: transition is smooth in practical devices

- "Long channel" (square law) devices:
  - $V_{GS} - V_{TH} = V_{dsat} = V_{ov} = V^*$
  - Significance:
    - Channel pinch-off
    - $I_D \sim V^{*2}$
    - Boundary between triode and saturation
    - r_o "large" for $V_{DS} > V^*$
    - C_{GS}, C_{GD} change
    - $V^* = 2\, I_D / g_m$

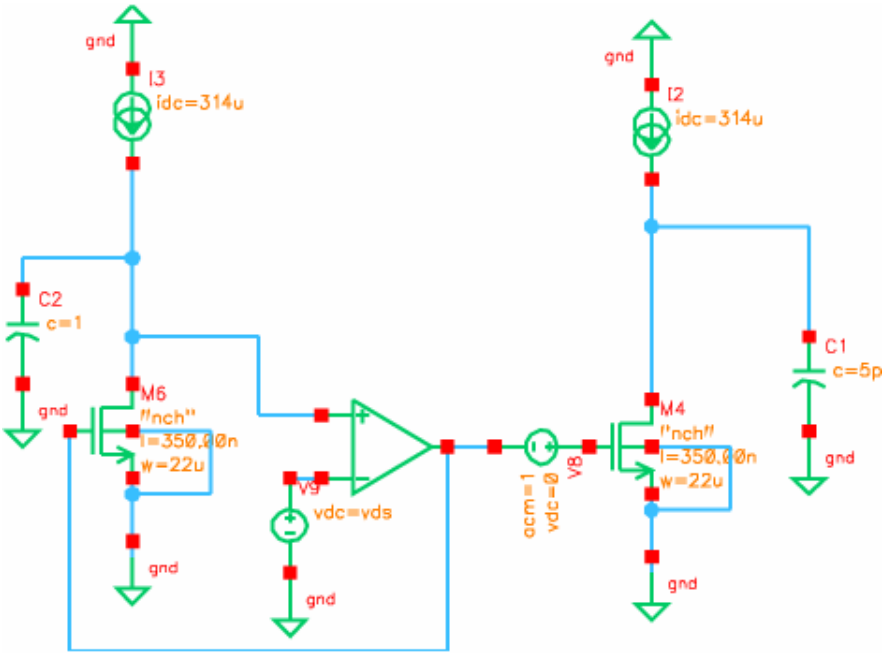
- "Short channel" devices:
  - All interpretations of V* are ***approximations***
  - Except $V^* = 2\, I_D / g_m$ (but $V^* \neq V_{dsat}$)



Design Example

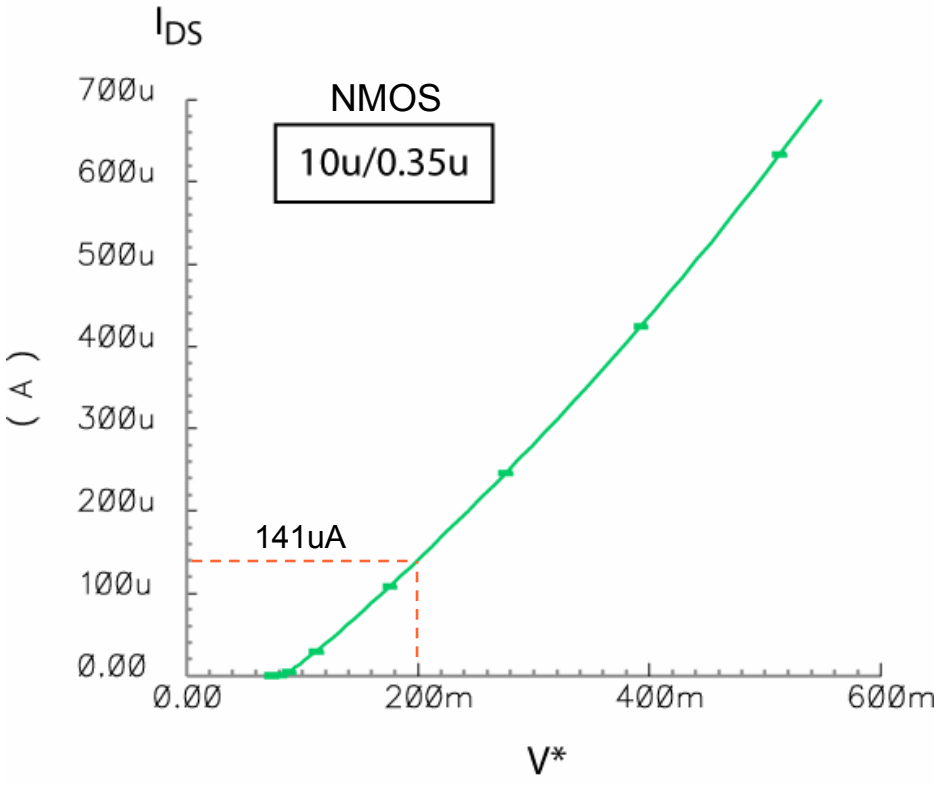
Example: Common-source amp

$a_{v0} > 70$, $f_u = 100\text{MHz}$ for $C_L = 5\text{pF}$



- $a_{v0} > 70 \rightarrow L = 0.35\mu\text{m}$
- $g_m \approx 2\pi f_u C_L = 3.14\text{mS}$
- High f_T (small C_{GS}): $V^* = 200\text{mV}$
- $I_D = \frac{g_m V^*}{2} = 314\mu\text{A}$

Device Sizing

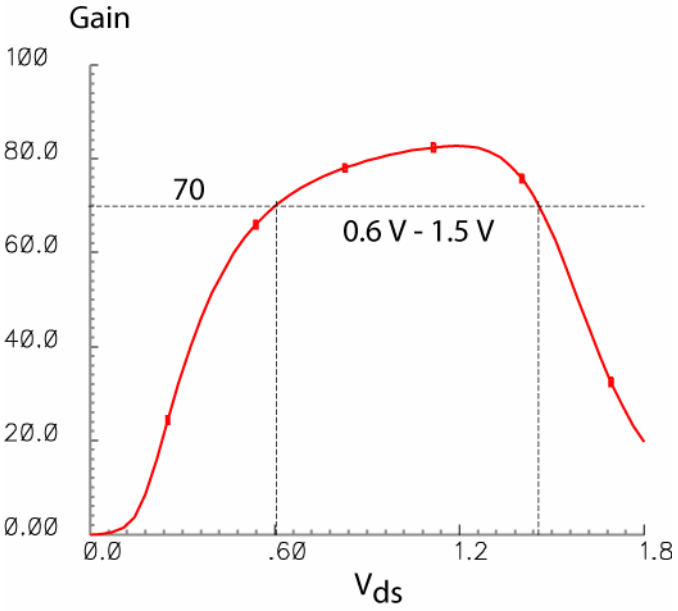


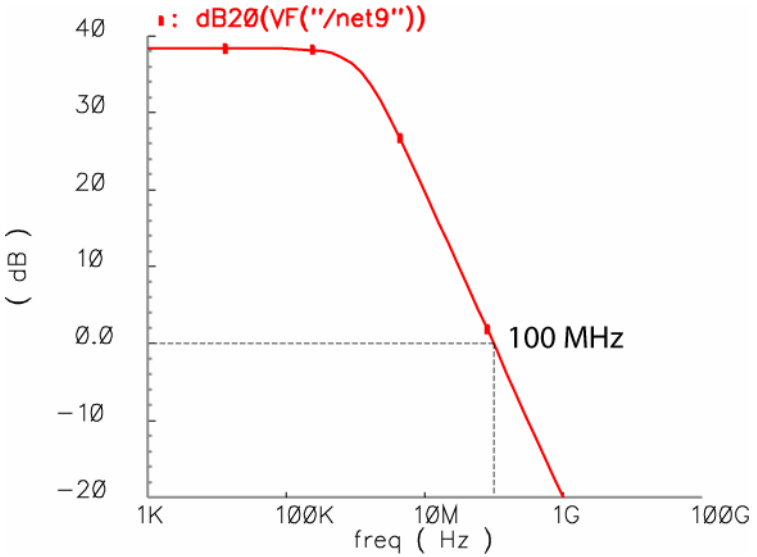
- Pick L 0.35µm
- Pick V* 200mV
- Determine g_m 3.14mS
- $I_D = 0.5\ g_m\ V^*$ 314µA
- W from graph (generate with SPICE)

  → W = 10µm (314µA /141µA)
  = 22µm

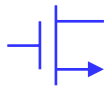
- ***Create such graphs for several device lengths for design reference***

Common Source Sims



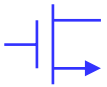


- Amplifier gain > 70
- Amplifier unity gain frequency is “dead on”
- Output range limited to 0.6 V – 1.5 V to maintain gain (about 0.45V swing)

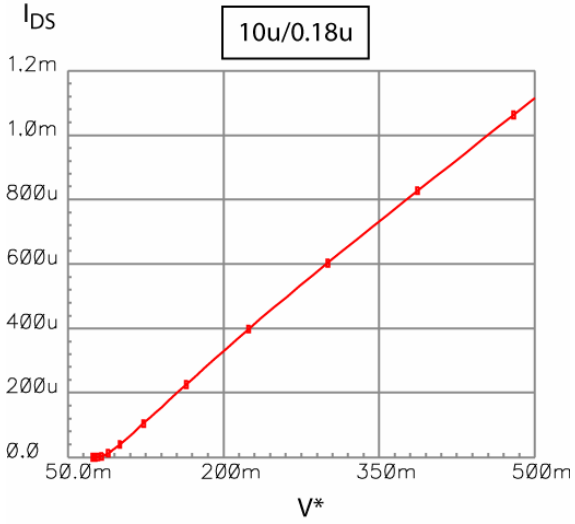


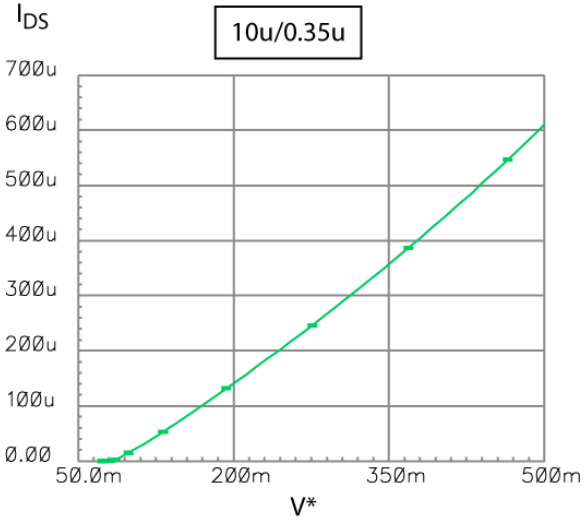
Small Signal Design Summary

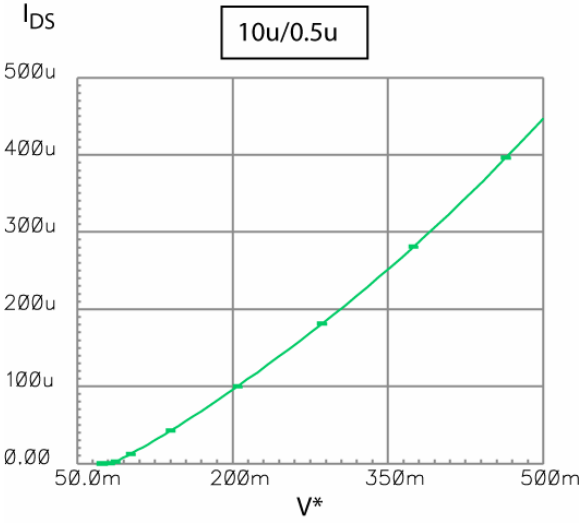
- Determine g_m (from design objectives)
- Pick L
  - Short channel → high f_T
  - Long channel → high r_o, a_{v0}
- Pick $V^* = 2I_D/g_m$
  - Since V^* is ***approximately*** the saturation voltage
  - Small V^* → large signal swing
  - High V^* → high f_T
  - Also affects noise (see later)
- Determine I_D (from g_m and V^*)
- Determine W (SPICE / plot)
- **Accurate for short channel devices → key for design**



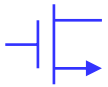
Device Sizing Chart







Generate these curves for a variety of L's and device flavors (NMOS, PMOS, thin oxide, thick oxide, different VT)



Device Parameter Summary

Device Parameter	Circuit Implications
V*	• Current efficiency, g_m/I_D • Power dissipation (I_D) • Speed (g_m) • Cutoff frequency, f_T → phase margin, noise • Headroom, $V_{DS,min}$
L	• Cutoff frequency, f_T → phase margin, noise • Intrinsic transistor gain (a_{v0})
W	• Obtain from L, I_D • Self loading (C_{GS}, C_{DB}, …)