EECS 240
Analog Integrated Circuits

Lecture 2: CMOS Technology and Passive Devices

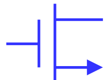
Ali M. Niknejad and Bernhard E. Boser

© 2006

Department of Electrical Engineering and Computer Sciences

CMOS Technology

- Why look at it (again)?
- Key issues:
  1. Perspective
     - Device dimensions
     - Device performance metrics, e.g.:
       - Current efficiency
       - Speed
       - Gain
       - Noise
  2. "Short-channel characteristics"
     - Square-law model
     - Models for circuit simulation
     - Design



© 2006 A. M. Niknejad and B. Boser

Today's Lecture

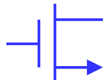
- CMOS cross-section
- Passive devices
  - Resistors
  - Capacitors
- Next time: MOS transistor

 © 2006 A. M. Niknejad and B. Boser

CMOS Process

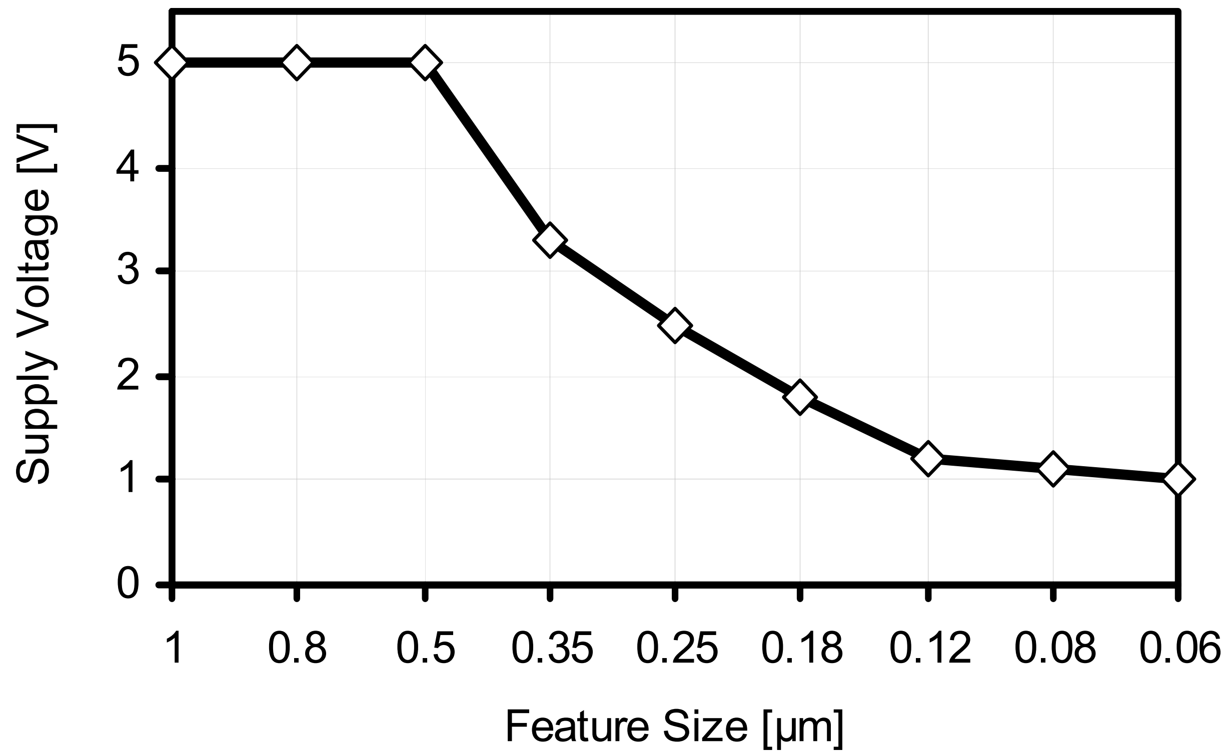
- EECS240 0.18μm 1P6M CMOS
  - Minimum channel length: 0.18μm
  - 1 level of polysilicon
  - 6 levels of metal (Cu)
  - 1.8V supply

- Other choices
  - Shorter channel length (90 nm / 1V)
  - Bipolar, SiGe HBT
  - SOI

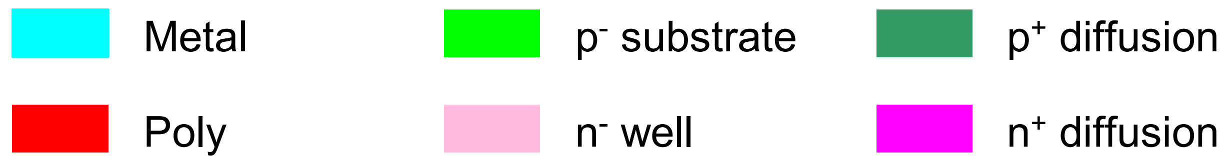


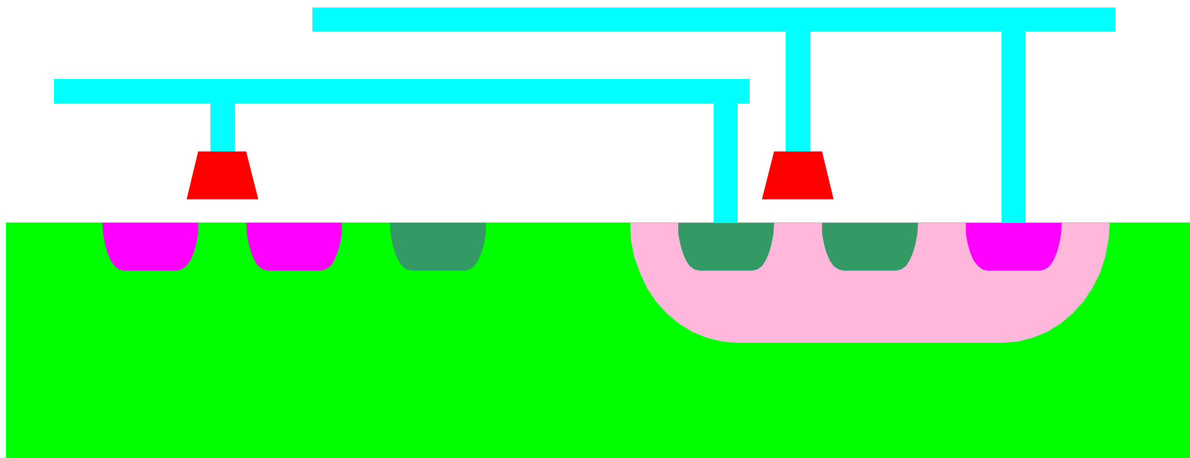
© 2006 A. M. Niknejad and B. Boser

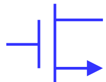
Supply Voltage



CMOS Cross Section







© 2006 A. M. Niknejad and B. Boser

Dimensions

≥ 0.35μm

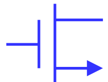
6.5nm

200nm

700mμ

1.2mμ

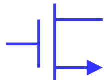
Drawing is not to scale!



© 2006 A. M. Niknejad and B. Boser

Devices

- Active
  - NMOS, PMOS
  - NPN, PNP
  - Diodes
- Passive
  - Resistors
  - Capacitors
  - Inductors



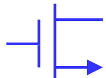
 © 2006 A. M. Niknejad and B. Boser

Resistors

- No provisions in standard CMOS
- Resistors are bad for digital circuits →
  - Minimized in standard CMOS
- Sheet resistance of available layers:

Layer	Sheet resistance
Aluminum	60 mΩ/□
Polysilicon	5 Ω/□
N+/P+ diffusion	5 Ω/□
N-well	1 kΩ/□

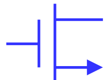
- Example: 100kΩ poly resistor
  → 1μm wide by 20,000μm long



© 2006 A. M. Niknejad and B. Boser

Process Options

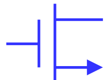
- Available for many processes
- Add features to “baseline process”
- E.g.
  - Capacitor option (MIM, 2 level poly, channel implant)
  - Low V_{TH} devices
  - “High voltage” devices (3.3V)
  - EEPROM
  - Silicide stop option
  - …



© 2006 A. M. Niknejad and B. Boser

Silicide Technology

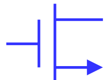
- Implants used to lower resistance of source/drain and polysilicon.
- Titanium Silicide ($TiSi_2$) is widely used salicide (self-aligned silicide), has low resistivity (13-17 $m\Omega$-cm) with melting point of 1540˚C. Another widely used silicide is $CoSi_2$.
- Platinum Silicide (PtSi) is a highly reliable contact metallization between the silicon substrate and the metal layers (Al).



Silicide Block Option

Layer	R/□ [Ω/□]	T_C [ppm/°C] @ T = 25 °C	V_C [ppm/V]	B_C [ppm/V]
N+ poly	100	-800	50	50
P+ poly	180	200	50	50
N+ diffusion	50	1500	500	-500
P+ diffusion	100	1600	500	-500
N-well	1000	-1500	20,000	30,000

- Non-silicided layers have significantly larger sheet resistance
- Resistor nonidealities:
  - Temperature coefficient: R = f(T)
  - Voltage coefficient: R = f(V)



Resistor Example

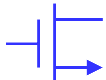
Goal: R = 100 kΩ, $T_C = 1/R \times dR/dT = 0$

Solution: combination of N+ and P+ poly resistors in series

$$R = R_N\left(1 + T_{CN}\Delta T\right) + R_P\left(1 + T_{CP}\Delta T\right)$$
$$= \underbrace{R_N + R_P}_{R} + \underbrace{\left(R_N T_{CN} + R_P T_{CP}\right)}_{0}\Delta T \quad \Rightarrow$$

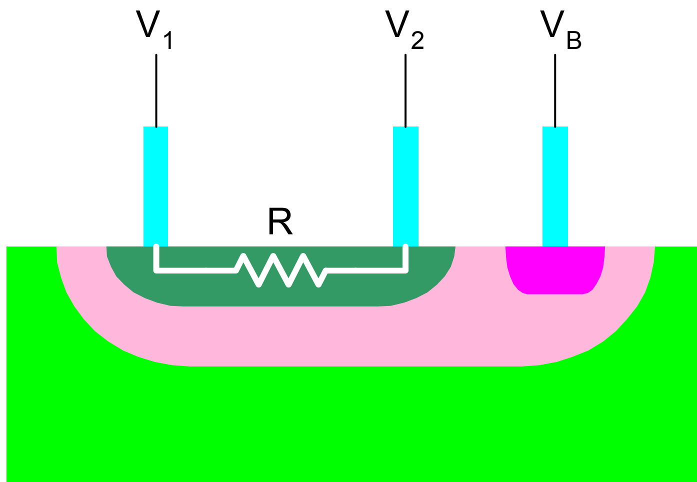
$$R_N = R\frac{1}{1 - \dfrac{T_{CN}}{T_{CP}}} = 20\text{k}\Omega = 200\text{ squares}$$

$$R_P = R\frac{1}{1 - \dfrac{T_{CP}}{T_{CN}}} = 80\text{k}\Omega = 444.4\text{ squares}$$



© 2006 A. M. Niknejad and B. Boser

Voltage Coefficient



Example:
Diffusion resistor

→ Applied voltage modulates depletion width
(cross-section of conductive channel)

→ Well acts as a shield

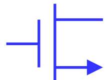
$$R = \frac{V_1 - V_2}{I}$$

$$\approx R_o\left[1 + T_C\left(T - 25^o\right) + V_C\left(V_1 - V_2\right) + B_C\left(\frac{V_1 + V_2}{2} - V_B\right)\right]$$

© 2006 A. M. Niknejad and B. Boser

Resistor Matching

- Types of mismatch
  - Systematic (e.g. contacts)
  - Run-to-run variations
  - Random variations between devices
- Absolute resistor value
  - E.g. filter time constant, bias current (BG reference)
  - ~ 15 percent variations (or more)
- Resistor ratios
  - E.g. opamp feedback network
  - Insensitive to absolute resistor value
  - "unit-element" approach rejects systematic variations (large area for non-integer ratios)
  - Process gradients
  - 0.1 … 1 percent matching possible with careful layout



Resistor Layout

Example: R1 : R2 = 1 : 2

gradient

Dummy →

0.5 * R2 + ΔR

R1

0.5 * R2 - ΔR

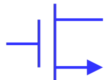
Dummy →

Resistor Layout (cont.)

Serpentine layout for large values:

Better layout (mitigates offset due to thermoelectric effects):

See Hastings, “The art of analog layout,” Prentice Hall, 2001.



© 2006 A. M. Niknejad and B. Boser

MOSFETs as Resistors

- Triode region ("square law"):

$$I_D = \mu C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS} \qquad \text{for} \quad V_{GS} - V_{TH} > V_{DS}$$

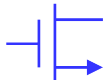
- Small signal resistance:

$$\frac{1}{R} = \frac{\partial I_D}{\partial V_{DS}} = \mu C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH} - V_{DS}\right)$$

$$R \approx \frac{1}{\mu C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH}\right)} \qquad \text{for} \quad V_{GS} - V_{TH} >> V_{DS}$$

- Voltage coefficient:

$$V_C = \frac{1}{R}\frac{\partial R}{\partial V_{DS}} = \frac{1}{V_{GS} - V_{TH} - V_{DS}}$$



© 2006 A. M. Niknejad and B. Boser

MOS Resistors

Example: R = 1 MΩ

$$R \approx \frac{1}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}$$

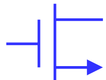
$$\frac{W}{L} = \frac{1}{\mu C_{ox} R (V_{GS} - V_{TH})}$$

$$= \frac{1}{100\frac{\mu\text{A}}{\text{V}^2} \times 1\text{M}\Omega \times 2\text{V}} = \frac{1}{200}$$

$$V_C\Big|_{V_{DS}=0V} = \frac{1}{V_{GS} - V_{TH}}$$

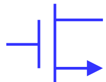
$$= \frac{1}{2\text{V}} = 0.5\text{V}^{-1}$$

- Large R-values realizable in small area
- Very large voltage coefficient
- Applications:
  - ***MOSFET-C filters:*** *(linearization)*
    Ref: Tsividis et al, "Continuous-Time MOSFET-C Filters in VLSI," JSSC, pp. 15-30, Feb. 1986.
  - ***Biasing:*** *(>1GΩ)*
    Ref: Geen et al, "Single-Chip Surface-Micromachined Integrated Gyroscope with 50°/hour Root Allen Variance," ISSCC, pp. 426-7, Feb. 2002.



Resistor Summary

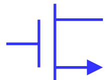
- No or limited support in standard CMOS
  - Costly: large area (compared to FETs)
  - Nonidealities:
    - Large run-to-run variations
    - Temperature coefficient
    - Voltage coefficients (nonlinear)
- Avoid them when you can
  - Especially in critical areas, e.g.
    - Amplifier feedback networks
    - Electronic filters
    - A/D converters
  - We will get back to this point



© 2006 A. M. Niknejad and B. Boser

Capacitor Applications

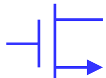
- Large value
  - Bypass capacitors
  - Frequency compensation
- High accuracy, linearity
  - Feedback & sampling networks
  - Filters



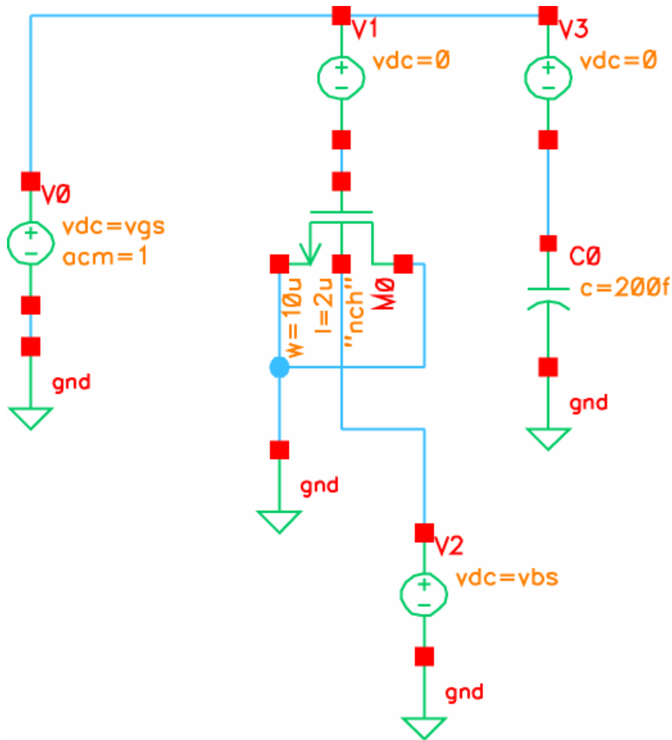
© 2006 A. M. Niknejad and B. Boser

Capacitor Options

Type	C [aF/μm^2]	V_C [ppm/V]	T_C [ppm/^{o}C]
Gate	5300	Huge	Big
Poly-poly (option)	1000	10	25
Metal-metal	50	20	30
Metal-substrate	30		
Metal-poly	50		
Poly-substrate	120		
Junction capacitors	~ 1000	Big	Big



MOS Capacitor



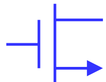
- High capacitance in inversion:
  - Linear region
  - Strong inversion
- SPICE:

$$C = \frac{I}{\omega V}$$

$$V = 1V$$

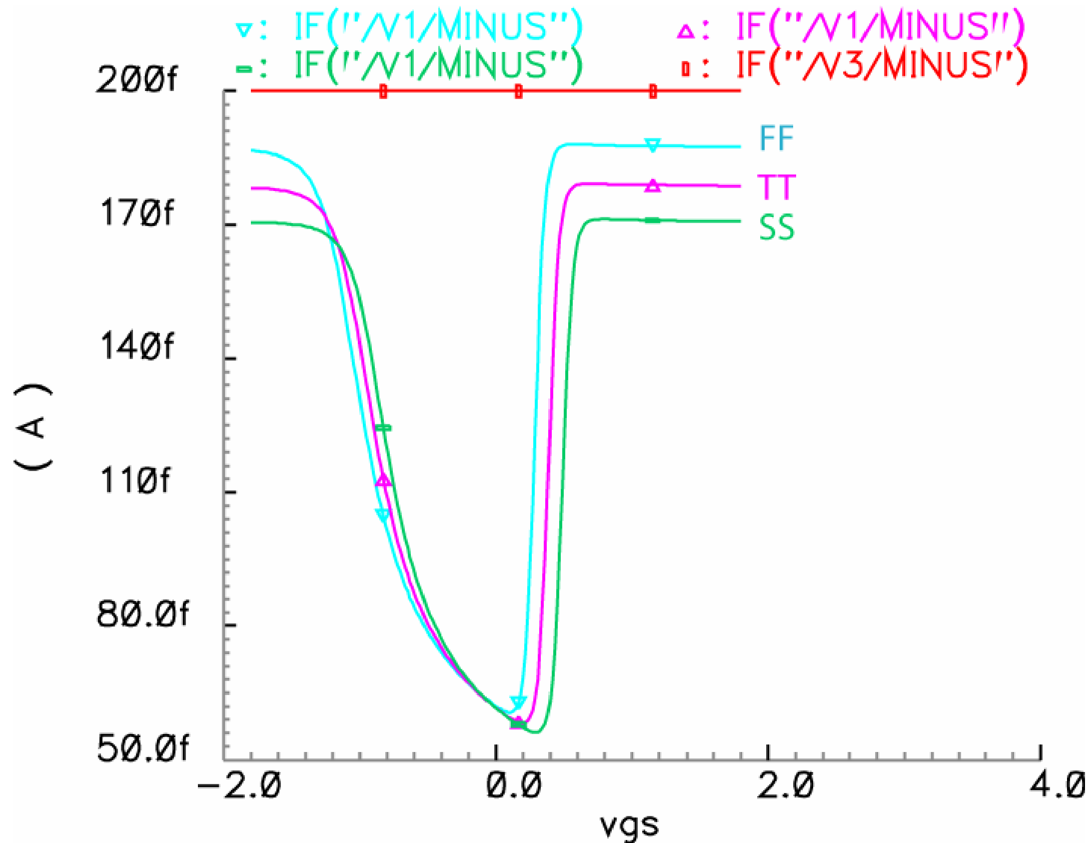
$$\omega = 1$$

$$\rightarrow C = I$$

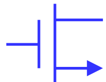


© 2006 A. M. Niknejad and B. Boser

MOS Capacitor



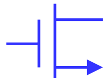
- High non-linearity, temperature coefficient
- Useful only for non-critical applications, e.g.
  - (Miller) compensation capacitor
  - Bypass capacitor (supply, bias)



© 2006 A. M. Niknejad and B. Boser

Poly-Poly Capacitor

- Applications:
  - Feedback networks
  - Filters (SC and continuous time)
  - Charge redistribution DACs & ADCs
- Cross-section
- Bottom- and top-plate parasitics
- Shields



© 2006 A. M. Niknejad and B. Boser

Capacitor Layout

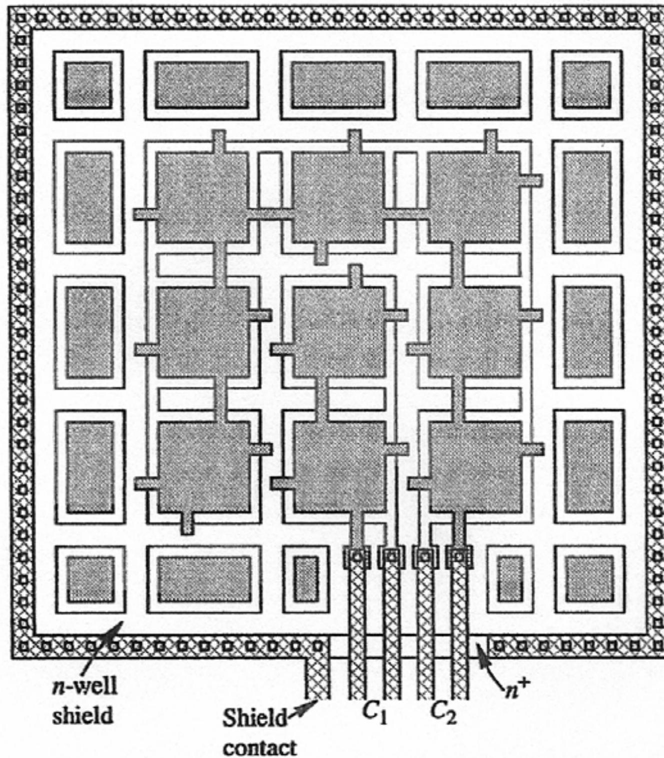
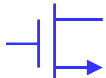


Figure 6.17 A layout of two capacitors with ratio $C_2/C_1 = \frac{3}{2}$, incorporating several of the techniques discussed in the text (adapted from Ref. 23).

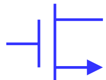
- Unit elements
- Shields:
  - Etching
  - Fringing fields
- "Common-centroid"
- Wiring and interconnect parasitics

Ref.: Y. Tsividis, "Mixed Analog-Digital VLSI Design and Technology," McGraw-Hill, 1996.



Metal Capacitors

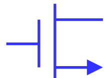
- Available in all processes (with at least 2 levels of metalization)
- Large bottom plate parasitic
  - Often loads amplifier → increased load adds power dissipation



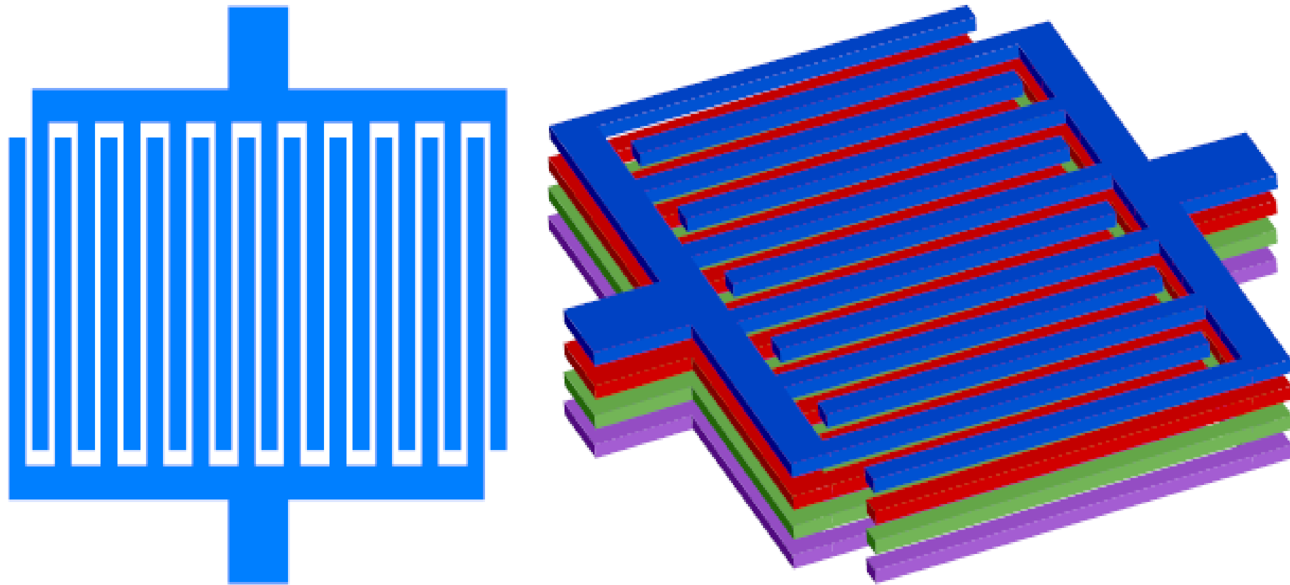
 © 2006 A. M. Niknejad and B. Boser

MIM Capacitors

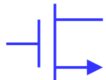
- Many processes have add-on options such as a MIM capacitor.
- This is simply a metal-insulator-metal (MIM) structure situated in the oxide layers. The insulator is a very thin layer (~25 nm), resulting in high density and relatively low back-plate parasitics.



Custom "MOM" Capacitors



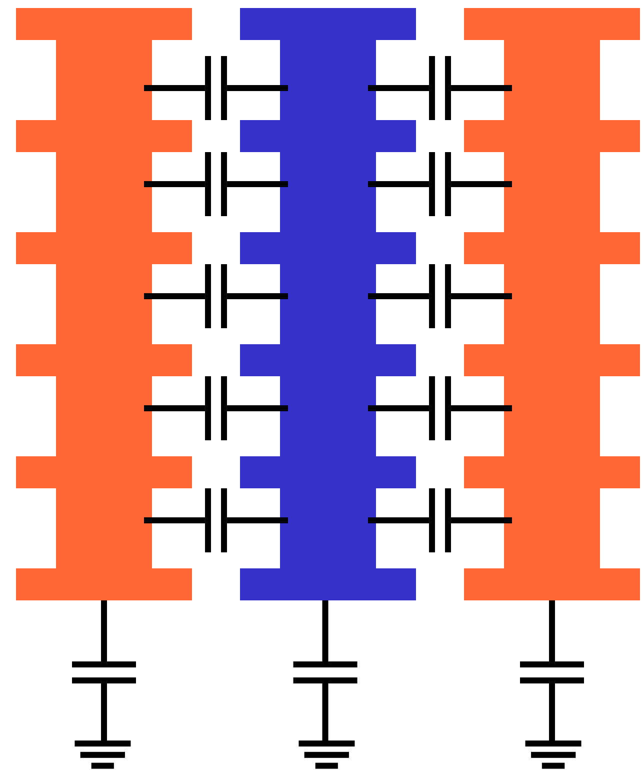
- Metal-Oxide-Metal capacitor. Free with modern CMOS.
- Use lateral flux ($\sim L_{min}$) and multiple metal layers to realize high capacitance values

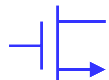


 © 2006 A. M. Niknejad and B. Boser

MOM Capacitor Cross Section

- Use a wall of metal and vias to realize high density.
- Use as many layers as possible. Use fewer layers to minimize back-plate parasitics.
- Reasonably good matching and accuracy.





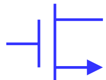
© 2006 A. M. Niknejad and B. Boser

Commercial BiCMOS Process

IBM 180-nm Technology Highlights

Category	Base Technology CMOS 7SF	Related Technologies CMOS 7RF	BiCMOS 7WL	BiCMOS 7HP
Process	Industry-standard 180-nm CMOS	CMOS 7SF with passive devices	CMOS 7RF with 60-GHz bipolar devices	CMOS 7SF with120-GHz bipolar devices
Wiring	Copper or aluminum	Copper and aluminum with analog metal	Copper and aluminum with analog metal	Copper with analog metal
Bipolar devices	N/A	N/A	3 HBTs, wireless focus	2 HBTs, high-speed optical/digital focus

www.ibm.com/chips/techlib/techlib.nsf/techdocs/FE154539B8C4C01687256CD9007346D7/$file/180-nmCMOS3-24-04.pdf



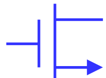
© 2006 A. M. Niknejad and B. Boser

Typical 180nm CMOS

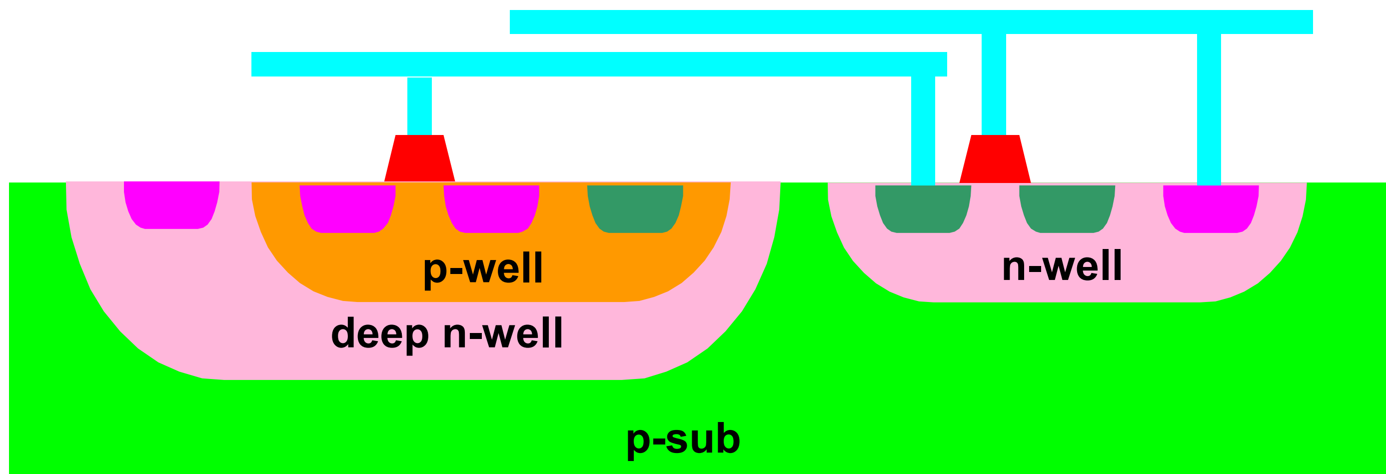
www.ibm.com/chips/techlib/techlib.nsf/techdocs/FE154539B8C4C01687256CD9007346D7/$file/180-nmCMOS3-24-04.pdf

- Leff < L
- High volage IO devices
- High voltage device has thick oxide

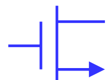
CMOS Specifications (common to 180-nm technology family)		
Lithography		180 nm
Voltage (V_{DD})		1.8 V
Additional power supply options		2.5 V / 3.3 V I/O
Standard NFET / PFET		
	L_{min}	0.18 µm
	L_{eff}	0.11 µm / 0.14 µm
	V_t	0.43 V / -0.38 V
	I_{Dsat}	600 mA / 260 mA
	I_{off}	<80 pA/µm (at 25°C)
	T_{ox}	3.5 nm
Thick-oxide NFET / PFET		
	L_{min}	0.4 µm
	L_{eff}	0.29 µm
	V_t	0.64 V / -0.67 V
	I_{Dsat}	550 mA / 235 mA
	I_{off}	<1 pA/µm (at 25°C)
	T_{ox}	7 nm



Triple Well Option



- Many modern process have a triple well (deep well) option that allows NFETs to be isolated from the substrate. Older notation: twin-well.
- This provides better immunity from digital noise in a mixed signal circuit.

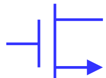


Isolation Options

CMOS Specifications	CMOS 7SF	CMOS 7RF	BiCMOS 7WL	BiCMOS 7HP
Isolation	Shallow trench	Shallow trench	Shallow and deep trench	Shallow and deep trench
Levels of metal	2–6	3–8	3–7	4–7
Metallization	Copper	Copper, aluminum	Copper, aluminum	Copper
FET devices (nominal voltage)*				
Standard NFET / PFET (1.8V)	✓	✓	✓	✓
Zero V_t NFET (1.8V)	✓	–	–	–
Isolated NFET (1.8V)	–	✓	✓	✓
High V_t NFET / PFET (1.8V)	✓	–	–	✓
High Gain NFET / PFET (1.8V)	✓	✓	–	–
Thick-oxide NFET (3.3V)	✓	✓	✓	✓
Thick-oxide Isolated NFET (3.3V)	–	✓	✓	✓
Thick-oxide Zero V_t NFET (3.3V)	✓	–	–	–

*FET devices can be used in a variety of design options that are defined in the respective technology design manuals.

www.ibm.com/chips/techlib/techlib.nsf/techdocs/FE154539B8C4C01687256CD9007346D7/$file/180-nmCMOS3-24-04.pdf



© 2006 A. M. Niknejad and B. Boser

Bipolar Devices

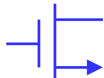
Bipolar Specifications	BiCMOS 7WL		BiCMOS 7HP	
Subcollector	Implanted		Buried	
Emitter	Not self-aligned		Self-aligned	
Transistor	High-speed	High-breakdown	High-speed	High-breakdown
Gain (ß)	140	140	500	350
V_a	155 V	170 V	90 V	120 V
BV_{ceo} / BV_{cbo}	3.3 V / 11 V	6.0 V / 9 V	1.8 V / 6.4 V	4.25 V / 12.5 V
C_{eb} / C_{cb}	5.7 / 1.97 fF/μm^2	6.6 / 1.75 fF/μm^2	9.5 / 4.6 fF/μm^2	8.5 / 2.8 fF/μm^2
R_e	9 Ω	15 Ω	2.5 Ω	45 Ω
F_t (at V_{ce} = 1 V)	60 GHz	45 GHz	120 GHz	27 GHz
F_{max} (at V_{ce} = 1 V)	85 GHz	73 GHz	100 GHz	57 GHz
$A_{e\,min}$ (length × width)	0.72 μm × 0.24 μm	0.72 μm × 0.24 μm	0.64 μm × 0.2 μm	0.64 μm × 0.2 μm

www.ibm.com/chips/techlib/techlib.nsf/techdocs/FE154539B8C4C01687256CD9007346D7/$file/180-nmCMOS3-24-04.pdf

Passives

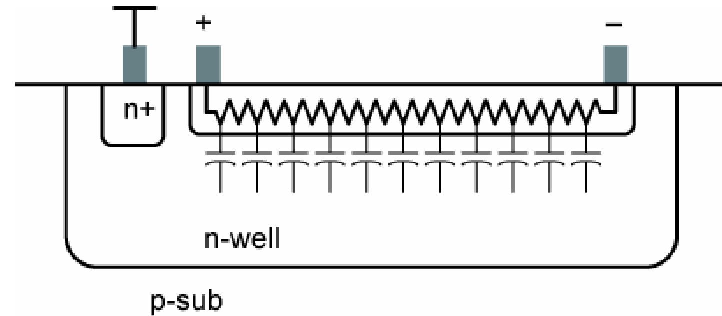
Passive Devices	CMOS 7SF	CMOS 7RF	BiCMOS 7WL	BiCMOS 7HP
Capacitors				
Single MIM	1.35 fF/µm² ± 15%	2.0 fF/µm² ± 10%	2.0 fF/µm² ± 10%	1.0 fF/µm² ± 15%
Dual MIM		4.0 fF/µm² ± 10%	4.0 fF/µm² ± 10%	
Thick-oxide MOS	7.9 fF/µm² ± 10%	7.9 fF/µm² ± 10%	7.9 fF/µm² ± 10%	2.5 fF/µm² ± 15%
Fuses	Laser	E-fuses	E-fuses	
Inductors*				
Analog metal spiral		Q = 10	Q = 10	
Thick analog metal spiral		Q = 18	Q = 18	Q = 18
Dual-metal spiral parallel stacked		Q = 24	Q = 24	
Resistors				
p+ diffusion	105 Ω/❑ ± 15%	105 Ω/❑ ± 15%	105 Ω/❑ ± 15%	105 Ω/❑ ± 15%
n+ diffusion	72 Ω/❑ ± 10%	72 Ω/❑ ± 10%	72 Ω/❑ ± 10%	72 Ω/❑ ± 10%
p+ polysilicon	260 Ω/❑ ± 15%	270 Ω/❑ ± 15%	270 Ω/❑ ± 15%	260 Ω/❑ ± 15%
p- polysilicon		1600 Ω/❑ ± 20%	1600 Ω/❑ ± 20%	1600 Ω/❑ ± 25%
Tantalum nitride on M1		61 Ω/❑ ± 6%	61 Ω/❑ ± 6%	142 Ω/❑ ± 10%
n+ subcollector diffusion				8.1 Ω/❑ ± 15%
Varactors				
Collector-base junction	–	–	✓	✓
Hyperabrupt junction	–	✓	✓	–
MOS	✓	✓	✓	✓

* All inductor measurements were taken at L = 1 nH and f = 2 GHz.



www.ibm.com/chips/techlib/techlib.nsf/techdocs/FE154539B8C4C01687256CD9007346D7/$file/180-nmCMOS3-24-04.pdf

Distributed Effects



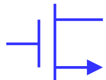
- Can model IC resistors as distributed RC circuits.
- Transmission line analysis yields the equivalent 2-port parameters.
- Inductance negligible for small IC structures up to ~10GHz.

$$R \gg \omega L$$

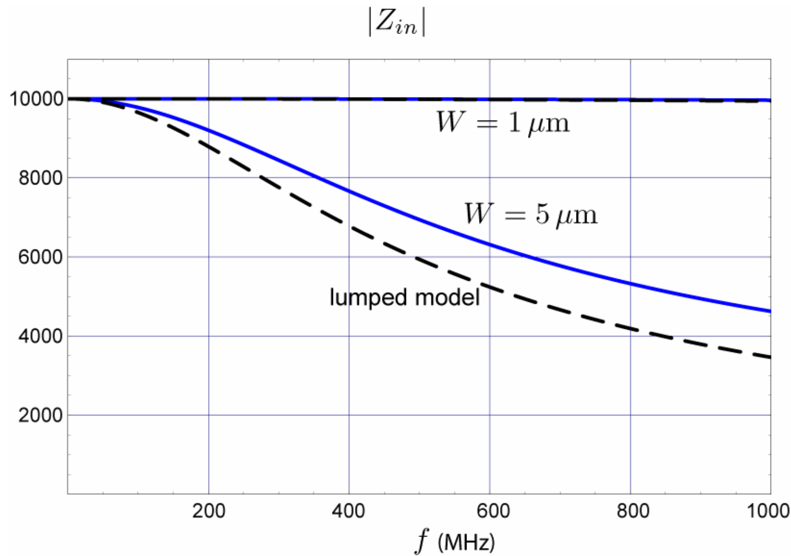
$$Y = Y_0 \begin{pmatrix} \coth\gamma\ell & \text{sech}\gamma\ell \\ \text{sech}\gamma\ell & \coth\gamma\ell \end{pmatrix}$$

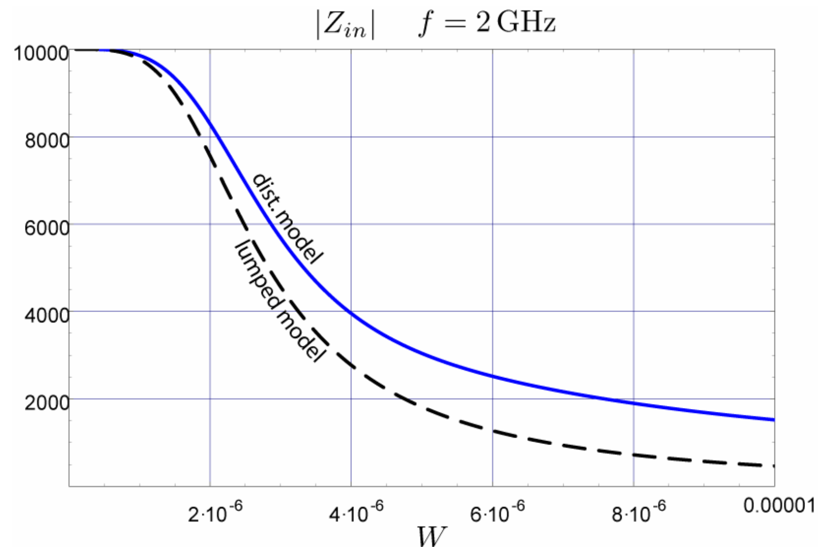
$$Z_0 = \frac{1}{Y_0} = \sqrt{\frac{R'}{j\omega C'}} = \frac{1}{W}\sqrt{\frac{R_{sh}}{j\omega C_x}}$$

$$\gamma = \sqrt{j\omega R'C'} = \sqrt{j\omega R_{sh}C_x}$$

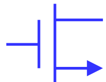


Effective Resistance



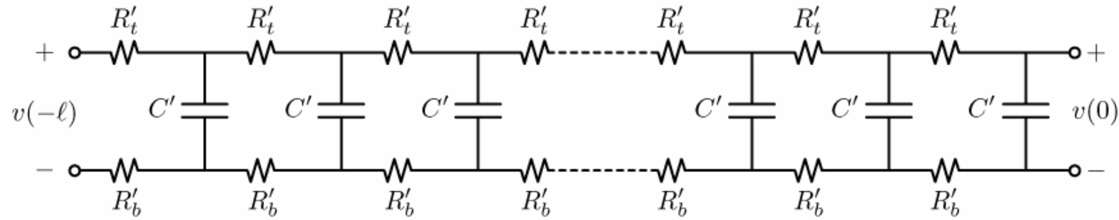


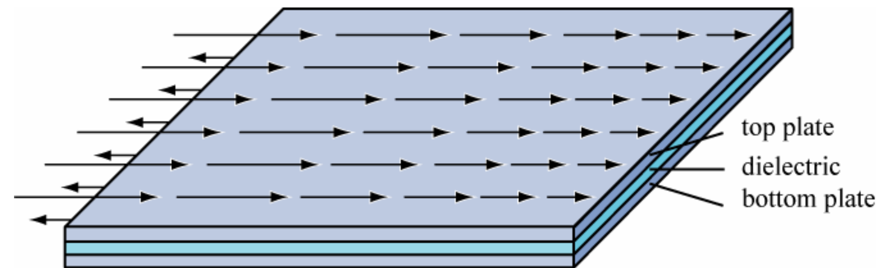
- R_{sh} = 100 Ω/□, C_x=3.45×10^{-5} F/m^2
- 10kΩ resistor drops to 5kΩ at 1 GHz ! (W=5μ)
- High frequency resistance depends on W. Need distributed model for accurate freq response.



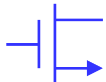
© 2006 A. M. Niknejad and B. Boser

Capacitor Q





- Current density in capacitor plates drops due to vertical displacement current.
- Must analyze the distributed RC circuit…



© 2006 A. M. Niknejad and B. Boser

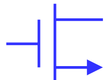
Capacitor Impedance

- For a capacitor contacted at one side, we can show that

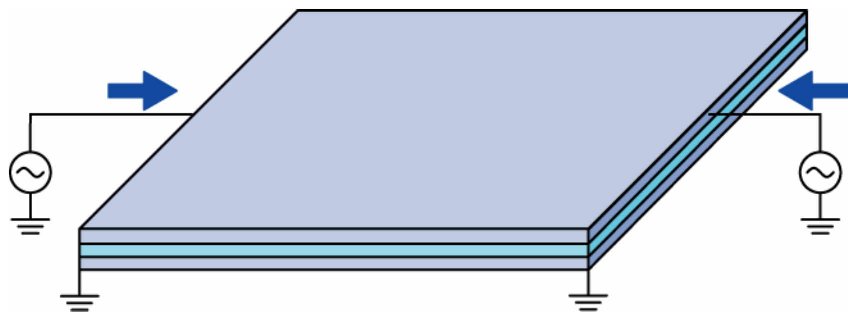
$$Z_{in} = \frac{\gamma}{j\omega C'} \coth(\gamma \ell)$$

- We can simplify this for small structures

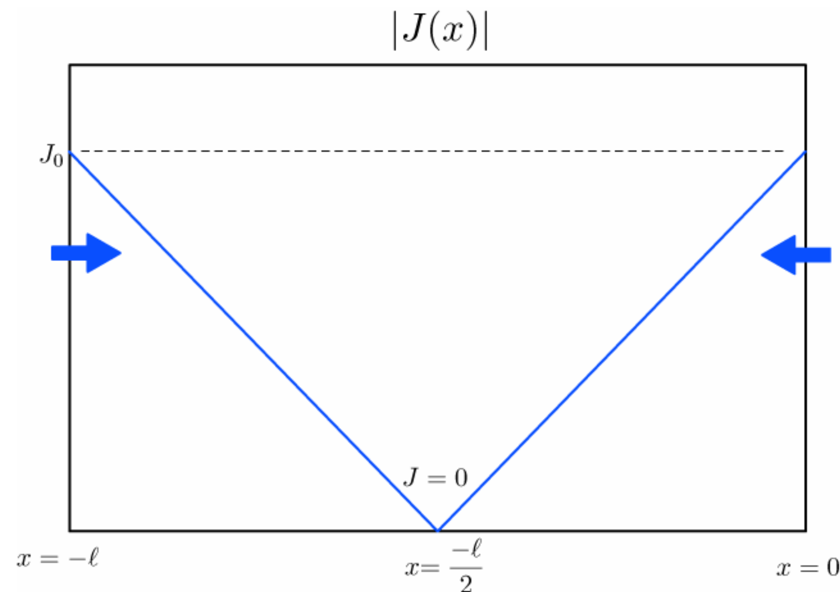
$$Z_{in} \approx \frac{R_T + R_B}{3} + \frac{1}{j\omega C}$$



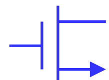
Double Contact Strucutre



$$Z_{in} \approx \frac{R}{12} + \frac{1}{j\omega C}$$

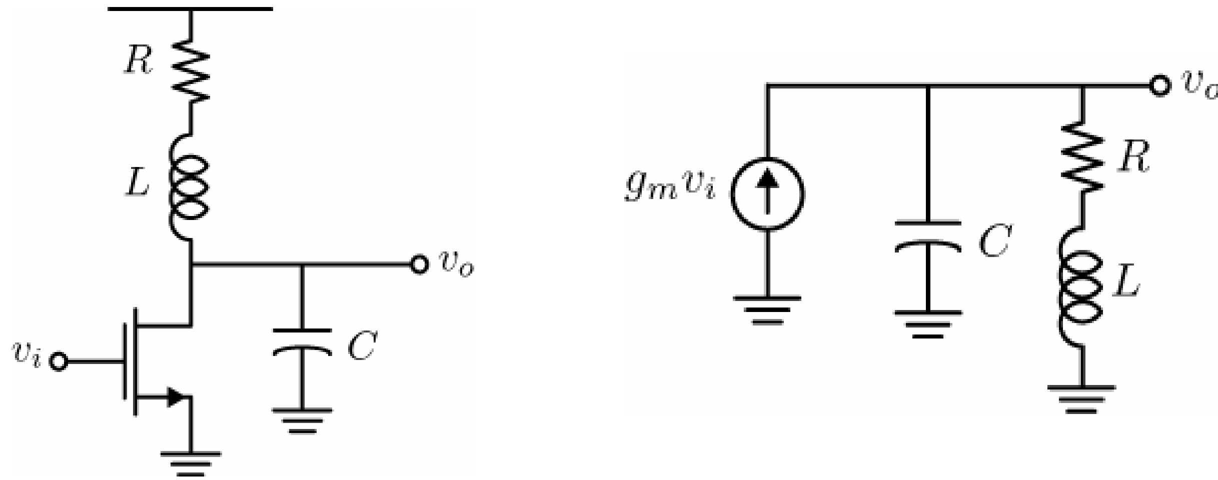


- Instead of doing distributed analysis, we can guess the current distribution as linear and quickly calculate the effective resistance.
- For a double contact case, the resistance drops by 4 times.

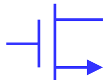


© 2006 A. M. Niknejad and B. Boser

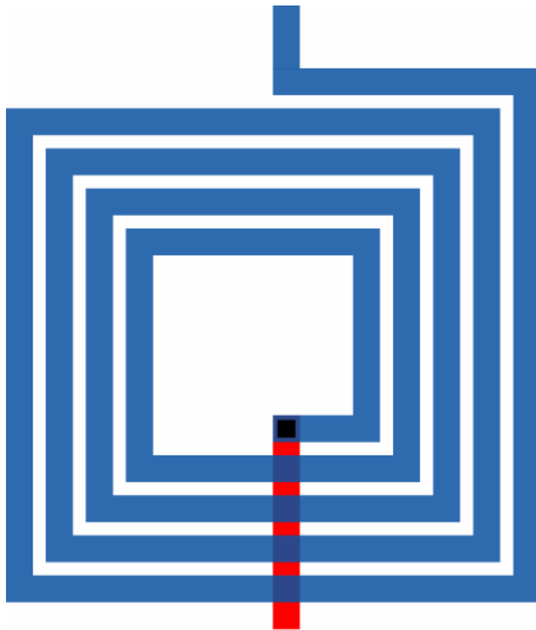
On-Chip Inductors

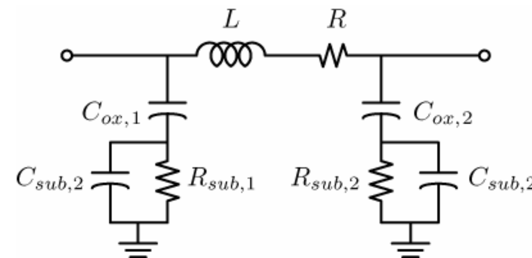


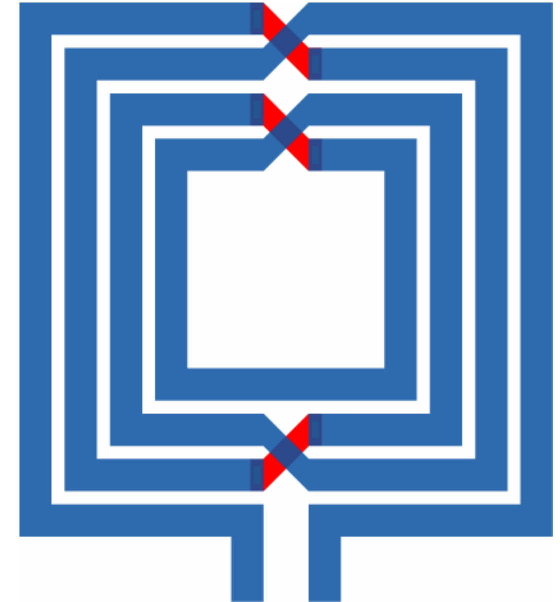
- Once in the domain of RF circuits, now inductors are finding applications in wideband design (e.g. shunt peaking).
- By proper design, the bandwidth of the RC circuit can be boosted by 85% (20% peaking).



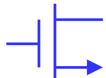
Spiral Inductors





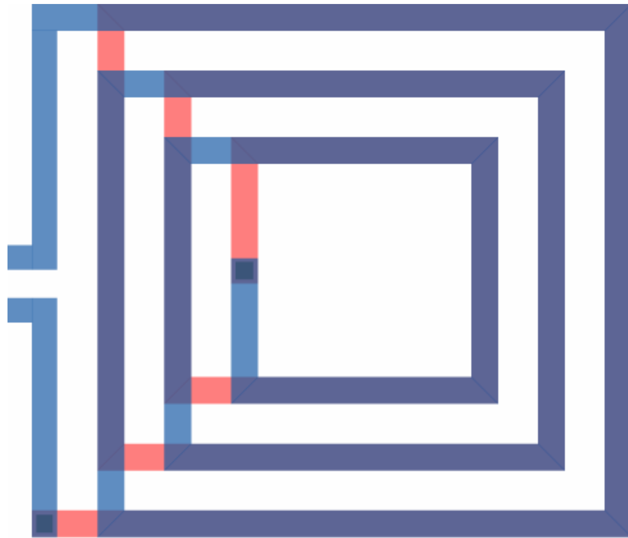


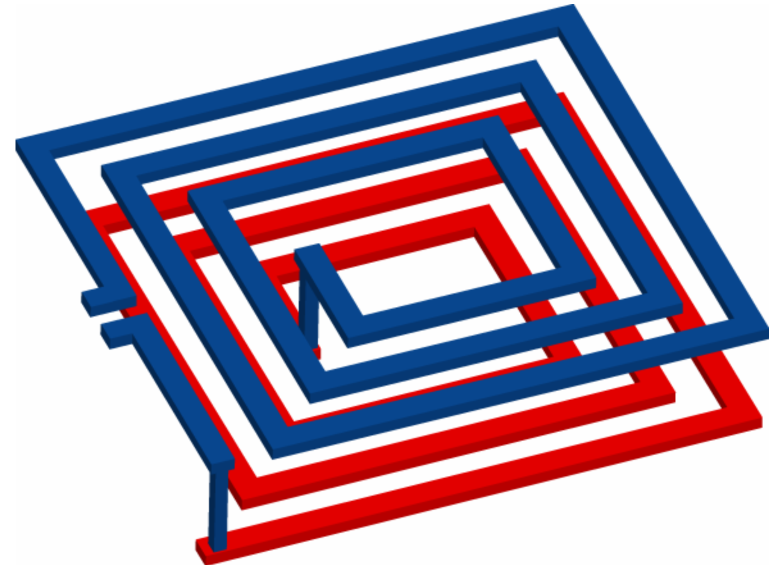
- These inductors are small (0.1-10 nH) and are used widely in RF circuits.
- Use top metal for high Q and high self resonance frequencies. Very good matching and accuracy.



© 2006 A. M. Niknejad and B. Boser

Multi-Layer Inductors


Top view


3D view (not to scale)

- By taking advantage of multiple metal layers and mutual coupling, we can realize very large inductors (~ 100 nH).