EE240 Homework #6
SOLUTIONS

Part (a), Stability:

Given that $\frac{g_m}{I_D} = 10$ for all transistors, results in $V^* = \frac{2I_D}{g_m} = 0.2V$. And since $g_{m1}=g_{m2}=10mS$, then $I_{D1} = I_{D2} = \frac{g_{m1}V^*}{2} = \frac{10mS \cdot 0.2V}{2} = 1mA$. Thus, the tail current source for the differential pair, M_{11}, must be 2mA. With this condition, the bottom current sources on the cascode side, M_3 and M_4, must also be 2mA each, and the top current sources on the cascode side, M_9 and M_{10}, must be 1mA each. Now, since M_5 and M_6 will each be carrying the same DC current as M_1 and M_2, their g_m's must also be 10mS. Finally, the sizes of the transistors were found by performing DC sweeps of the widths to achieve the required g_m while carrying the specified drain current. This resulted in the following widths: $W_1=W_2=270\mu m$, and $W_5=W_6=73\mu m$. Figure 1 below shows the final schematic and Figure 2 the simulation results for the low-frequency open-loop differential mode gain A_{dm} versus V_{od}.

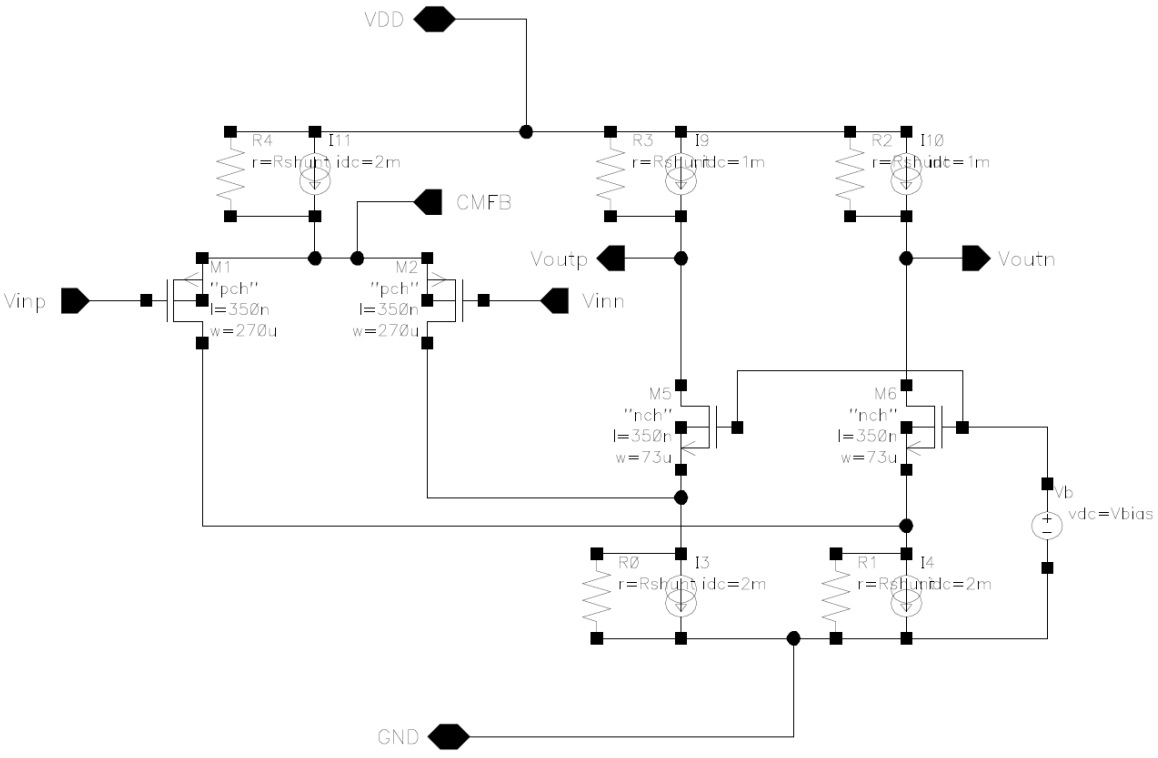

Figure 1 - Part A Schematic

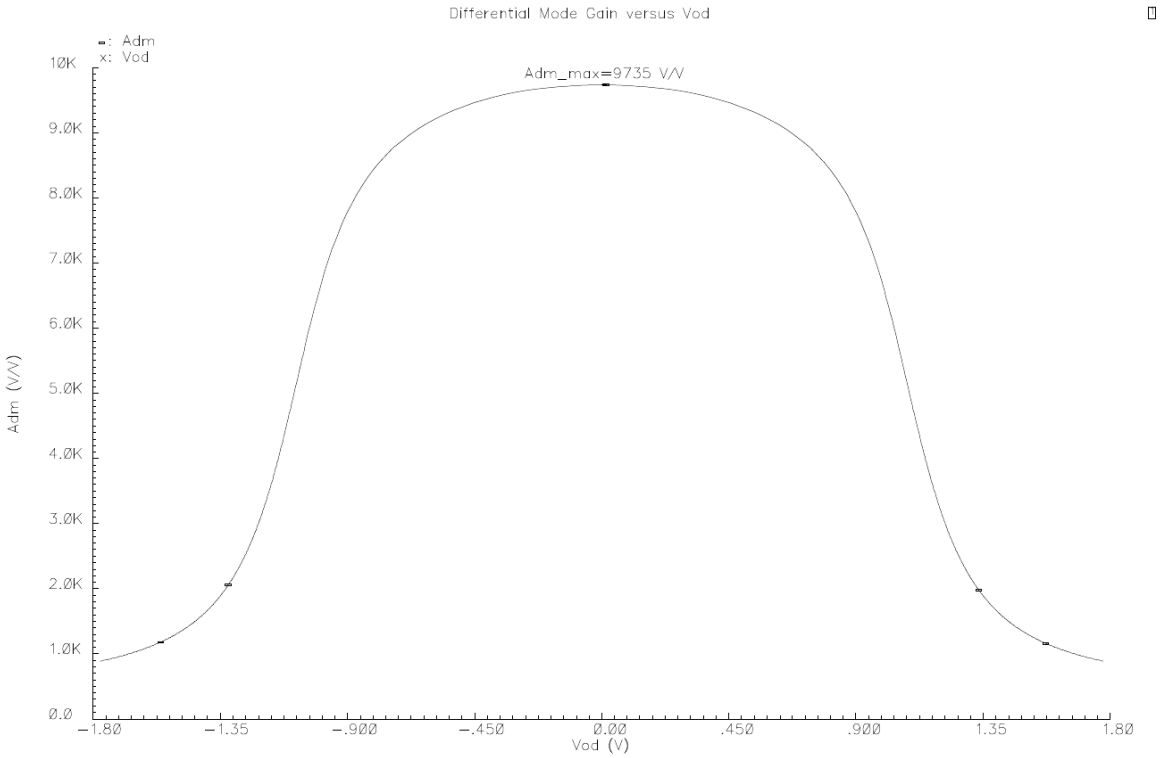

Figure 2 - A_{dm} vs V_{od}

Next, we close the feedback loop and calculate the loop gain. From Figure 1 above we can see that the low frequency maximum gain is 9,735. However, the amplifier has a frequency dependent gain $A_{dm}(s)$ which, from simulation, has a 3-dB bandwidth of approximately 30kHz. The loop-gain can be found by multiplying this with the feedback factor F, which is also frequency dependent.

$$T_{dm}(s) = A_{dm}(s) \cdot F(s)$$

$$F(s) = \frac{C_f}{C_f + C_s + C_{gs1} + (1 - A_V(s)) \cdot C_{gd1}}$$

Where $A_V(s)$ is the voltage gain of transistor M_1 and creates a frequency dependent Miller Effect on C_{gd1}. From DC analysis, C_{gs1}=720fF and C_{gd1}=182fF.

$$A_V(s) = -g_{m1} \cdot r_{o1} \parallel Z_{in,M5} = -g_{m1} \cdot r_{o1} \parallel \left(\frac{1}{g_{m5}} \left(1 + \frac{1}{s \cdot C_L \cdot r_{o5}} \right) \right)$$

From DC analysis, r_{o1}=12.9kΩ and r_{o5}=7.3kΩ. At low frequencies, Z_L=∞ and $A_V(s)$ simplifies and leads to

$$A_{V,LF} = -g_{m1} \cdot r_{o1} = -10mS \cdot 12.9k\Omega = -129$$

$$F_{LF} = \frac{C_f}{C_f + C_s + C_{gs1} + \left(1 - A_{V,LF}\right) \cdot C_{gd1}} = 0.004 \quad \text{(-48dB)}$$

At high frequencies, Z_L=0 and A_V(s) simplifies and leads to

$$A_{V,HF} = -\frac{g_{m1}}{g_{m5}} = -1$$

$$F_{HF} = \frac{C_f}{C_f + C_s + C_{gs1} + \left(1 - A_{V,HF}\right) \cdot C_{gd1}} = 0.063 \quad \text{(-24dB)}$$

The frequency at which F begins to transition from F_{LF} to F_{HF} is when $r_{o1} \cong \left| Z_{in,cascode} \right|$

$$r_{o1} = \frac{1}{g_{m5}} \left| 1 + \frac{1}{j \cdot \omega \cdot C_L \cdot r_{o5}} \right|$$

$$r_{o1} \approx \frac{1}{g_{m5} \cdot \omega \cdot C_L \cdot r_{o5}}$$

$$f_1 = \frac{1}{2\pi g_{m5} r_{o5} r_{01} C_L} = 33.8kHz$$

Since F has a single pole and a single zero, we know that it will roll up at 20dB/dec and thus we can find the frequency at which it will flatten out into F_{HF} by looking at the magnitude difference between F_{HF} and F_{LF}.

$$f_2 = f_1 \cdot 10^{\frac{F_{HF,dB} - F_{LF,dB}}{20dB}} = 533kHz$$

Now we can see that A_{dm}(s) has a pole which causes it to roll-off at about 30kHz but F(s) has a zero at about the same frequency that cancels this pole and keeps T_{dm}(s) flat for just over one more decade. At 533kHz, F(s) has a pole that then causes T_{dm}(s) to roll-off with a slope of 20dB/dec. Next, we need to calculate the low frequency loop gain.

$$T_{dm,LF} = A_{dm,LF} \cdot F_{LF} = 9735 \cdot 0.004 = 39.12 = 31.85dB$$

Finally, we need to calculate the unity-gain frequency and the frequency of the non-dominant pole in order to find the phase margin. Luckily, the non-dominant pole is approximately ω_T of M_5, which is at a very high frequency.

$$f_u = \frac{g_{m1} F_{HF}}{2\pi C_L} = 20.1MHz$$

$$f_{non-dom} = \frac{g_{m5}}{2\pi C_{gs5}} = 3.48GHz$$

$$P.M. = \arctan\left(\frac{f_{non-dom}}{f_u}\right) = 89.67^o$$

Figure 3 below shows a comparison between hand calculations and the simulation of closed-loop gain, $T_{dm}(s)$, and the phase margin.

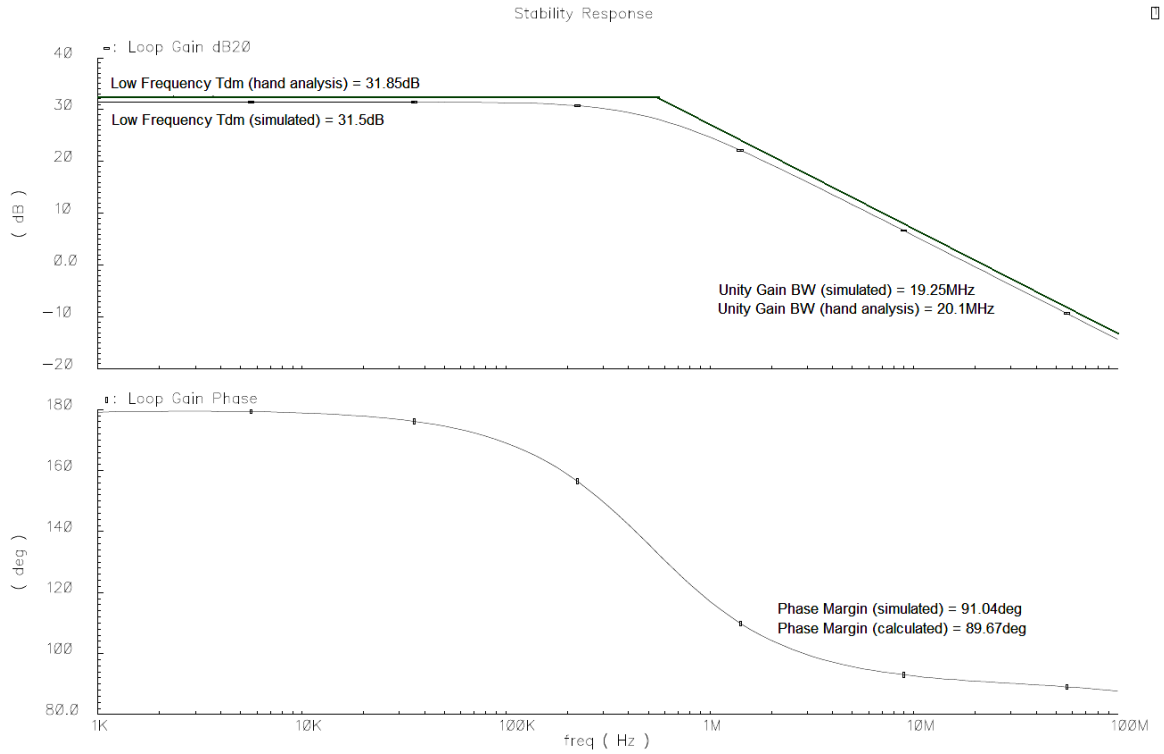

Figure 3 - Loop Gain Analysis

Part (b), Common-Mode Feedback:

In the design of the common mode feedback we first replace the tail current source of the differential pair with transistor M_{11} biased in a current mirror configuration through a large resistor in order to set the DC bias. This change is shown in the schematic in Figure 4 below.

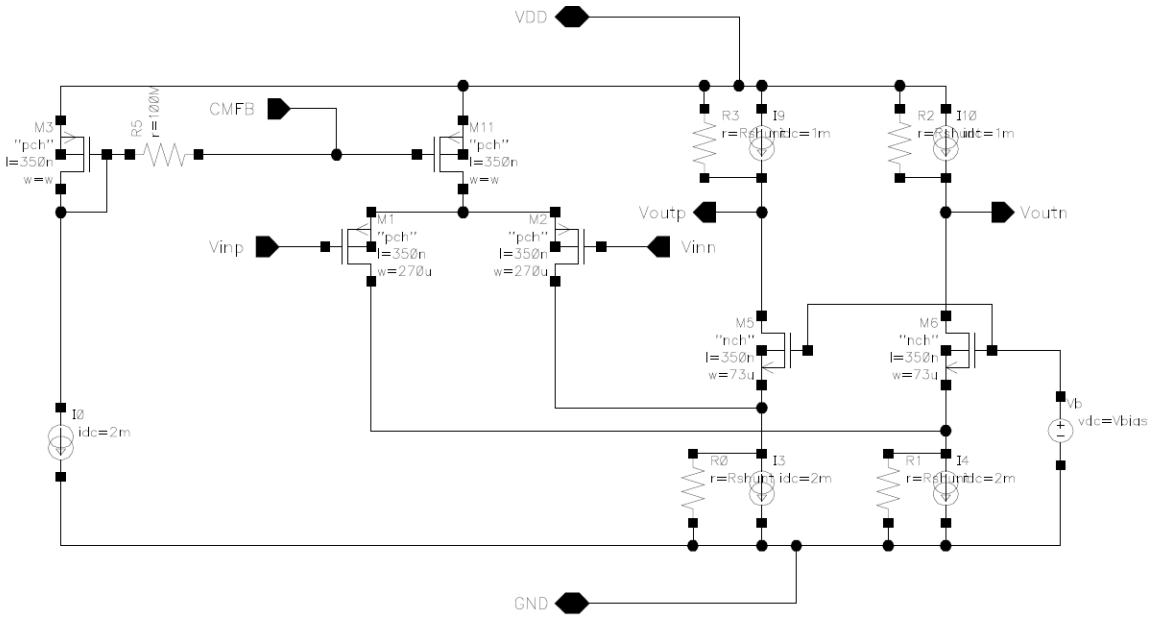

Figure 4 - Part B Schematic

Next, we add a capacitive common-mode feedback to the gate of M_{11} as shown in the high level schematic in Figure 5 below.

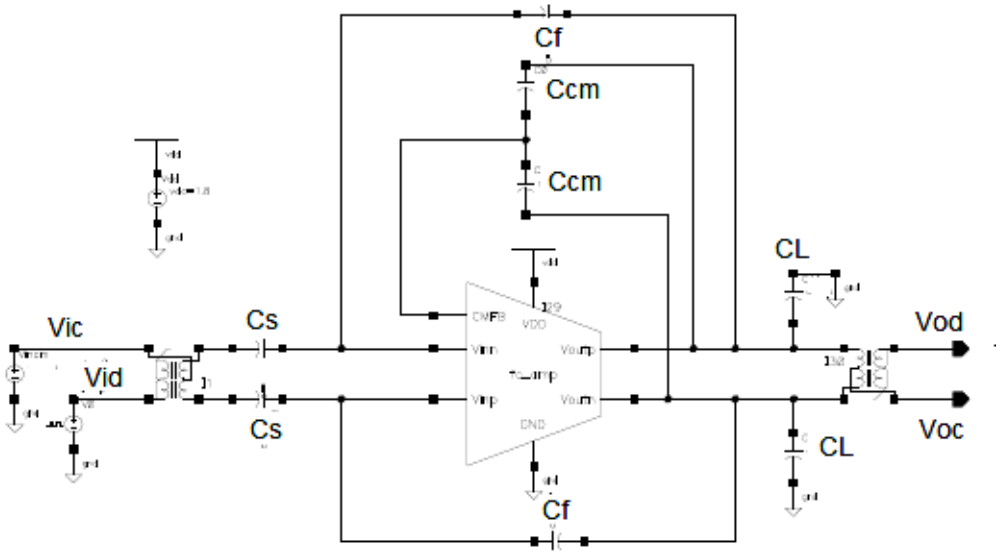

Figure 5 - Fully Differential Amplifier with Capacitive CMFB

Finally, we size M_{11} and the common-mode feedback capacitors such that the unity gain loop bandwidth of the CMFB is at least 50% of the unity gain loop bandwidth of the amplifier. Since the amplifier has a unity gain loop bandwidth of 19.25MHz, the CMFB must have a unity gain loop bandwidth greater than approximately 10MHz.

$$F_{CM} = \frac{2C_{CM}}{2C_{CM} + C_{gs11}}$$
$$\omega_{u,CM} = \frac{g_{m11}F_{CM}}{2C_L}$$

In order to maintain a device size approximately the same as the differential pair transistors, choose g_{m11}=12mS. Through DC simulations, the width of the device is found to be 200μm, giving a C_{gs11} of 570fF. Now, we can simply solve for the minimum value of F_{CM}, and resulting value of C_{CM}, that satisfies the bandwidth constraint.

$$\frac{g_{m11}F_{CM}}{2C_L} > 2\pi \cdot 10MHz$$
$$F_{CM} > \frac{4\pi \cdot 10MHz \cdot C_L}{g_{m11}}$$
$$F_{CM} > 0.026$$
$$\frac{2C_{CM}}{2C_{CM} + C_{gs11}} > 0.026$$
$$C_{CM} > 7.66\,fF$$

Thus, we can choose C_{CM} to be the same size as C_{gs11}, 570fF, in order to get F_{CM}=2/3 and maintain high gain in the common-mode feedback loop. Figure 6 below shows V_{oc} versus V_{GS11} while Figure 7 shows V_{od}, and V_{oc} versus time for an input step with V_{id} = 150mV. As can be seen from the plot, the output common mode moves by only 100μV when the input step is applied.

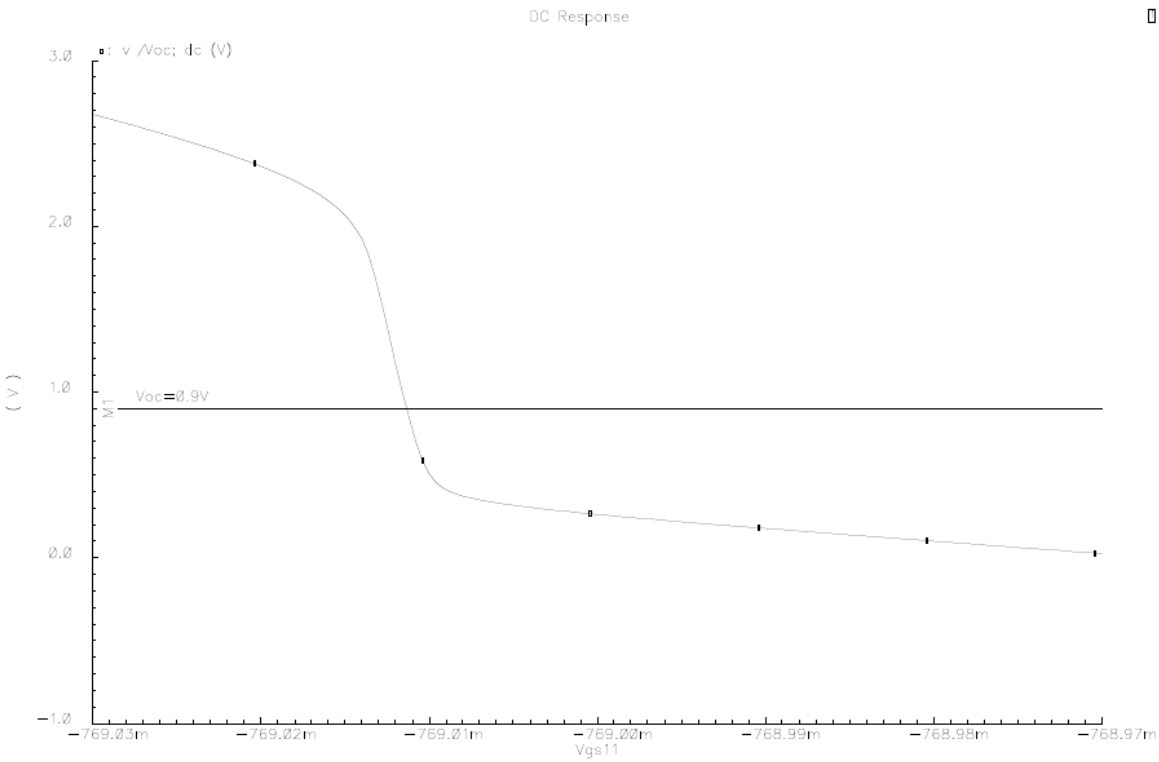

Figure 6 - V_{oc} vs V_{gs11}

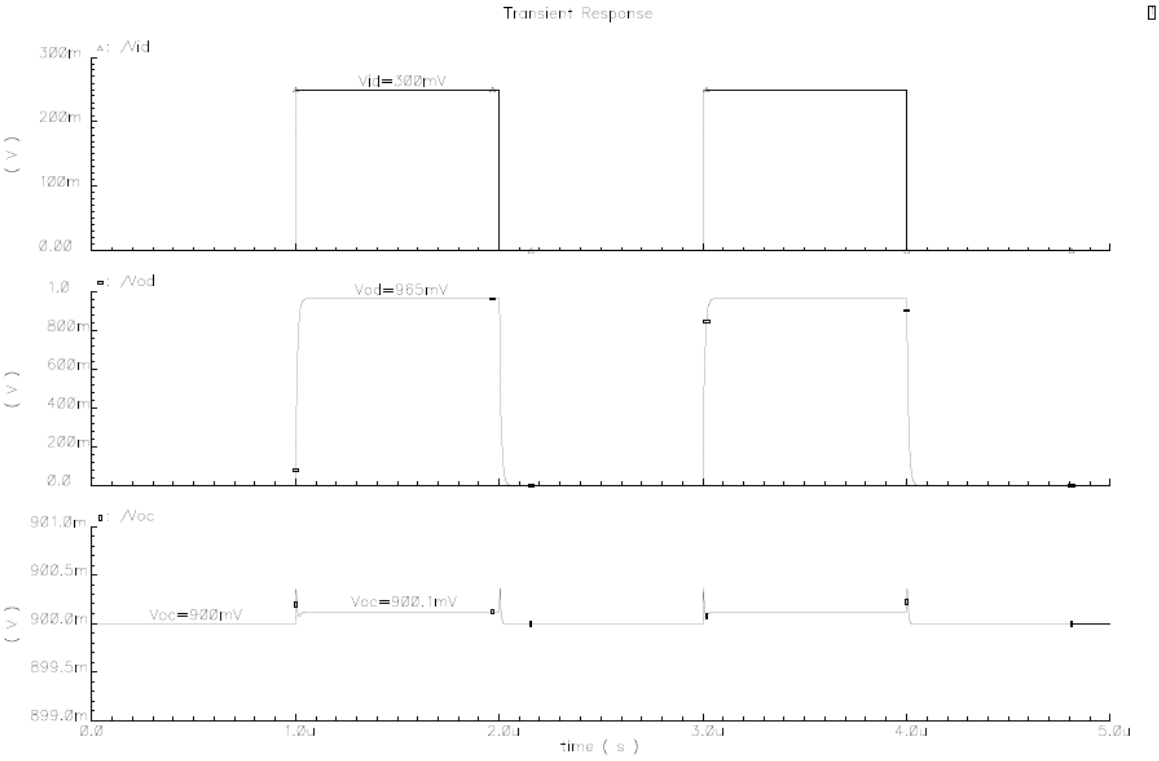

Figure 7 - V_{id}, V_{od}, V_{oc} vs Time

Part (c), Settling:

In order to find the settling time, we apply an input step which introduces multiple high frequency components so we should treat it as a high frequency signal. First we must consider whether or not we can ignore the feedforward zero. From part (a) we know that at high enough frequencies F goes to $F_{HF} = 0.063$.

$$C_{L,eff} = C_L + C_{CM} + (1-F)C_f = 5.81pF$$

Since $\left|\frac{p}{z}\right| = \frac{F \cdot C_f}{C_{L,eff}} = 0.0025 << 1$, we can ignore the feedforward zero and proceed as if we were only dealing with a single pole system.

$$\tau = \frac{-t_S}{\ln(\varepsilon)} = \frac{-50ns}{\ln(0.0005)} = 6.57ns$$

$$g_{m1} = \frac{C_{L,eff}}{F \cdot \tau} = \frac{5.81pF}{0.063 \cdot 6.57ns} = 14mS$$

Running a DC simulation yields a drain current of 2.06mA to achieve g_{m1} = 14mS, however, a transient analysis shows that the system is in fact too fast. Therefore, we can reduce the bias current until the target of 50ns settling time is achieved. The final results are as follows:

I_{D1} = 1.7mA $\qquad$ g_{m1} = 12.87mS

Finally, Figure 8 below shows the dynamic error during settling and Figure 9 shows the currents at the output of the amplifier.

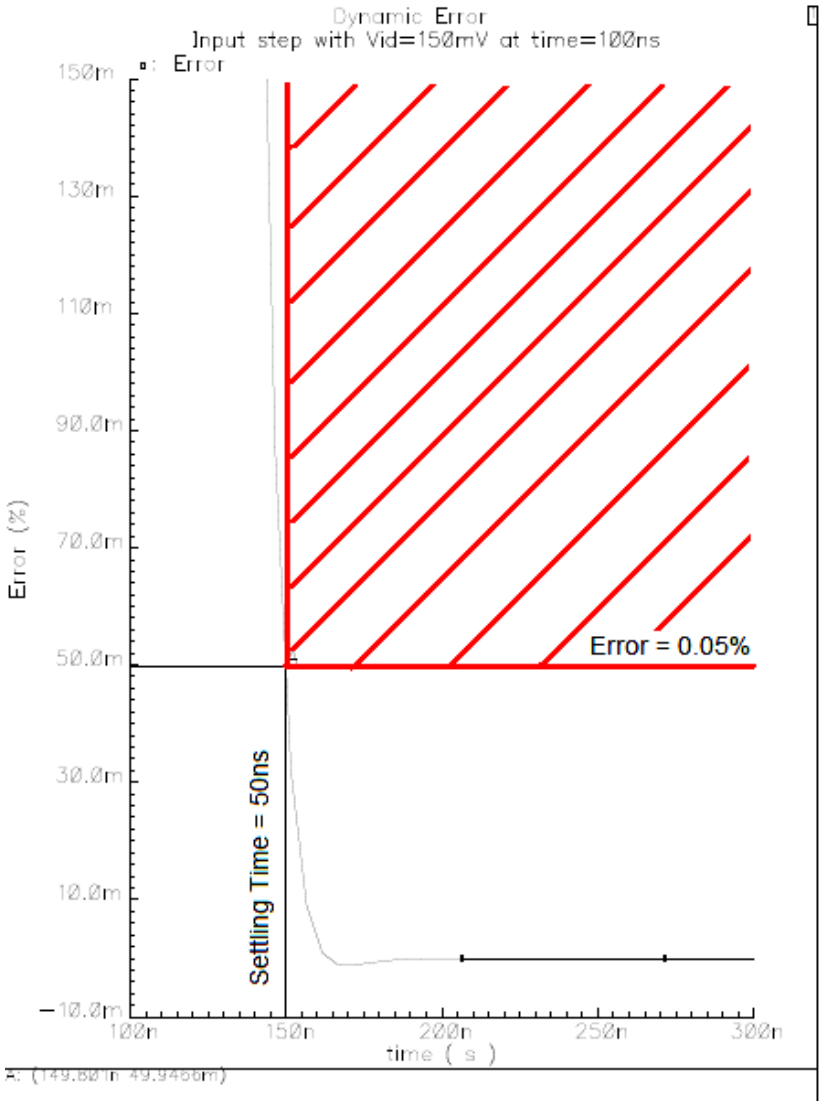

Figure 8 - Settling Time

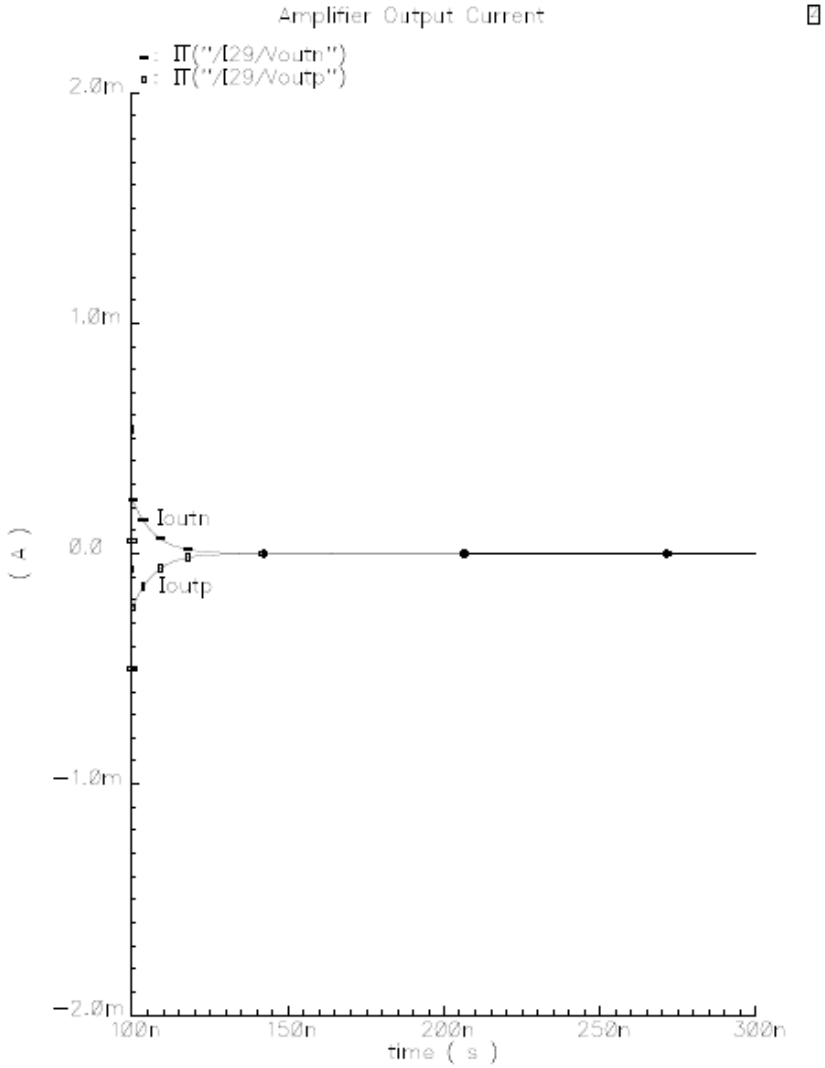

Figure 9 - Output Currents

Part (d), Noise:

The updated schematic from part (a) is shown below in Figure 10. The current sources and their cascodes have been realized with transistors and the biasing has been realized with the use of high swing cascode current mirrors. Since all new transistors are biased with $\frac{g_m}{I_D} = 5$, they all have g_m = 5mS.

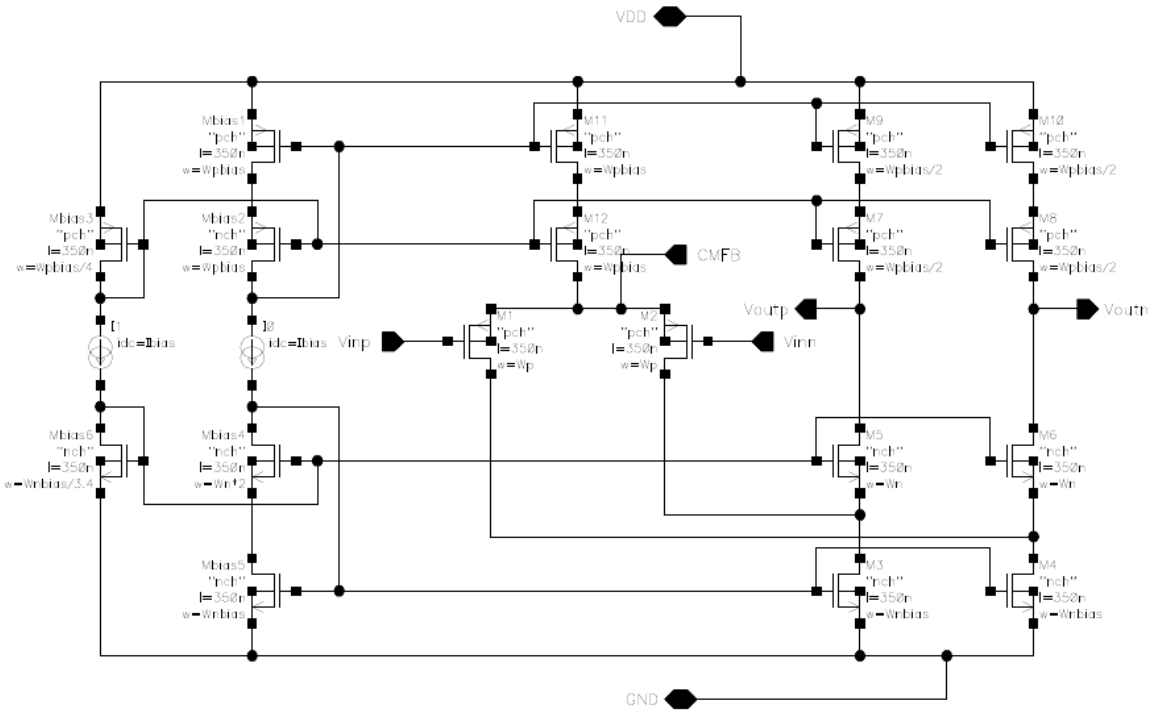

Figure 10 - Part D Schematic

First we recognize that the output resistance of the feedback amplifier is approximately calculated as

$$R_o = \frac{1}{F \cdot G_m} = \frac{1}{F \cdot g_{m1}}$$

Next we can calculate the output noise due to the main contributors. For simplicity we assume the bias transistors, cascodes, and tail current source contribute negligible amounts of noise to the output. We also ignore flicker noise for simplicity.

$$\overline{i_o^2} = 2\left(\overline{i_1^2} + \overline{i_4^2} + \overline{i_{10}^2}\right) f_{-3dB,noise}^2$$

$$\overline{v_o^2} = 2\left(\overline{i_1^2} + \overline{i_4^2} + \overline{i_{10}^2}\right) \cdot R_o^2 \cdot f_{-3dB,noise}^2$$

$$\overline{v_o^2} = 2 \cdot 4 \cdot kT\gamma\left(g_{m1} + g_{m4} + g_{m10}\right) R_o^2 \frac{\pi}{2} \cdot \frac{1}{2\pi R_o C_{L,eff}}$$

$$\overline{v_o^2} = \frac{2kT\gamma}{FC_{L,eff}}\left(1+\frac{g_{m4}}{g_{m1}}+\frac{g_{m10}}{g_{m1}}\right) = \frac{5kT\gamma}{FC_{L,eff}}$$

Assuming $\gamma = 1$, this results in $\overline{v_o^2} = 62.2nV^2$. Now we must find the target noise we must achieve to attain a peak SNR of 90dB.

$$\left(\frac{V_{od,\max,rms}^2}{\overline{v_o^2}}\right) = 10^{SNR/20dB}$$

$$\overline{v_o^2} = \frac{\left(\frac{1.6}{2\sqrt{2}}\right)^2}{10^{90dB/20dB}} = 320pV^2$$

Finally, in order to maintain the speed of the amplifier we must keep τ constant, and therefore the ratio of $g_{m1}F$ to $C_{L,eff}$ must remain constant. The target noise was achieved by scaling up C_f, C_s, C_L, I_{bias}, and the transistor widths using an optimization program while maintaining a constant τ. The final component sizes are as follows:

g_{m1}	=	422.8mS	C_f	=	60.1pF
C_s	=	240pF	C_L	=	486pF

The noise summary shown below demonstrates that the final total output noise achieved was $319.1pV^2$, giving an SNR at the output of the amplifier of 90.01dB.

Device	Param	Noise Contribution	% Of Total
I30.M3	id	7.20051e-11	22.56
I30.M4	id	7.20051e-11	22.56
I30.M1	id	3.50512e-11	10.98
I30.M2	id	3.50512e-11	10.98
I30.M10	id	2.3789e-11	7.45
I30.M9	id	2.3789e-11	7.45
I30.M3	fn	1.99371e-11	6.25
I30.M4	fn	1.99371e-11	6.25
I30.M10	fn	4.27903e-12	1.34
I30.M9	fn	4.27903e-12	1.34
I30.M2	fn	2.67693e-12	0.84
I30.M1	fn	2.67693e-12	0.84
I30.M5	id	1.35606e-12	0.42
I30.M6	id	1.35606e-12	0.42
I30.M5	fn	2.57809e-13	0.08
I30.M6	fn	2.57809e-13	0.08
I30.M7	id	1.80383e-13	0.06
I30.M8	id	1.80383e-13	0.06
I30.M7	fn	2.78595e-14	0.01
I30.M8	fn	2.78595e-14	0.01

Integrated Noise Summary (in V^2) Sorted By Noise Contributors
Total Output Noise = 3.19121e-10
Total Input Referred Noise = 4.15475e-10
The above noise summary info is for noise data