UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
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	Problem Set 6	**EECS 240**
NIKNEJAD	**Due April 13, 2006**	**SPRING 2006**

You are to design three aspects of a fully differential folded-cascode amplifier with PMOS inputs (see lecture). You may use ideal current sources (shunt with large resistor in case of convergence problems) for M3, M4, M9, M10, and M11 (omit cascodes M7, M8, M12) and an ideal CMFB (e.g. a VCCS) except when stated otherwise. Use the high-swing cascode bias circuit designed in an earlier homework or ideal voltage sources for biasing. Embed the amplifier into a fully differential feedback network with C_L=5pF, C_s=400fF, C_f=100fF.

Annotate all SPICE plots with:

- Specification (red): indicate "forbidden", i.e. out-of-spec region, which the simulation result should not traverse
- Hand-analysis (green)
- Computer simulation (black): set appropriate scale so that spec is easily verifiable. Mark axes.
- Other annotation and comments (blue)

a) **Stability:** find the width of M1, M2, M5, M6 and all bias currents such that g_{m1}=10mS and g_m/I_D=10 1/V. Use L=0.35μm. Plot (with SPICE) the low-frequency open-loop differential mode gain A_{dm} versus V_{od}. Then close the feedback loop and calculate the loop-gain $T_{dm}(s)$ and the phase margin. Verify with SPICE.

b) **CMFB:** replace the current source simulating M11 with a transistor and add a capacitive CMFB from the amplifier output to the gate of M11. Dimension all devices such that the loop bandwidth of the CMFB is at least 50% of the amplifier differential-mode loop-gain bandwidth. Perform the following checks with SPICE:
   i) .dc analysis of V_{oc} versus V_{GS11}.
   ii) .tran V_{od} and V_{oc} versus time for an input step with V_{id}=1V (add C_f back in).

c) **Settling:** Find the minimum biasing current and g_{m1} required for a dynamic settling error ε=0.05%, t_s=50ns, and $V_{id,step}$=500mV. Verify with SPICE (plot zoomed version of dynamic error and current at output of amplifier).

d) **Noise:** Revert to circuit from part (a) but realize the current sources (and their cascodes) with real transistors with $g_m/I_D=5V^{-1}$ (L=0.35μm). Find g_{m1} (change W and I_D compared to part (a)), C_L, C_s and C_f such that the peak SNR at the amplifier output (with feedback) is 90dB. Use V_{od,max_peak_peak}=1.6V (V_{DD}=3V).