Problem Set 2
Due Thursday February 9, 2006

For the following questions, use the EECS 240 180nm CMOS process technology. Note a new version has been posted with flicker noise (K_f).

1. Integrate the input referred flicker noise for a 50/0.25 NMOS transistor in a common source configuration ($R_s = 0$) from 1Hz to 1GHz. Specify the result in Vrms. Use $V^* = 200\text{mV}$ and $g_m = 100\mu\text{S}$. How does the result change if you alter the lower limit of integration to 1 year?

2. Derive an expression for the input referred noise of an NMOS common-source amplifier M1 with a PMOS load M2. Assume M1 and m2 are both in saturation and that a capacitor C_L dominates the load at the output. Specify the results as the noise from M1 multiplied by a factor that is a function of the V^* of the two transistors. Analysis of flicker noise is optional but recommended. What is the conclusion?

3. Compare the noise performance of a MOS and BJT common source/emitter stage biased with the same drain/collector current and driven from a source with resistance R_s. Derive the value of R_s for which the input referred noise from the MOS and BJT amplifier are equal. When is the BJT advantageous? Use $I_o = 150\mu\text{A}$, and $V^* = 200\text{mV}$, $\gamma = 1.5$, and $\beta = 250$. Ignore flicker noise.