University of California, Berkeley *Spring 2006*
EECS 240 *Prof. A. Niknejad*

Problem Set 2
Due Thursday February 2, 2006

For the following questions, use the EECS 240 180nm CMOS process technology.

1. Design a PMOS common-source stage driving a 5pF load with 100MHz unity-gain bandwidth. Choose L large enough to obtain a peak gain of 75 and $V^* = 200\text{mV}$. You may use an ideal current source. Verify your design with SPICE. Using SPICE plot the small-signal gain as a function of the output DC level.

2. What is the minimum drain current to bias a 10/0.18 NMOS and PMOS device in strong inversion? For the device to be clearly in strong inversion, $V^* > 150\text{mV}$.