Problem Set 1
Due Thursday January 26, 2006

For the following questions, use the EECS 240 180nm CMOS process technology. Unless otherwise specified, use a minimum sized transistor with $W = 10\mu$. For some questions, you need to access internal device parameters such as g_m or V_T. Each simulator has a specific way of doing this. Plot the results for all process corners.
With SpectreRF, you can DC sweep any parameter but to access the DC parameters in a sweep, you need a statement "`save MX:all`" in your netlist, where `MX` is the transistor in question. The results of the sweep can be accessed through the results browser (not the waveform calculator).

1. Plot the threshold voltage of an NFET and PFET as a function of channel length L. What causes the variation in V_T.

2. (NFET) Plot the g_m versus V_{GS} of the transistor on a linear and log scale. Compare the results with a simple square law and sub-threshold model. Bias the transistor with $V_{GS} = V_{DS}$. What is the μC_{ox} for the transistor?

3. (NFET) Plot g_m/I_D of the transistor versus V_{GS}. Compare the results to simple model equations. Where is the best point to operate the transistor to minimize power? Bias the transistor with $V_{DS} = V_{GS}$.

4. Plot the total gate capacitance of a NFET configured as a MOS capacitor. Vary the V_G to cover accumulation, depletion, and inversion. How does this compare to a simple CV model?

5. Plot the output resistance r_o and DC gain $g_m r_o$ versus V_{DS} for an NFET and PFET. To maintain a DC gain of 80% of the peak value, what is the allowed output swing. Bias the transistor with $V_{GS} - V_T = 200\text{mV}$. What is λ? Explain a possible reason for teh difference between the NFET and PFET.

6. (NFET and PFET) Plot the device f_T versus V_{GS}. For $V_{GS} - V_T = 200\text{mV}$, plot the f_T versus L.