Lecture 22:
Si Microwave Amplifier Survey

Ali Niknejad

EECS 217

A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier

Derek K. Shaeffer, *Student Member, IEEE*, and Thomas H. Lee, *Member, IEEE*

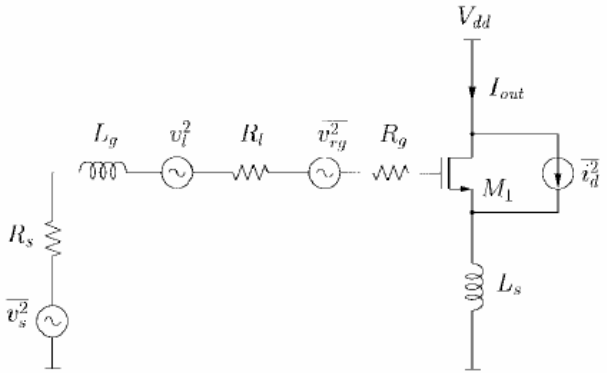


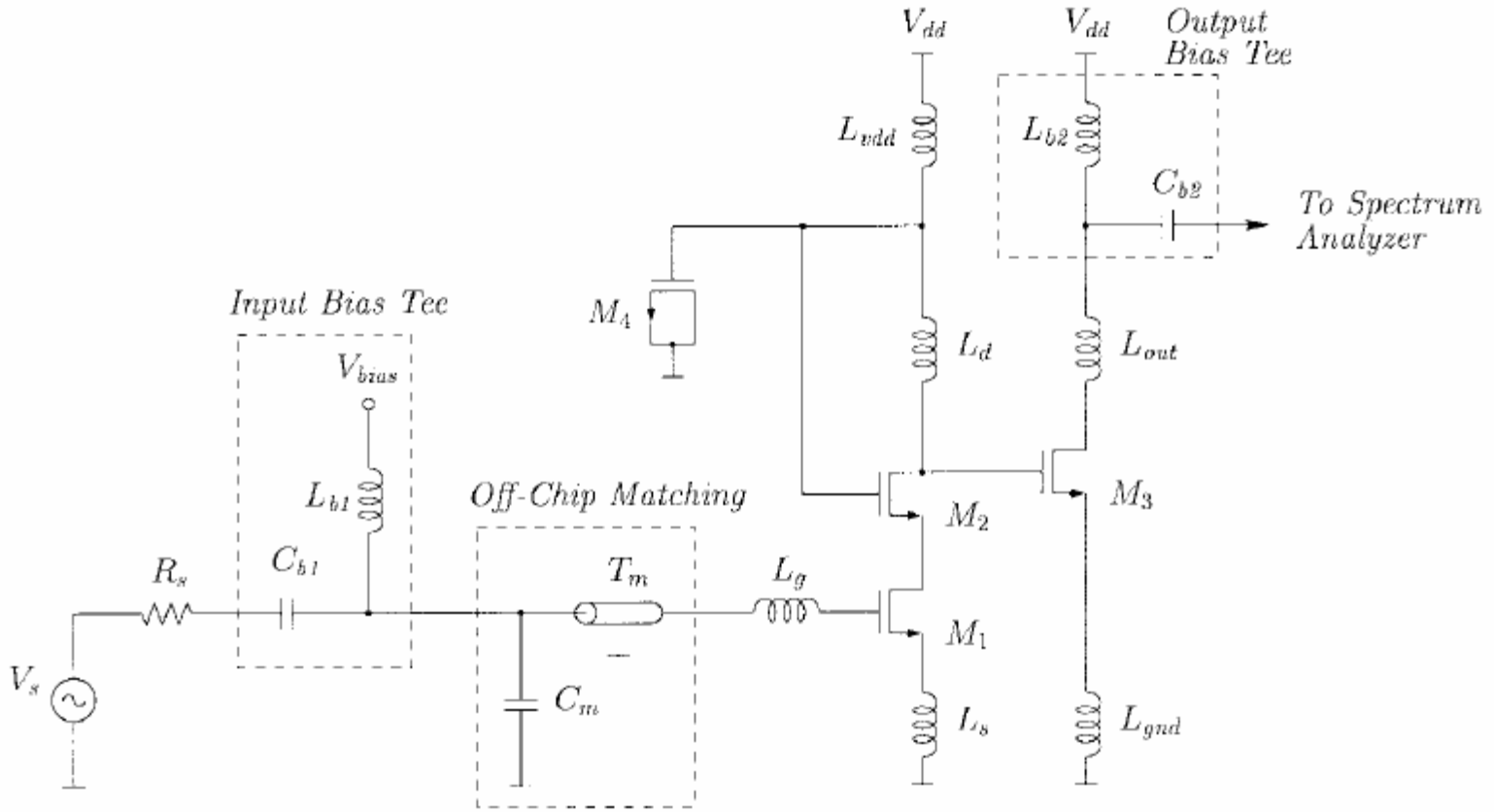
Fig. 4. Equivalent circuit for input stage noise calculations.

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}\left(\frac{\omega_0}{\omega_T}\right).$$

$$\chi = \kappa + \xi = 1 + 2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1 + Q_L^2).$$

$$F_{min,G_m} = 1 + \sqrt{\frac{4}{5}\delta\gamma}\left(\frac{\omega_0}{\omega_T}\right)\left\{|c| + \sqrt{1 + \frac{\delta\alpha^2}{5\gamma}}\right\}$$
$$\geq 1 + 1.33\left(\frac{\omega_0}{\omega_T}\right).$$

$$F_{min,P_D} \approx 1 + 2.4\frac{\gamma}{\alpha}\left(\frac{\omega_0}{\omega_T}\right) \geq 1 + 1.62\left(\frac{\omega_0}{\omega_T}\right)$$



$$W_{M_1,opt,P_D} = \left[\frac{2}{3}\omega_0 L C_{ox} R_s Q_{L,opt,P_D}\right]^{-1} \approx 496\,\mu\text{m} \quad (53)$$

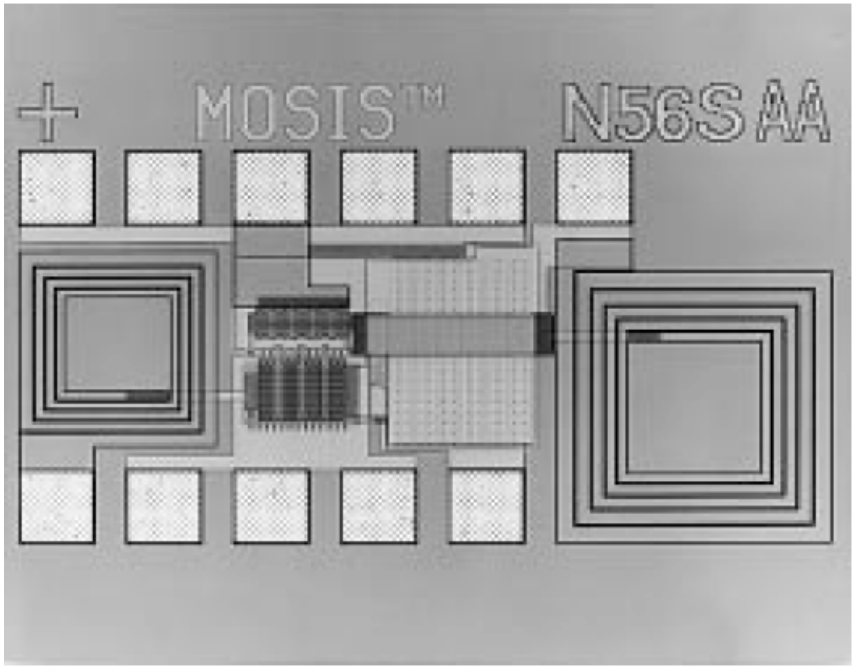


TABLE II
LNA PERFORMANCE SUMMARY

Frequency	1.5 GHz
Noise Figure	3.5 dB
S21	22 dB
IP3 (Output)	12.7 dBm
1 dB Compression (Output)	0 dBm
Supply Voltage	1.5 V
Power Dissipation	30 mW
(First Stage)	7.5 mW
Technology	0.6-μm CMOS
Die Area	0.12 mm2

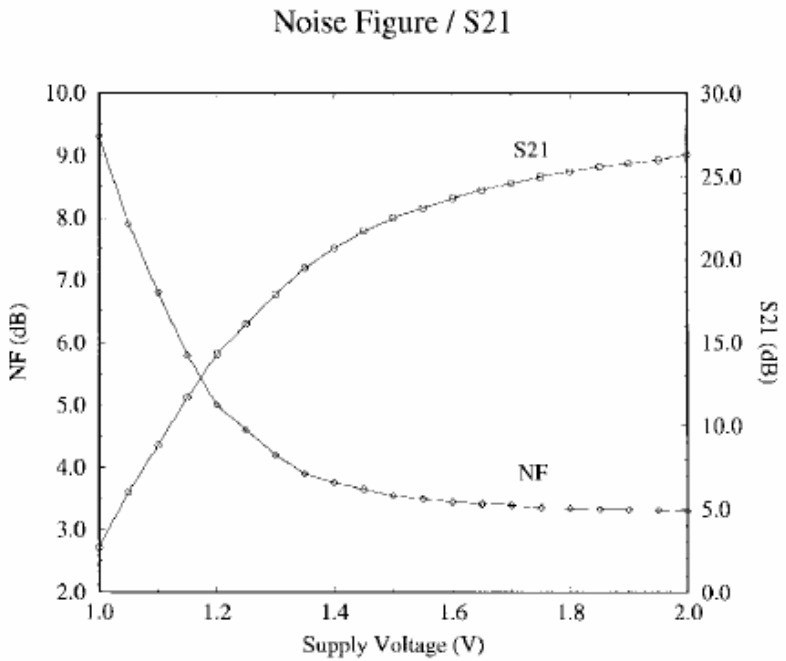
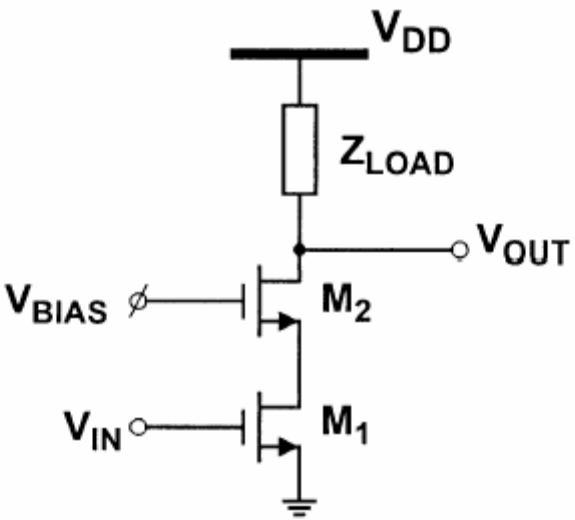


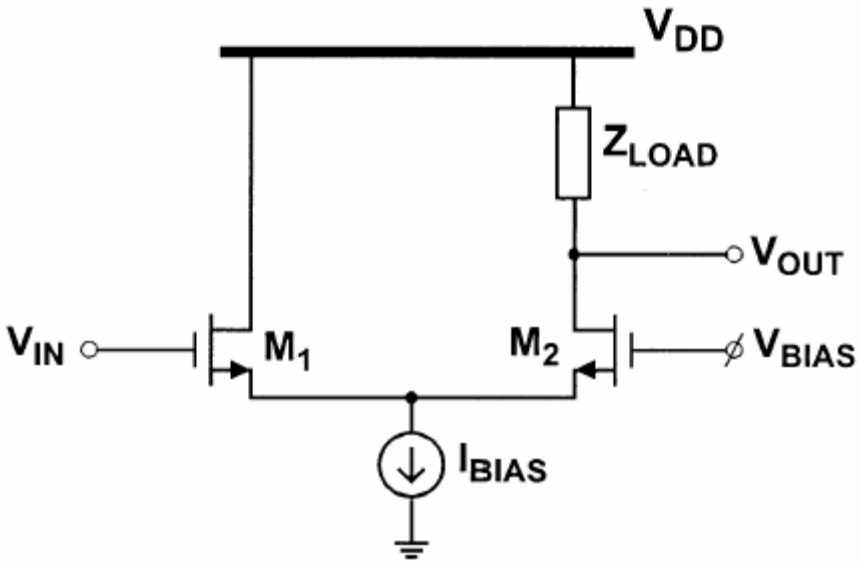
Fig. 19. Noise figure and forward gain of the LNA.

A 1V 0.9dB NF Low Noise Amplifier for 5-6GHz WLAN in 0.18μm CMOS

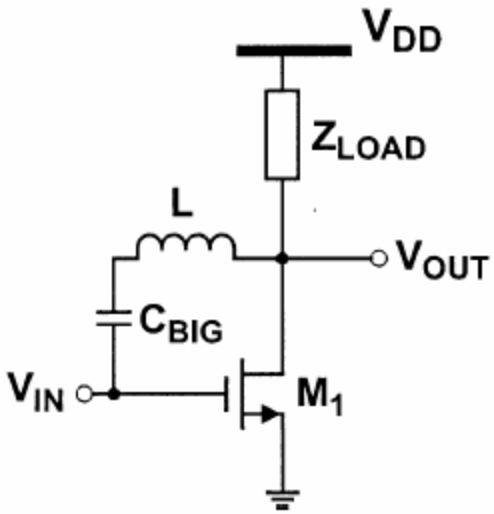
David Cassan and John Long
University of Toronto, Toronto, Canada[1]

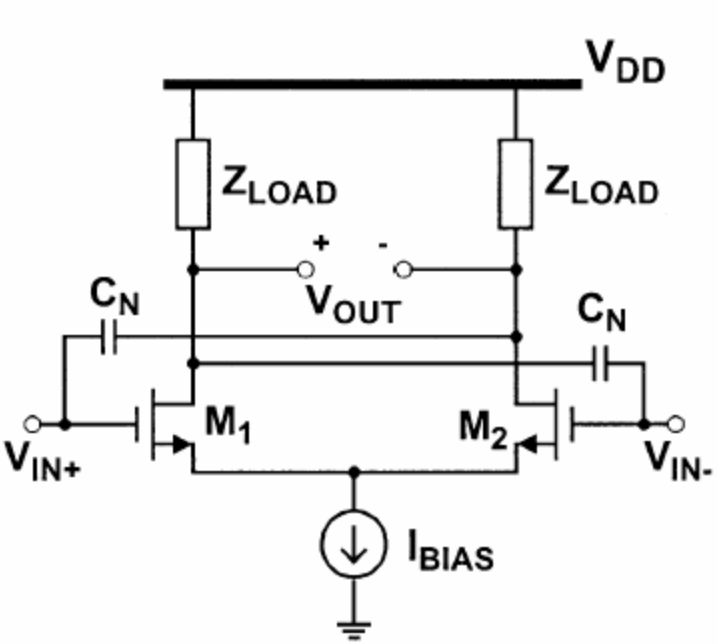

VDD
ZLOAD
VOUT
VBIAS
M2
VIN
M1

(a)

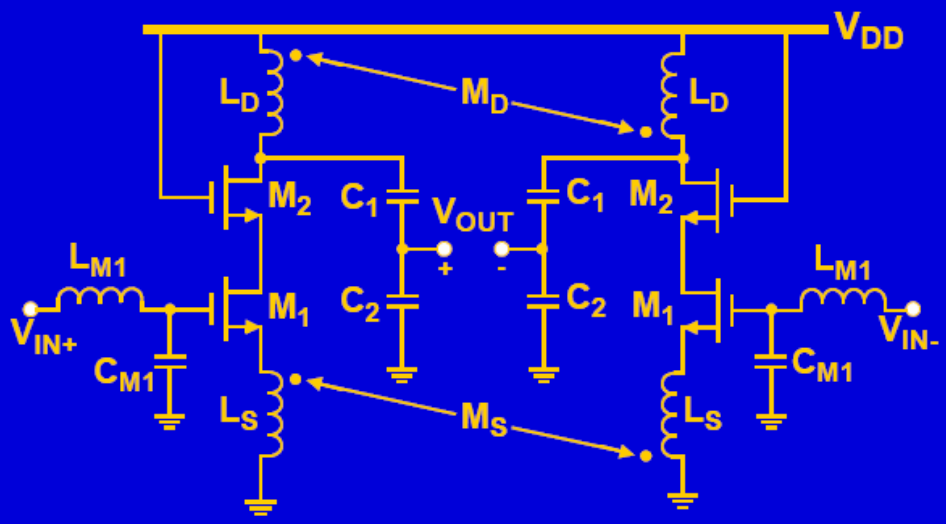

VDD
ZLOAD
VOUT
VIN
M1
M2
VBIAS
IBIAS

(b)


VDD
ZLOAD
L
VOUT
CBIG
VIN
M1

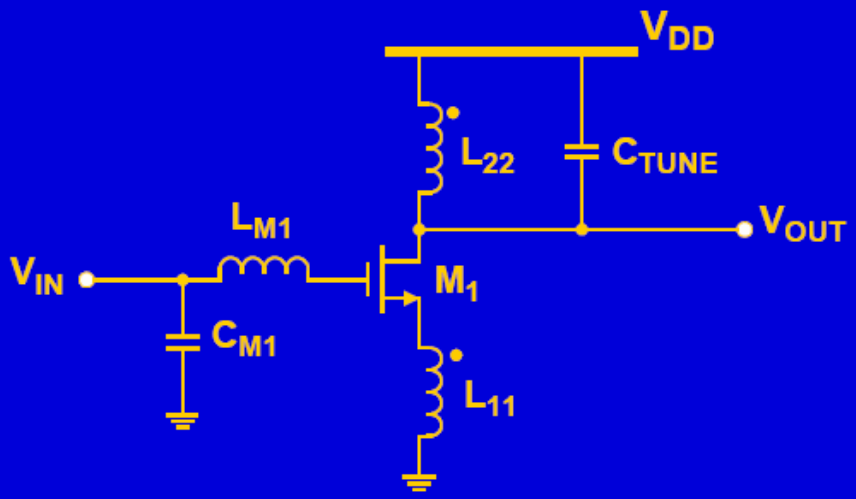

VDD
ZLOAD
ZLOAD
+
-
CN
VOUT
CN
M1
M2
VIN+
VIN-
IBIAS

Cascode LNA

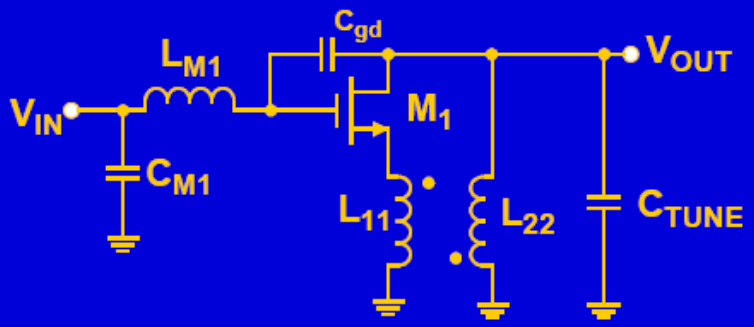


- M_2 improves reverse isolation and suppresses Miller multiplication of C_{gd} of M_1
- 6mA drain current required for IIP3 > 0dBm from 1.8V supply
- L_S and width of M_1 optimized for minimum noise figure

Transformer-Feedback LNA



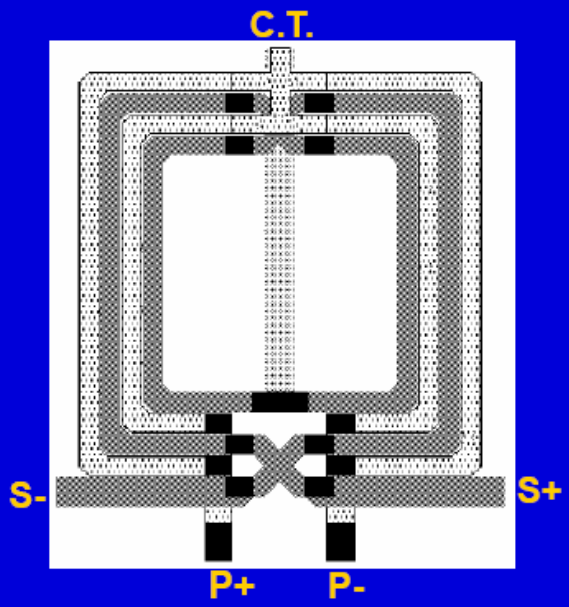
(a) Single-ended schematic



(b) Small-signal equivalent

- Transformer (L_{11} and L_{22}) is inverting for RF signals
- Full supply voltage across transistor (i.e., $V_{DS} = V_{DD}$)

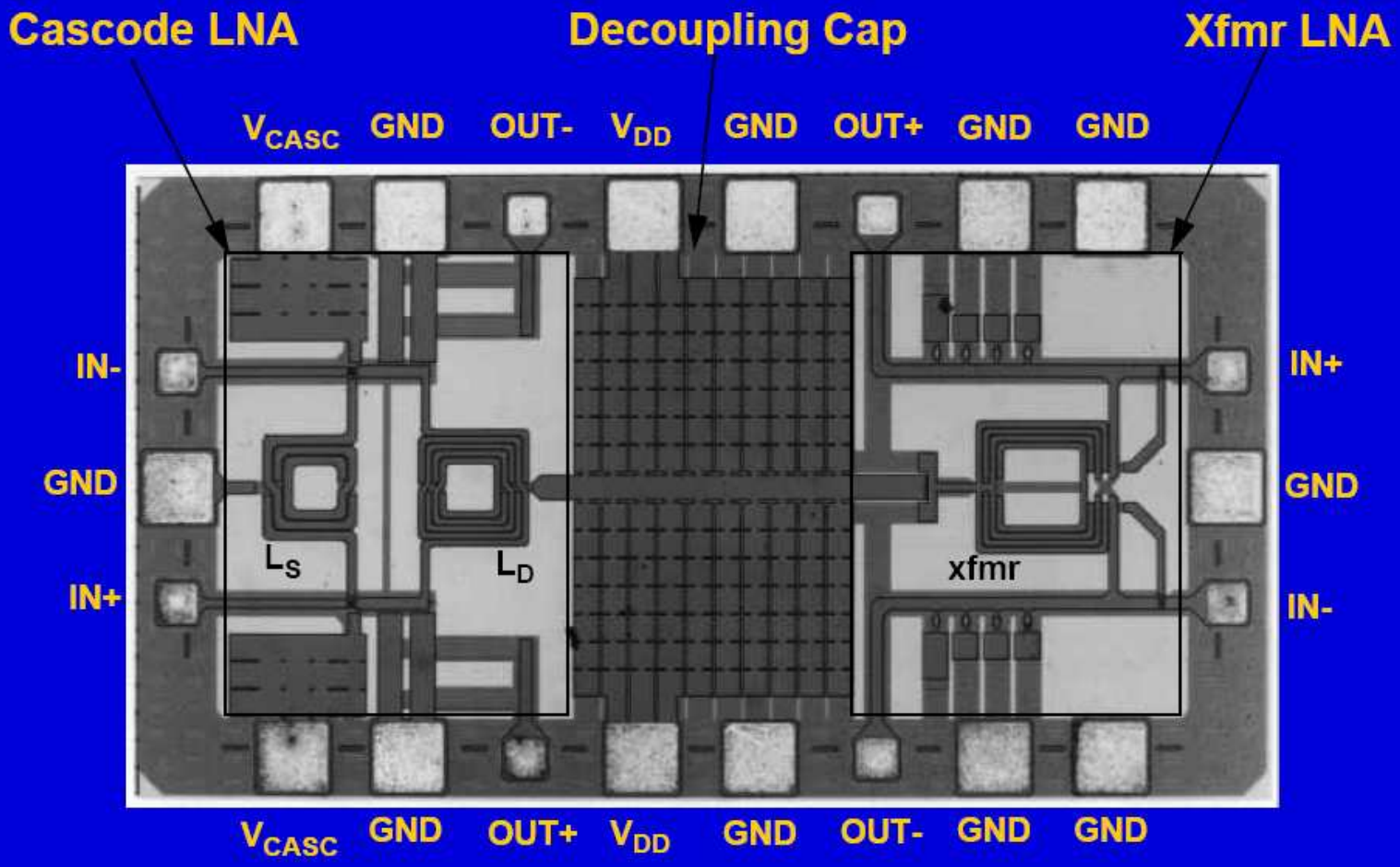
Monolithic Transformer Design



- Θ outer diameter = 170um
- Θ line width = 8um
- Θ line spacing = 1um

Electrical Parameter	Value
Turns Ratio (n)	2.13
Coupling Coefficient (k)	0.58
Primary Self Inductance (L_{11})	0.16 nH
Secondary Self Inductance (L_{22})	0.70 nH
Secondary Q-Factor @ 5.75 GHz	6.1

Chip Micrograph



Summary of Results

Parameter	Measured Differential Transformer LNA	Measured Differential Cascode LNA	SiGe single-ended Transformer LNA [Long96]	CMOS Differential Cascode LNA [Liu00]
Frequency	5.75GHz	5.75GHz	2.4GHz	5.15GHz
Transducer Power Gain (S_{21})	14.2dB	13.9dB	10.5dB	16dB
Noise Figure	0.9dB	1.8dB	0.95dB	2.5dB
IIP3	0.9dBm	4.2dBm	-4.5dBm	-11.3dBm*
Supply Voltage	1.0V	1.8V	1.0V	3.0V
Power Dissipation	16mW	21.6mW	2.5mW	48mW
Technology	0.18 μm CMOS	0.18 μm CMOS	0.50 μm SiGe HBT	0.25 μm CMOS

*value quoted for receive path (LNA+mixer). LNA linearity must be at lest this value

Brief Papers

A 24-GHz CMOS Front-End

Xiang Guan, *Student Member, IEEE,* and Ali Hajimiri, *Member, IEEE*

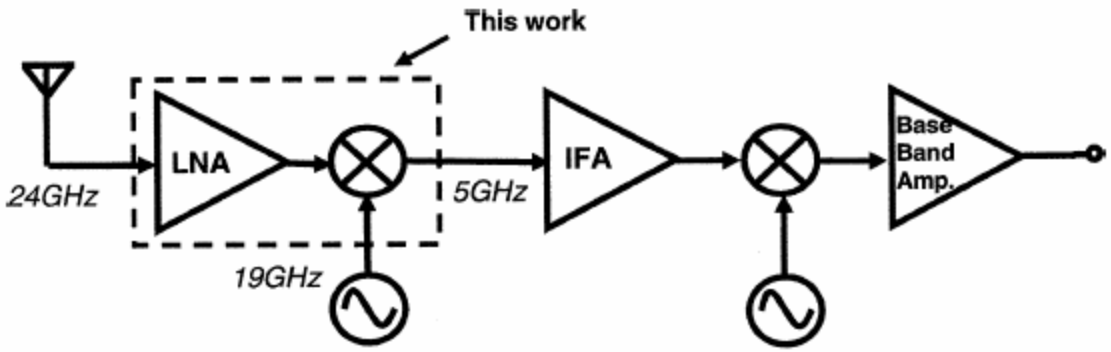
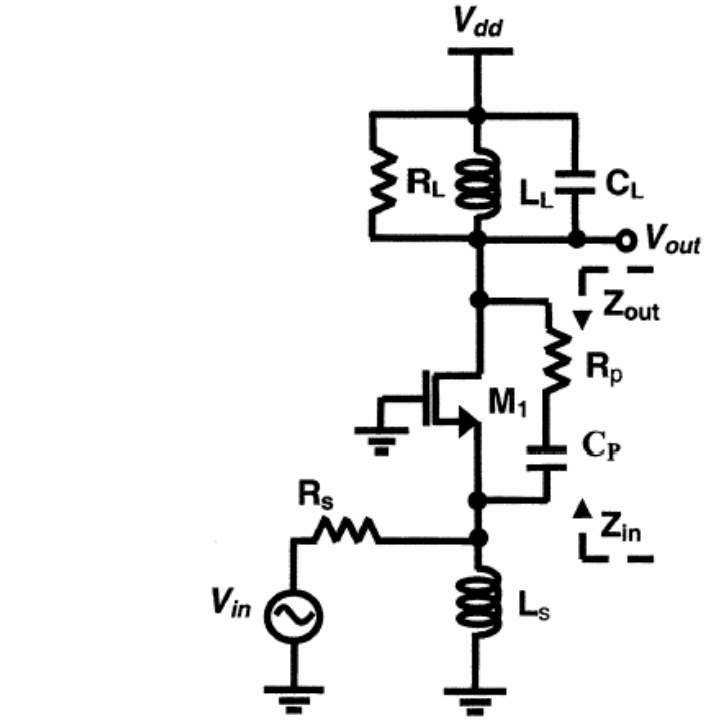
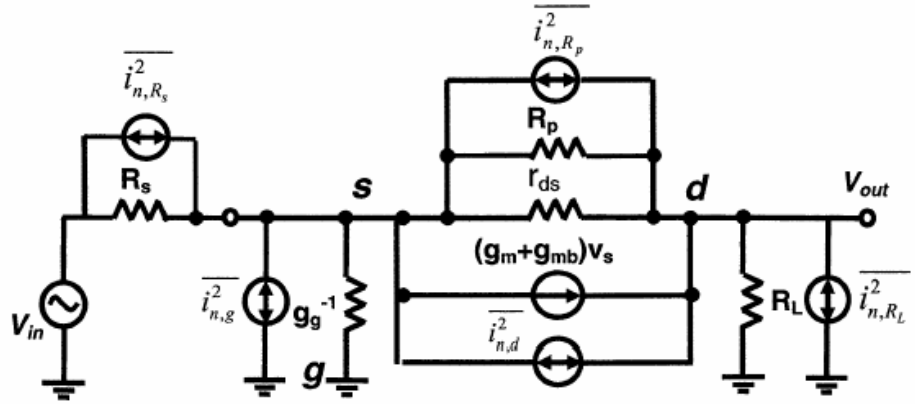


Fig. 1. 24-GHz receiver.



(a)



(b)

Fig. 2. Common-gate with resistive feedthrough LNA. (a) Schematic. (b) Small-signal equivalent circuits.

$$Z_{\text{in}} = \left(\frac{1 + g_m R_f (1+\chi)}{R_f + R_L} + \eta(\omega_0) g_m \right)^{-1} \tag{7}$$

$$F_{\text{CGRF,min}} \approx 1 + \frac{\gamma}{1+\chi} \left(\sqrt{\frac{4\delta}{5\gamma}} \left(\frac{\omega_0}{\omega_T} \right) + \frac{2}{5(1+\chi)} \left(\frac{\omega_0}{\omega_T} \right)^2 \right). \tag{12}$$

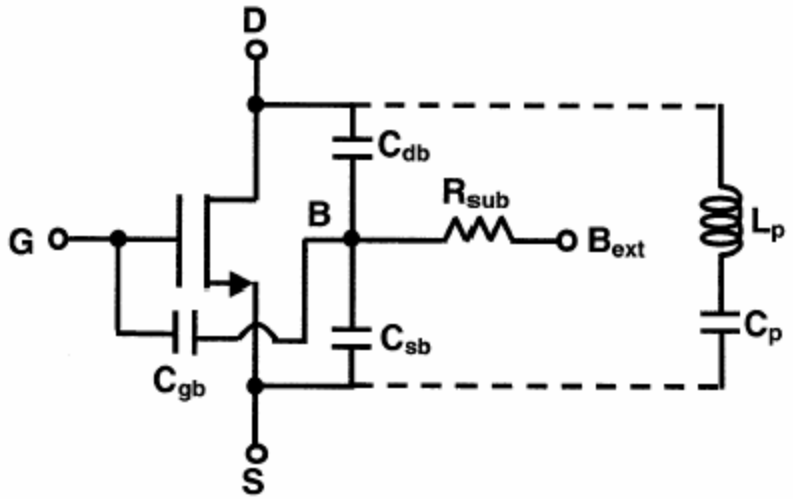
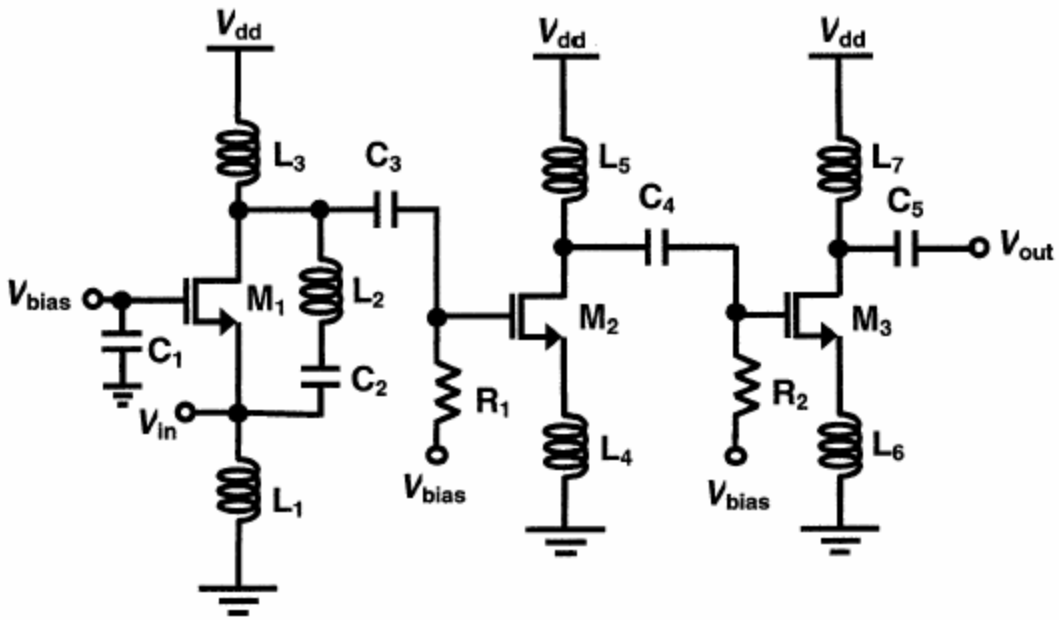


Fig. 3. Reducing substrate coupling by using parallel inductor.



(a)

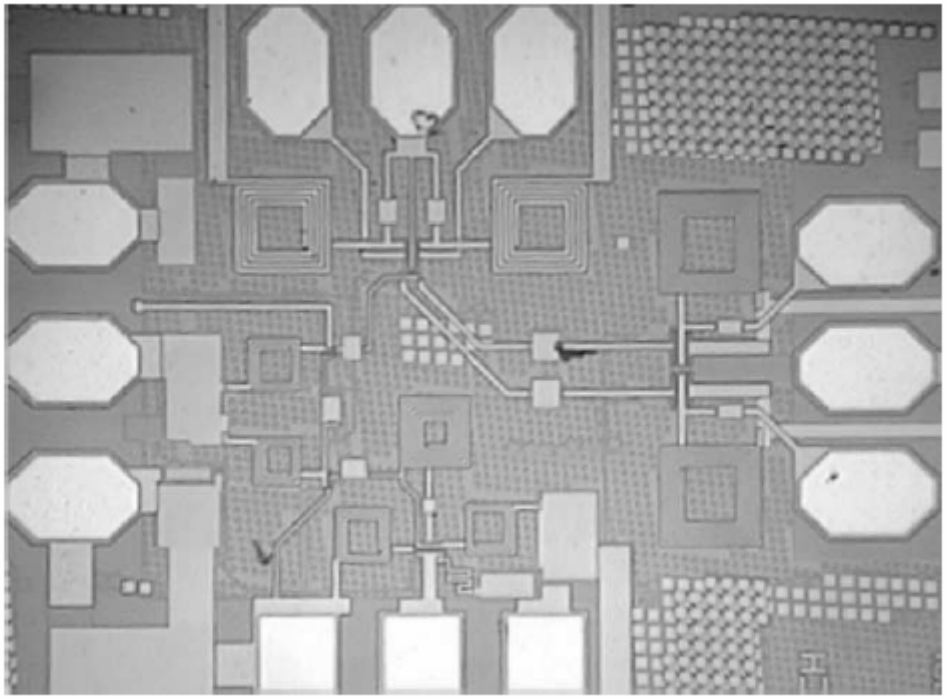
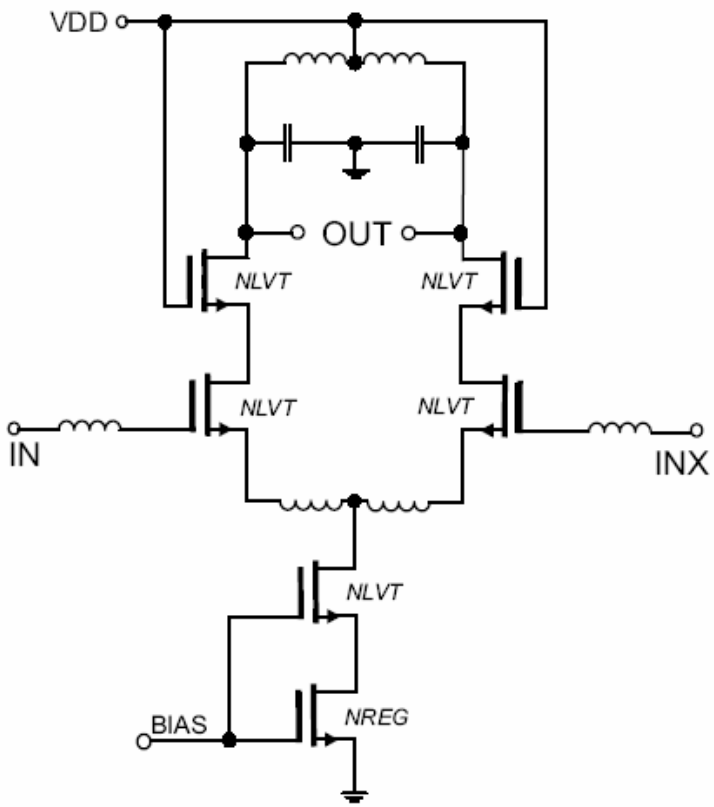


Fig. 5. Die micrograph.

Parameters	Overall Front-end	LNA
S_{11}	-21 dB	-21 dB
S_{22}	-10 dB	--
Peak Frequency	21.8 GHz RF	21.8 GHz RF
Power Gain	27.5 dB	15 dB
Voltage Gain	35.7 dB	--
Noise Figure	7.7 dB	6 dB
1-dB Compression Point	-23 dBm	--
Image Rejection	31 dB	--
Current Consumption	43 mA	16 mA
Supply Voltage	1.5 V	1.5 V
Chip Area	0.4 x 0.5mm^2	0.2 x 0.25 mm^2

An Integrated 17 GHz Front-End for ISM/WLAN Applications in 0.13 μm CMOS

C. Kienmayer [1,2], R. Thüringer [1,2], M. Tiebout [2], W. Simbürger [2], A. L. Scholtz [1]



Power supply	1.5 V
Total power consumption	70 mW
LNA power consumption	5.2 mW
Mixer power consumption	27 mW
LO-Driver power consumption	12 mW
IF-Amplifier power consumption	25.8 mW
IF frequency	3.4 GHz
Power Gain	34.7 dB
Noise Figure SSB	6.6 dB
Input compression point	-39 dBm
Input IP3	-34.4 dBm
3 dB Bandwidth	200 MHz
Die Area	0.88mm^2
Technology	0.13 μm standard CMOS

Fig. 2. Simplified schematic diagram of the LNA.

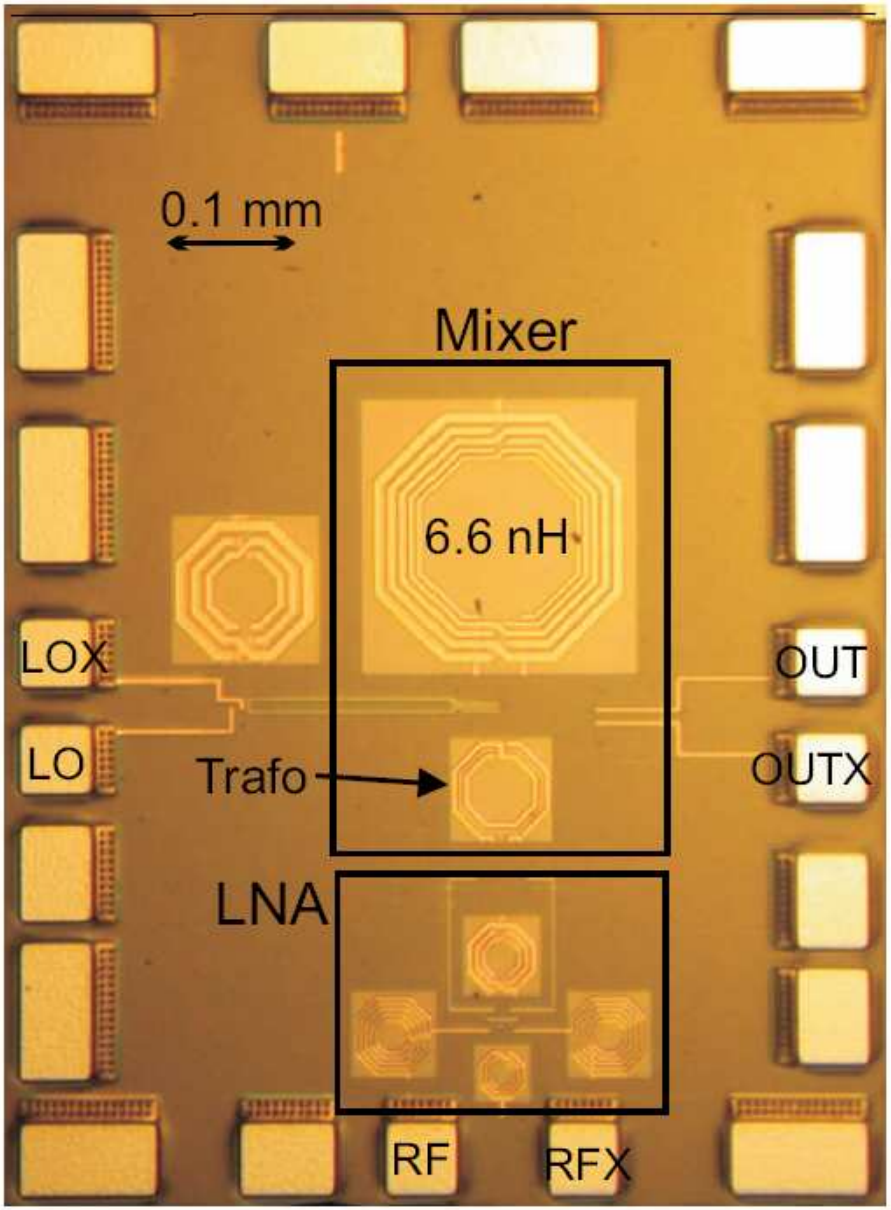


Fig. 5. Receiver front-end chip photograph (Die size 800 μm x 1100 μm)

26–42 GHz SOI CMOS Low Noise Amplifier

Frank Ellinger, *Member, IEEE*

TABLE I
COMPARISON WITH STATE-OF-THE-ART MICROWAVE AND MILLIMETER-WAVE LNAs

Ref.	Technology/f_t	f_{center}	S_{21}	NF	P_{1dB}	V_{dc}	I_{dc}
III/V							
8	70nm InP PHEMT/500GHz	160GHz	9dB	6dB	n.a.	1.4V	33mA
9	150nm InP PHEMT/n.a	26.5GHz	14.5dB	1.7dB	n.a.	n.a.	n.a
SiGe HBT							
10	SiGe HBT/47GHz	16GHz	14.5dB	3.8dB	n.a.	1.5V	1.5mA
11	SiGe HBT/155GHz	19GHz	26dB	2.2dB	n.a.	3V	8.7mA
5	SiGe HBT/80GHz	24GHz	10dB	9dB	n.a.	3.6V	46mA
CMOS							
12	180nm CMOS/n.a.	13GHz	4.9dB	4.7dB	n.a.	1.8V	5.4mA
13	180nm CMOS/50GHz	16GHz	9dB	4dB	n.a.	3V	15.5mA
6	180nm CMOS/54GHz	21.8GHz	15dB	6dB	-8dBm	1.5V	16mA
7	100nm SOI CMOS/100GHz	23.8GHz	7.3dB	10dB	0dBm	1.5V	53mA
This work	**90 nm SOI CMOS/149GHz**	**35GHz**	**11.9dB**	**3.6dB**	**4dBm**	**2.4V**	**17mA**
		40GHz	**9.5dB**	**4dB**			

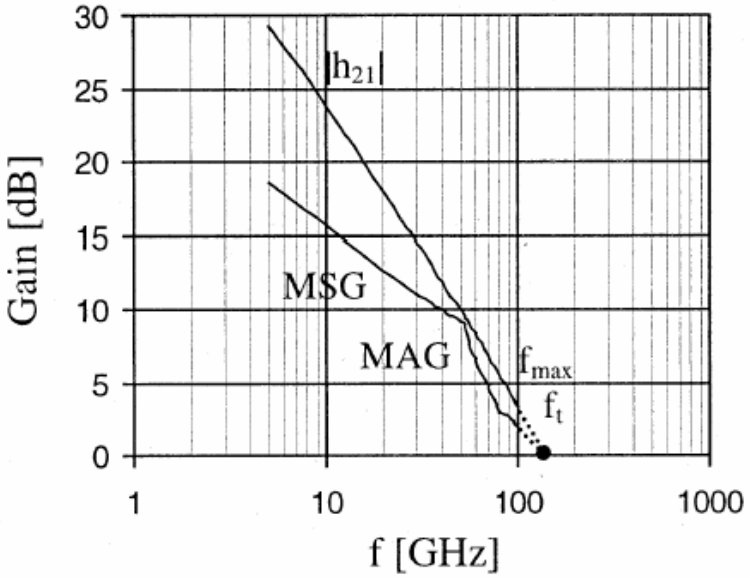


Fig. 1. Measured $f_{\max}$ and f_t versus frequency at $V_{\rm gs} = 0.5$ V, $V_{\rm ds} = 1$ V and $I_{\rm ds} = 16$ mA corresponding to a current density of 0.25 mA/μm.

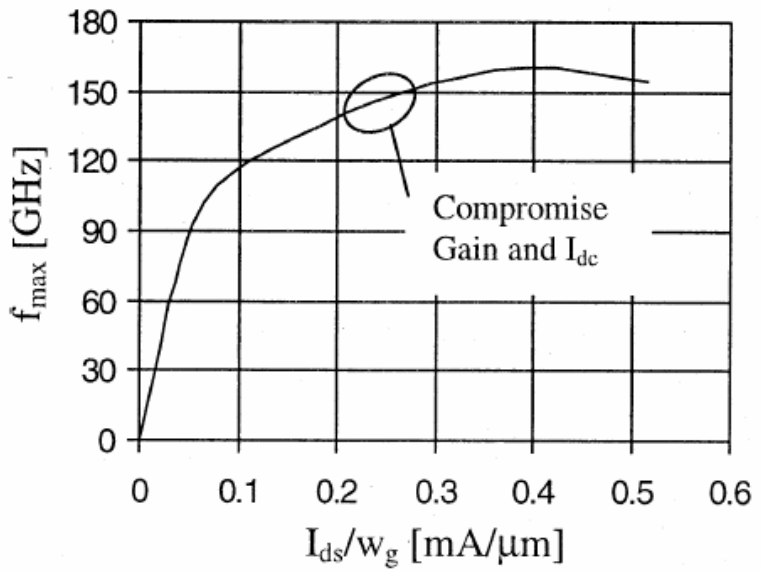


Fig. 2. Measured $f_{\max}$ at $V_{\rm ds} = 1$ V versus current density.

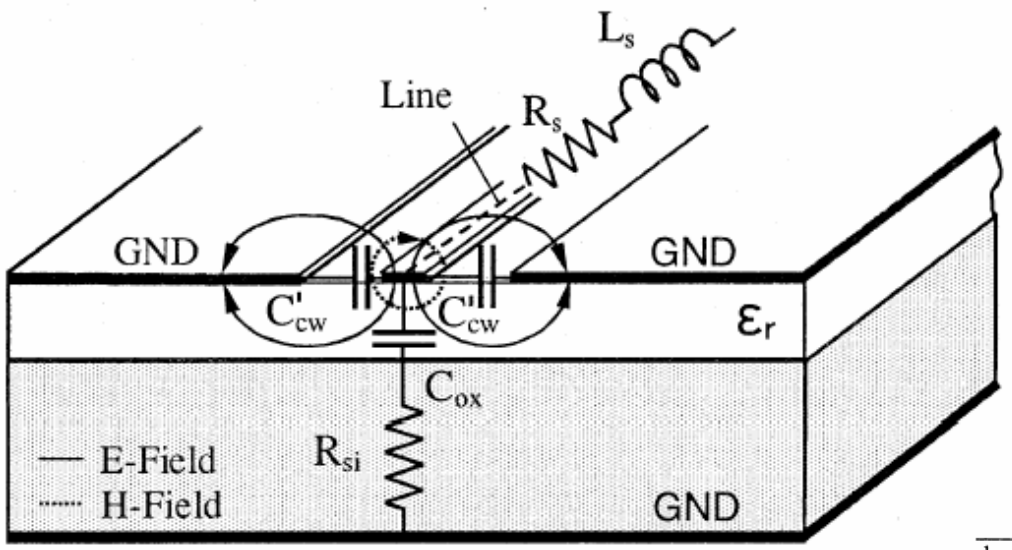


Fig. 4. Simplified cross view of transmission line, $C'_{\rm cw} = 0.5\ C_{\rm cw}$.

TABLE II
ELEMENT VALUES OF SCALABLE INDUCTIVE TRANSMISSION LINE

l_n	L_s	R_s	C_{ox}	R_{si}	C_{cw}
l/1mm	0.7nH/l_n	7.2Ω l_n	50fF l_n	17Ω/l_n	27fF l_n

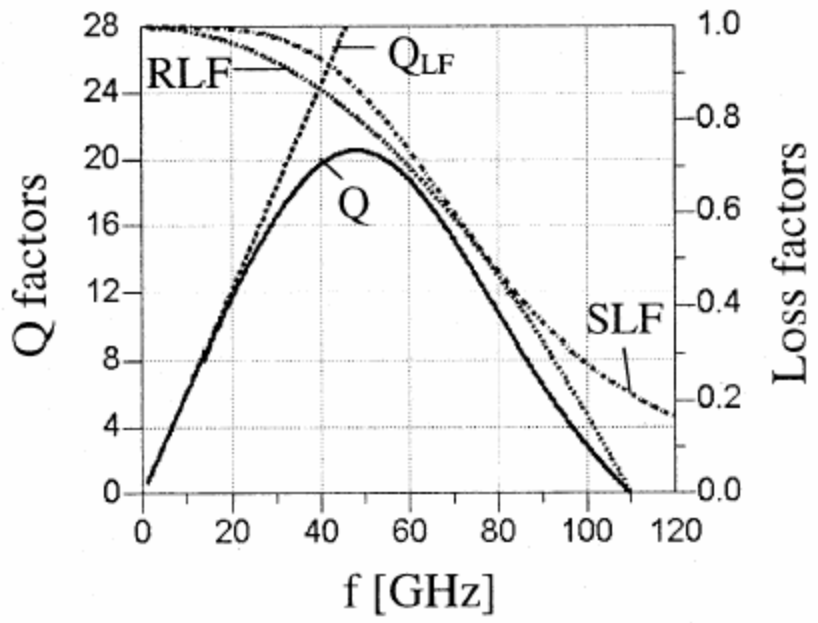


Fig. 7. Q factor, low-frequency Q factor Q_{LF}, substrate loss factor SLF, and self-resonance loss factor RLF of line with $L_s = 0.195$ nH.

$$
\begin{aligned}
Q = & \frac{\omega \cdot L_s}{R_s} \cdot \frac{R_p}{R_p + \left[\left(\frac{\omega \cdot L_s}{R_s}\right)^2 + 1\right] \cdot R_s} \\
& \cdot \left[1 - \frac{R_S^2 \cdot (C_{cw} + C_p)}{L_s} - \omega^2 \cdot L_s \cdot (C_{cw} + C_p)\right] \\
= & \, Q_{\mathrm{LF}} \cdot \mathrm{SLF} \cdot \mathrm{RLF}
\end{aligned}
$$

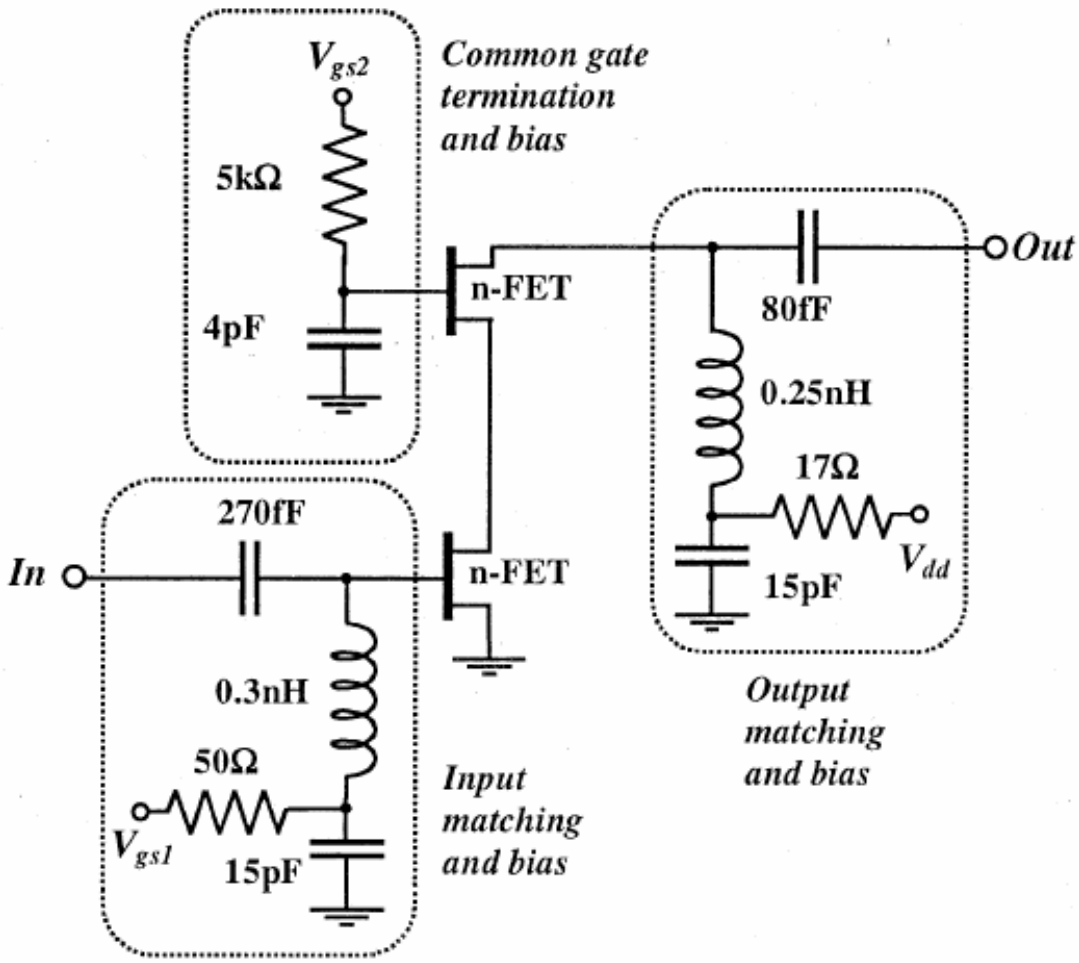
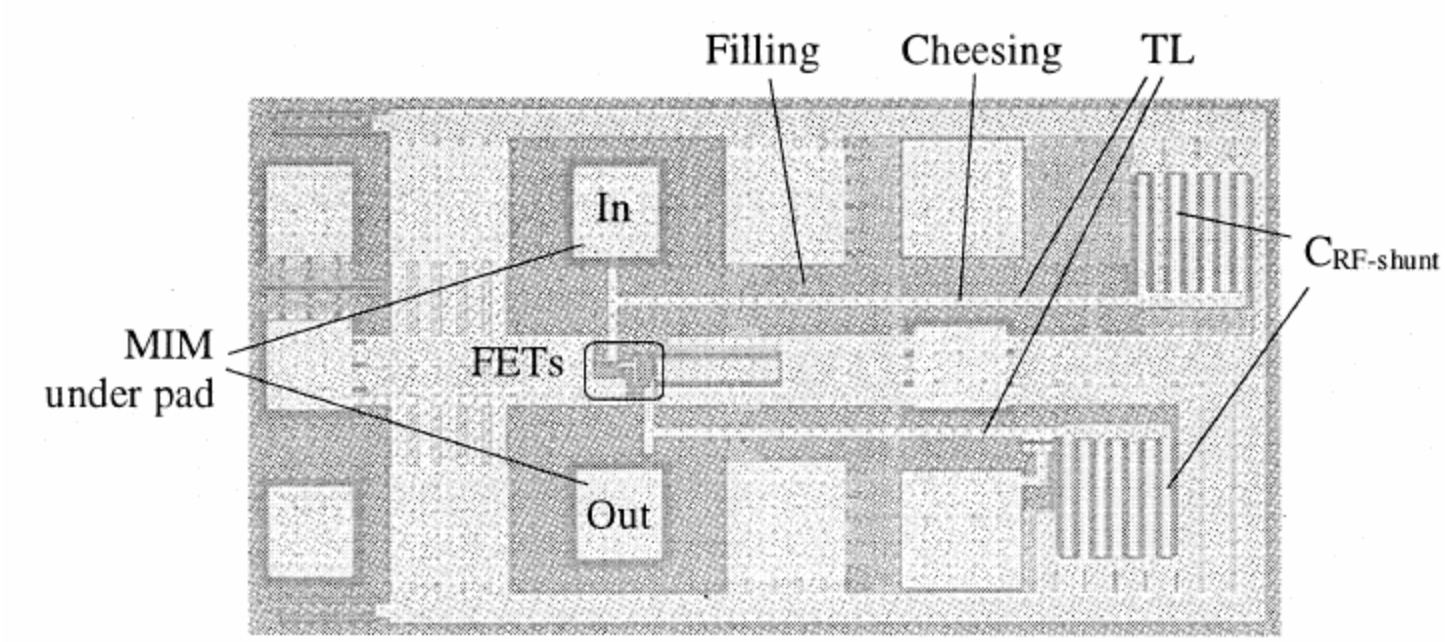


Fig. 10. Simplified equivalent circuit of the LNA.



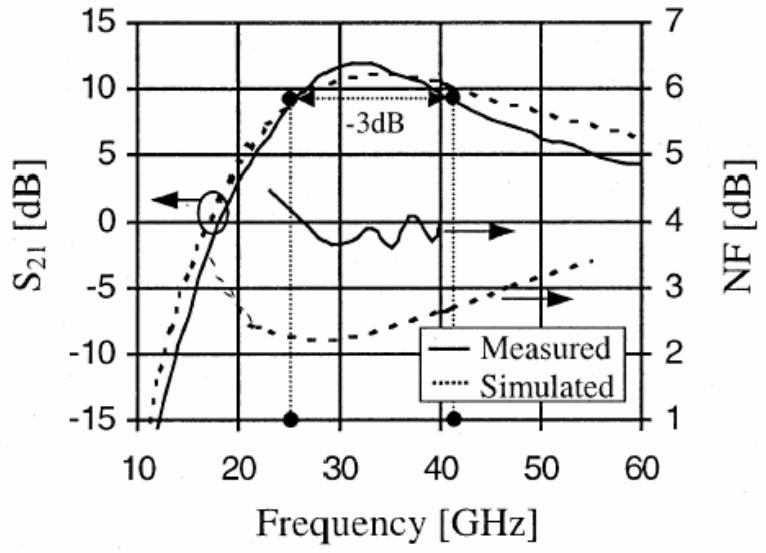
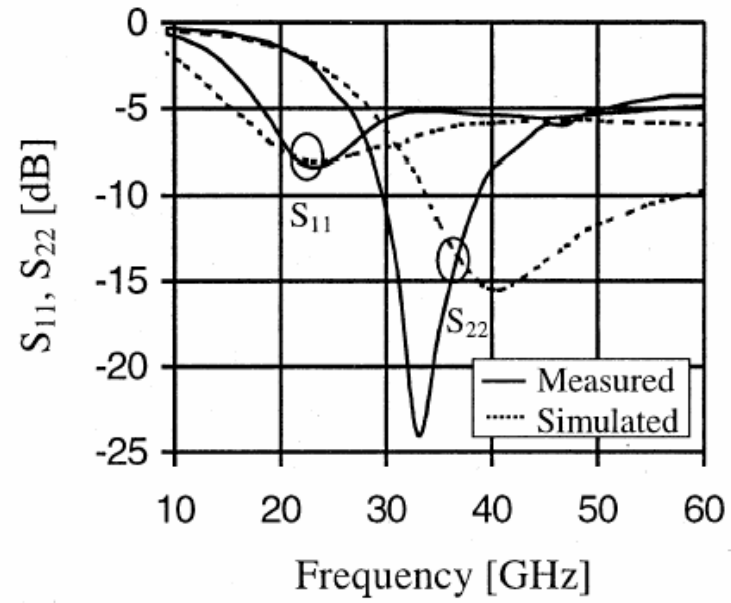


Fig. 12. Measured and simulated gain and noise figure, $V_{dc} = 2.4$ V, $I_{dc} = 17$ mA.



Measured and simulated return losses, $V_{dc} = 2.4$ V, $I_{dc} = 17$ mA.

24.5 60GHz Transceiver Circuits in SiGe Bipolar Technology

Scott Reynolds, Brian Floyd, Ullrich Pfeiffer, Thomas Zwick

IBM, Yorktown Heights, NY

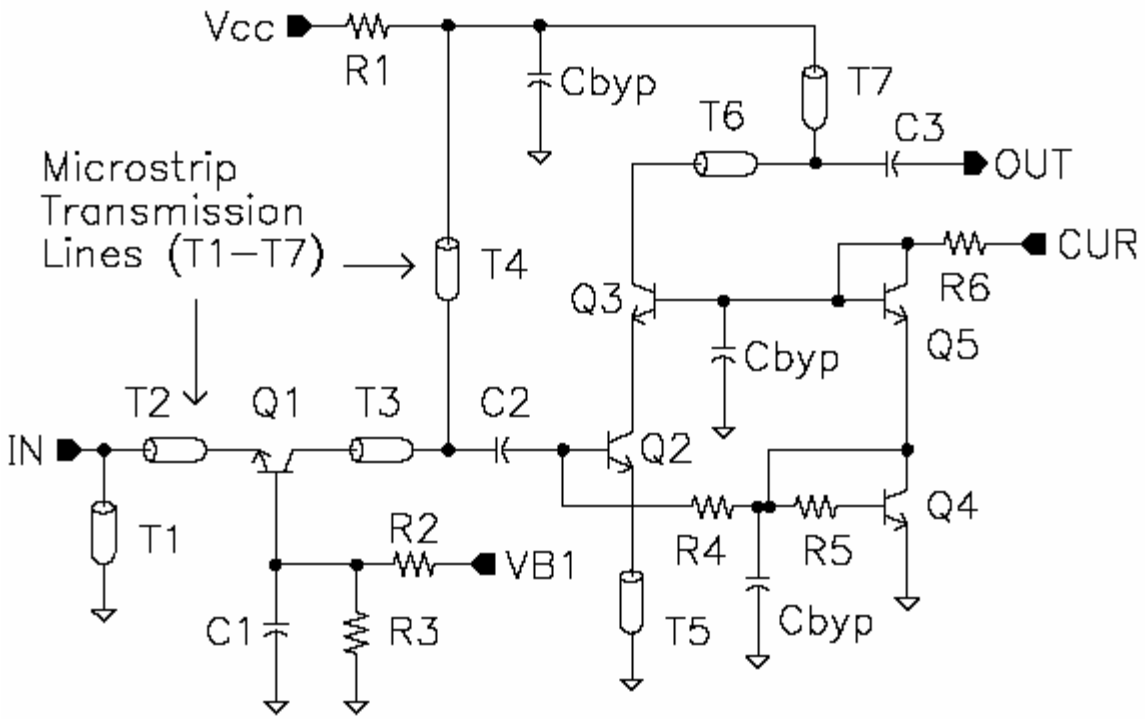
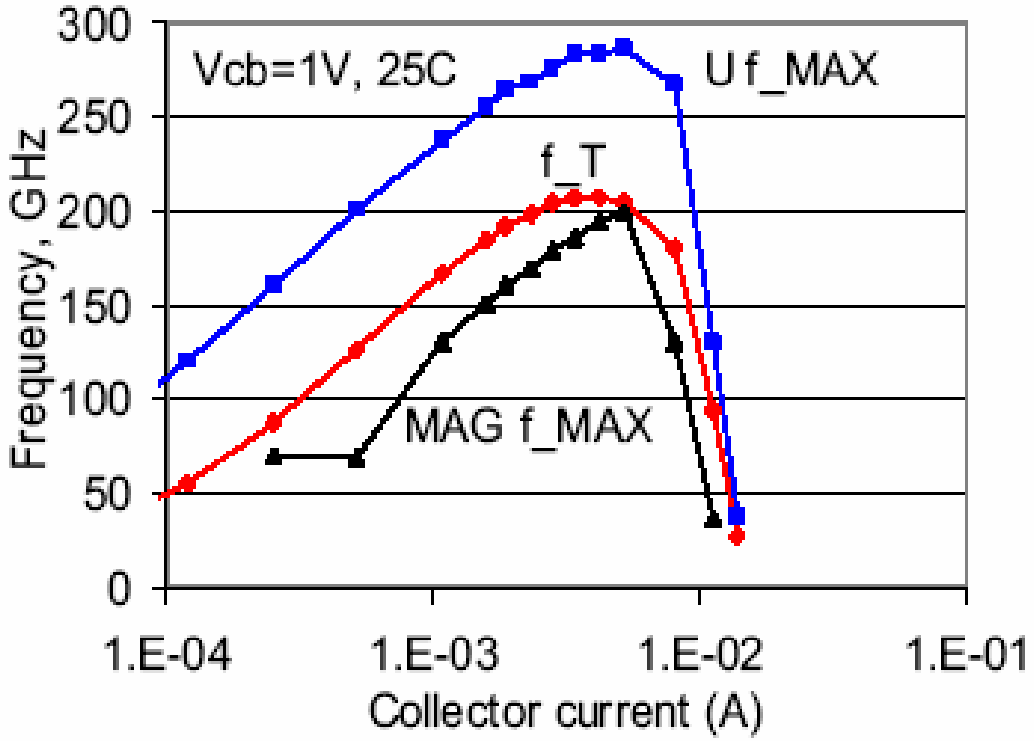
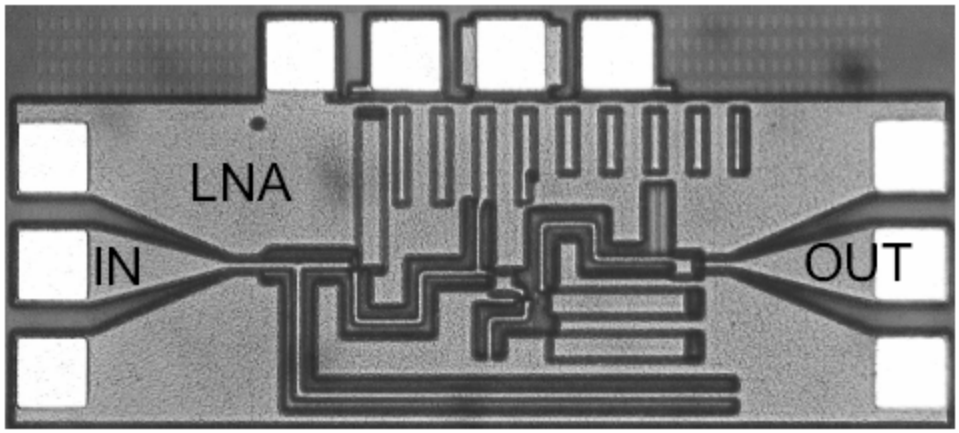


Figure 24.5.2: Schematic of 60GHz low-noise amplifier.

SiGe Bipolar Technology Features



- 0.12-µm emitter stripe
- f_T = 200 GHz
- unilateral f_{MAX} = 250 GHz
- BV_{CEO} = 1.7 V
- BV_{CBO} = 5.8 V
- 2 Cu layers, 2 thick top Al layers
- MIM capacitors
- metal-film resistors



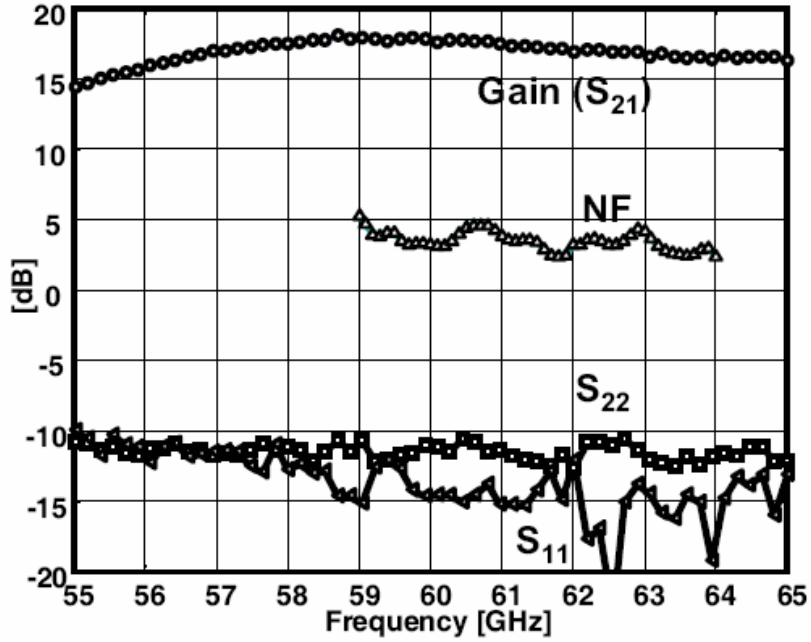


Figure 24.5.3: Measured gain, noise figure, S11, and S22 for LNA with CPW tapers.

	LNA
Freq.	61.5 GHz
Gain	17 dB
NF	4.2 dB
P1dB	-20 dBm (in)
IIP3	-8.5 dBm
IIP2	-
Psat	-
LO leakage to LNA2 input	-
S11	-14 dB
S22	-12 dB
S12	-40 dB
Supply Current	6 mA @ 1.8V

The Road to 60 GHz Wireless CMOS

Ali M. Niknejad and Robert W. Brodersen
Chinh H. Doan, Sohrab Emami, David Sobel,
Sayf Alalusi, Mounir Bohsali, Matthew Muh

Berkeley Wireless Research Center
University of California at Berkeley

Challenges and Solution

- Major Challenges:
  - High path loss at 60 GHz (relative to 5 GHz)
  - Silicon substrate is lossy – high Q passive elements difficult to realize
  - CMOS building blocks at 60 GHz
  - Need new design methodology for CMOS *mm*-wave
  - Low power baseband architecture for Gbps communication

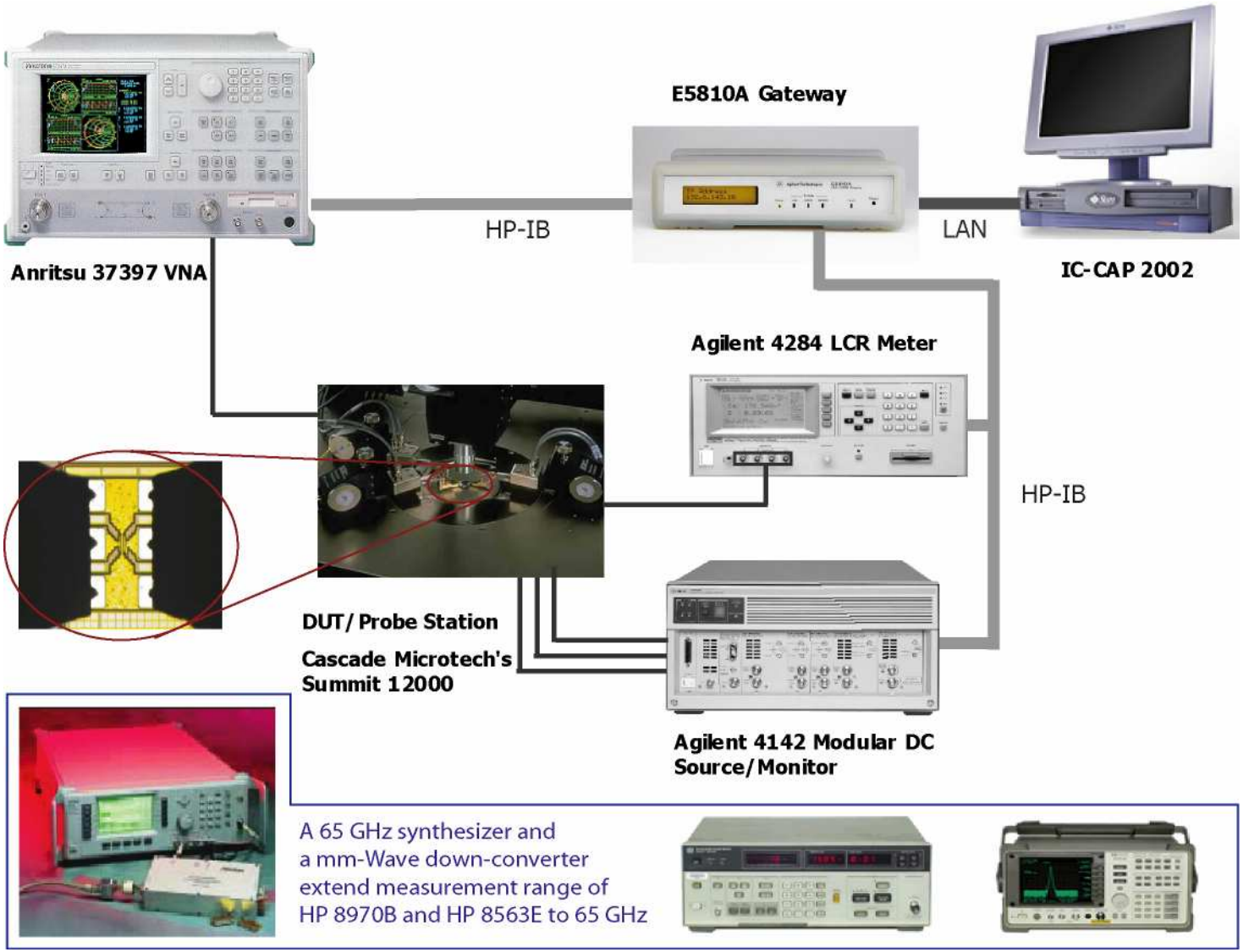
- Solution:
  - CMOS technology is inexpensive and constantly shrinking and operating at higher speeds – multiple transceivers can be integrated in a single chip
  - Antenna elements are small enough to allow integration into package
  - Beam forming can improve antenna gain, spatial diversity offers resilience to multi-path fading
  - Due to spatial power combining, individual PAs need to deliver only ~ 50 mW

Importance of Modeling at 60 GHz

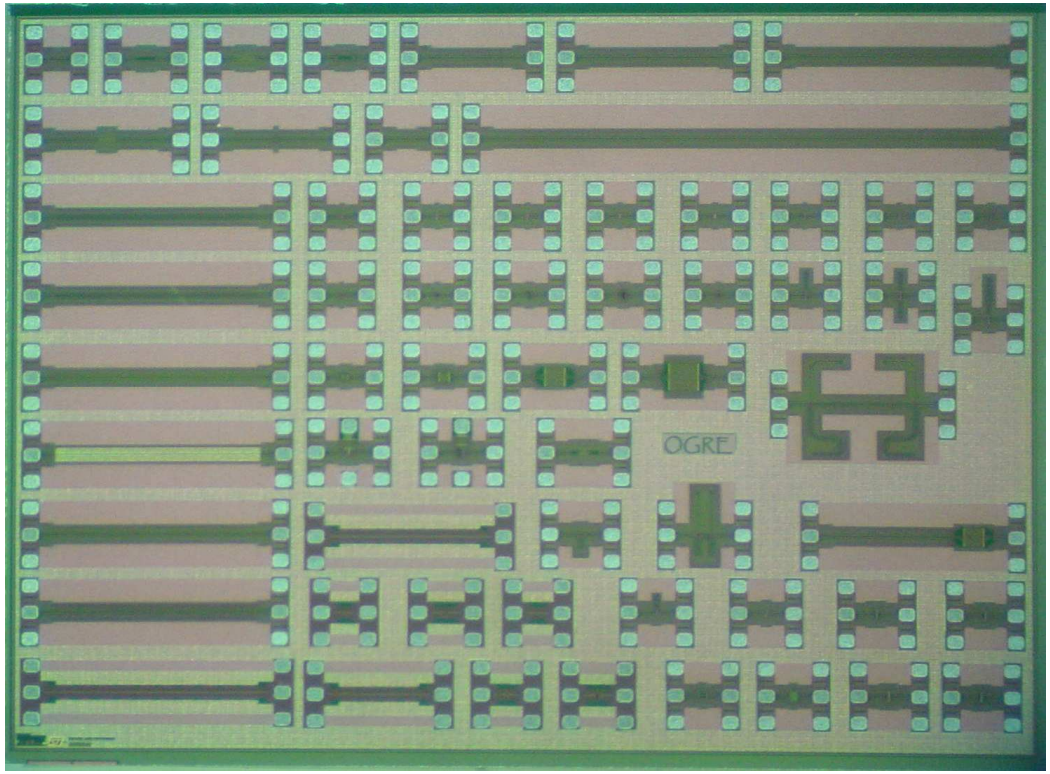
- Transistors
  - Compact model not verified near f_{max}/f_t
  - Table-based model lacks flexibility
  - Parasitics no longer negligible
  - Highly layout dependent
- Passives
  - Need accurate reactances
  - Loss not negligible
  - Scalable models desired
  - Allows comparison of arbitrary structures

Accurate models required for circuits operating near limit of process

Measurement Setup



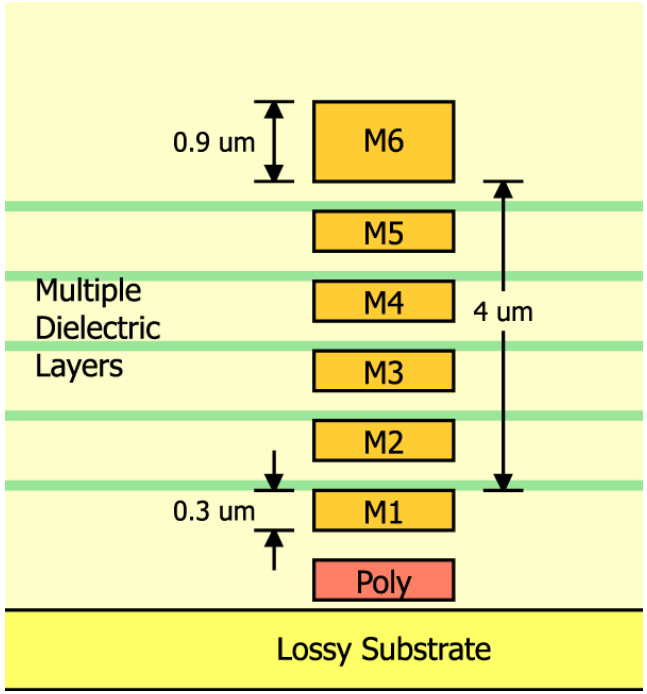
Device Test Chip

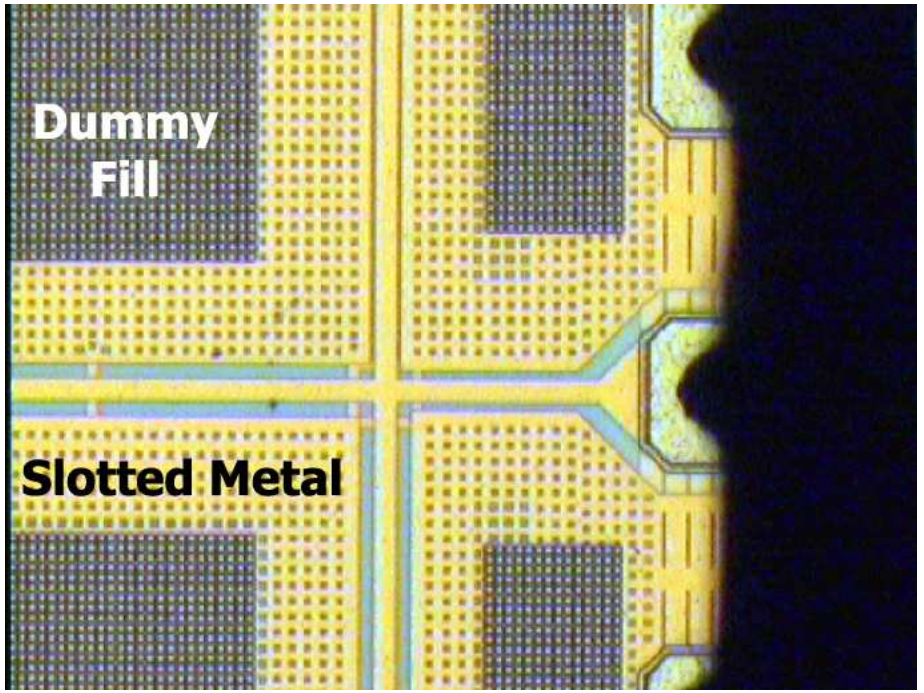


Test Chip Includes:

- Multi-line TRL calibration
- Transmission lines
  - Coplanar (CPW)
  - Microstrip
- Fingered capacitors
  - Coupling
  - Supply bypass
- Poly/N-well caps
- Passive filters
- RF NMOS layout with varying W_F, N_F

Modeling challenges for modern CMOS

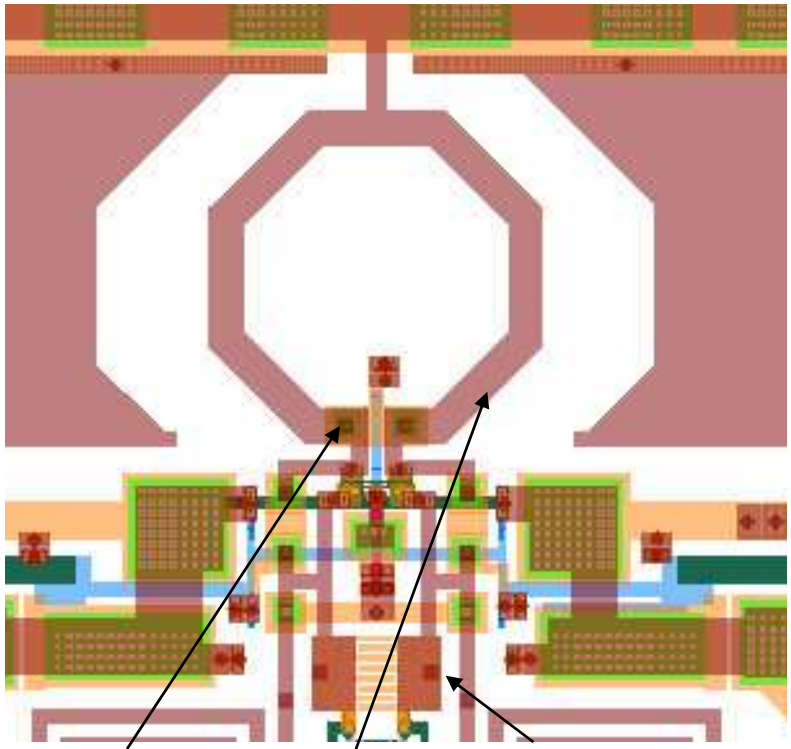


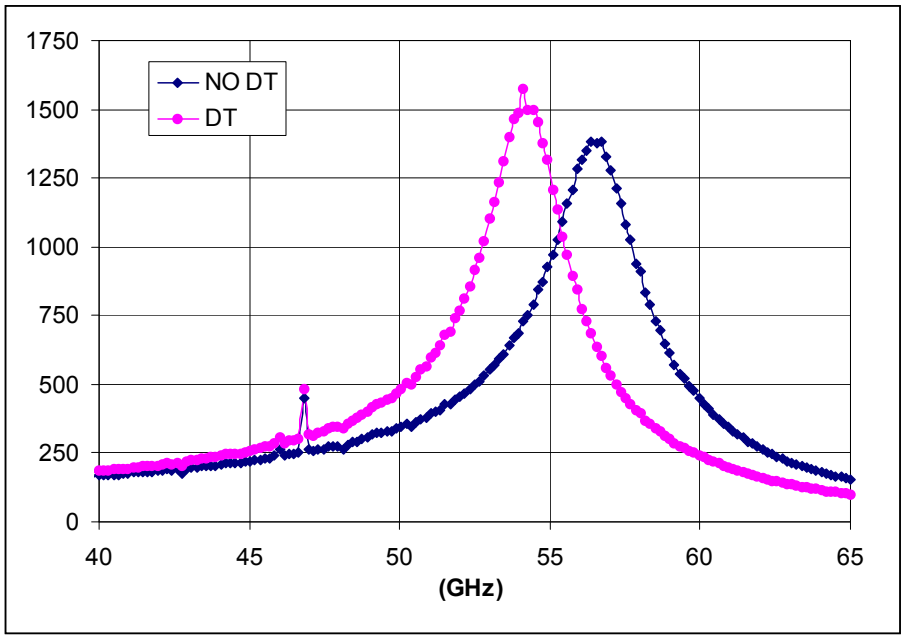


- Lossy substrate (~10 Ω-cm)
- 6–8 metal levels (copper)
- Chemical mechanical planarization (20-80% metal density)
  - Slots required in metal lines
  - Fill metal in empty areas
- Multiple dielectric layers

Ring Inductors Measurements

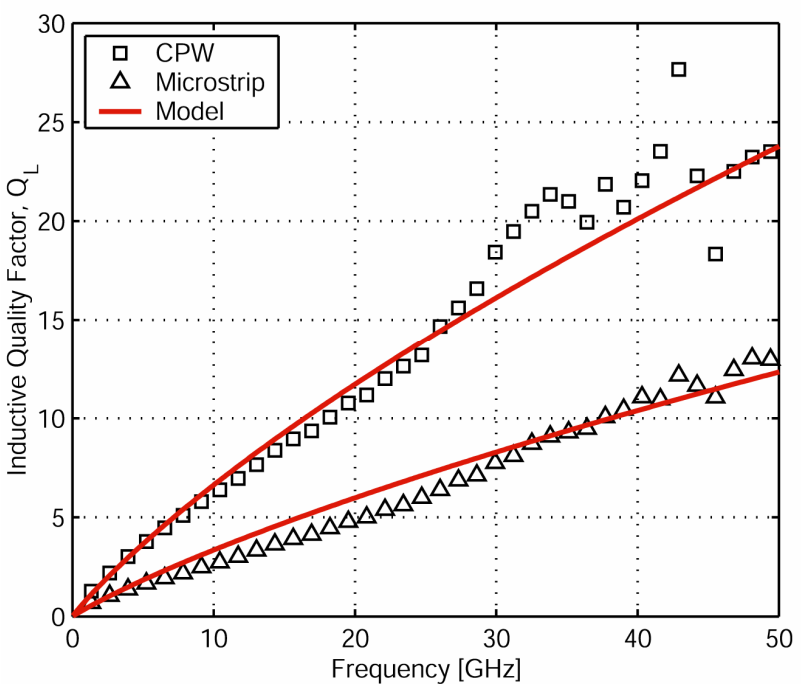
Low Loss MIM Cap and Inductor Ring
Tightly Coupled for Low Loss





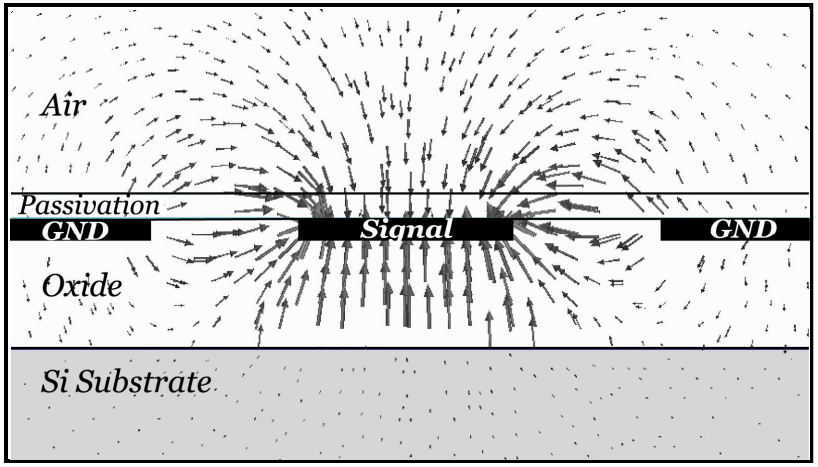
- Tank resonates at design frequency (56 GHz)
- Tank with DT (deep-trench) array has slightly higher Q but lower SRF
- Loaded Q > 20 encouraging measurement

Co-planar (CPW) and Microstrip T-Lines

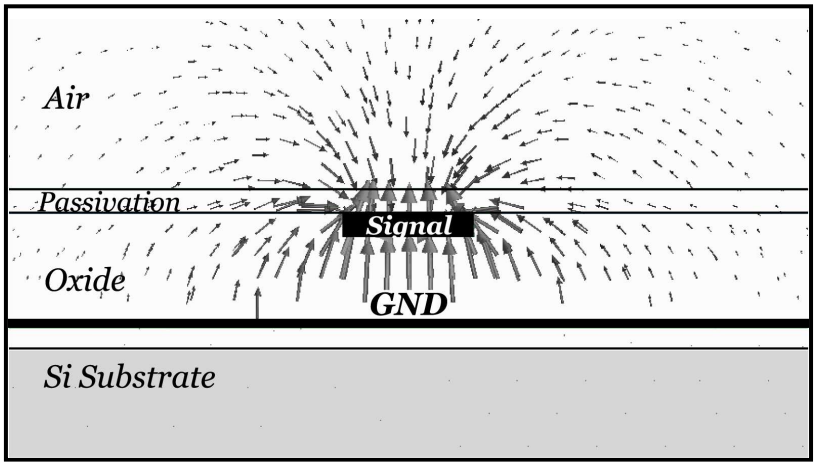


- Microstrip shields EM fields from substrate
- CPW can realize higher Q inductors needed for tuning out device capacitance
- Use CPW

CPW



Microstrip



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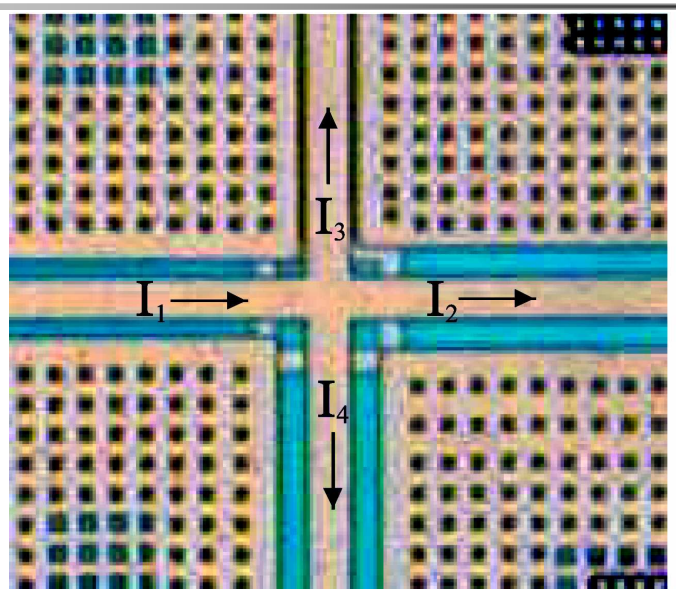
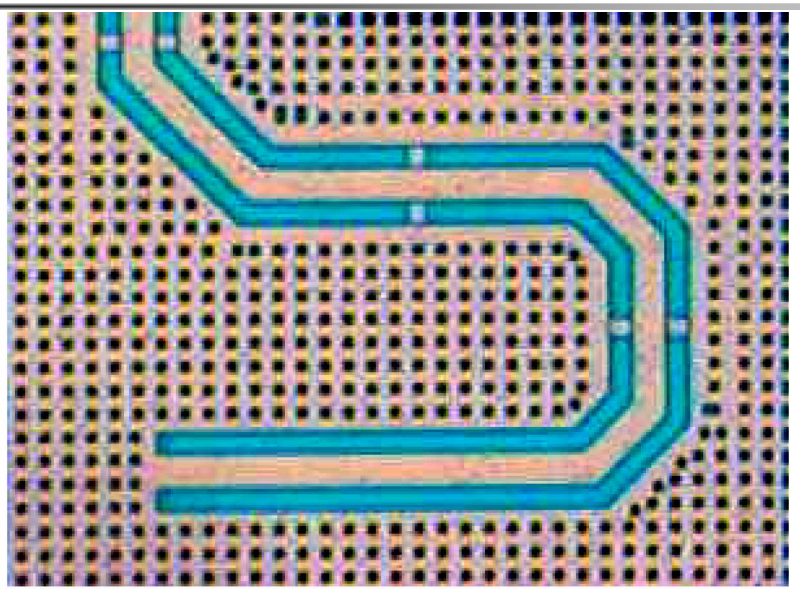
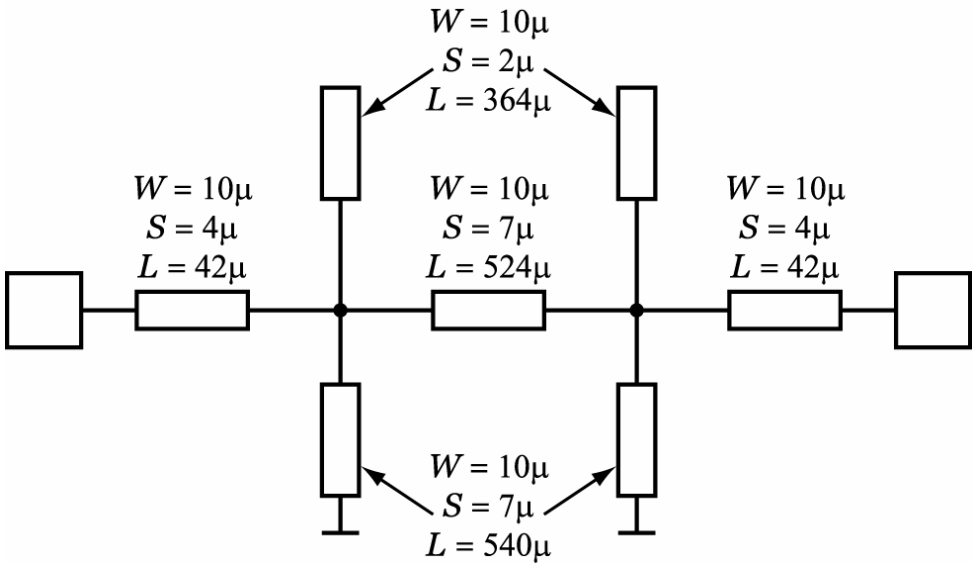
Co-planar waveguide layout issues

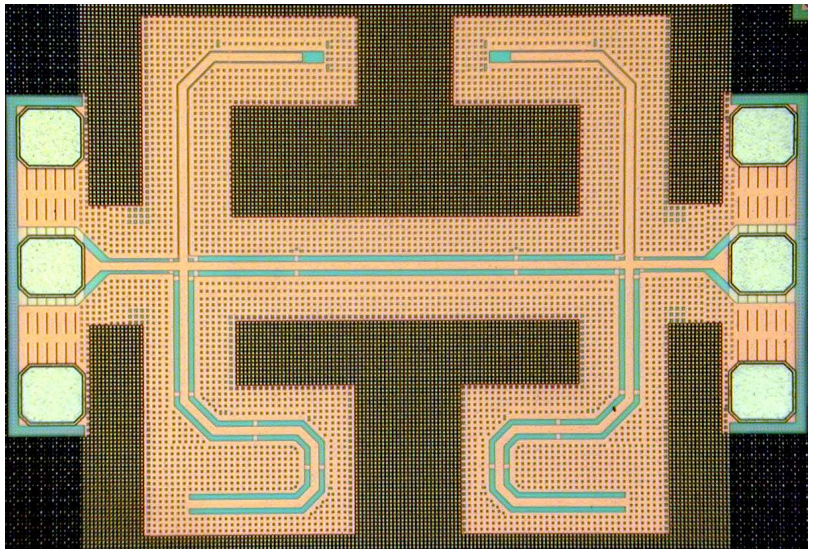




- Bridges suppress odd-mode propagation
  - Keep ground currents ***balanced***
  - Advantage of the multi-layer metallization in CMOS
- Signal-to-ground spacing
  - Used to set Z_0
  - Helps confine EM fields
  - Effects of bends are reduced

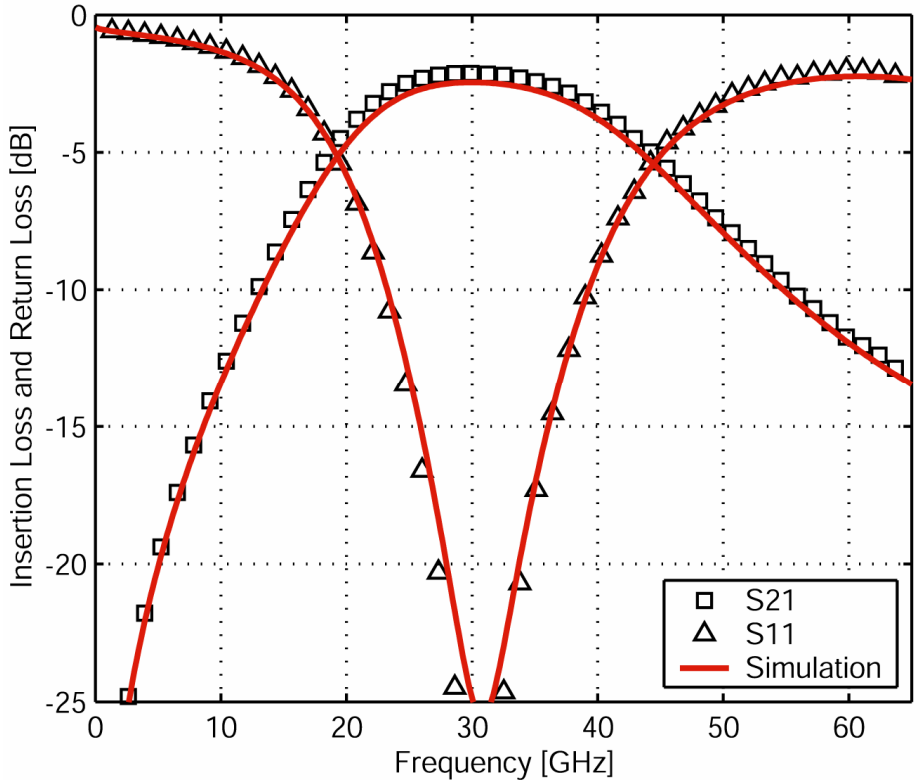
30-GHz Co-Planar Waveguide Filter





- 30-GHz center frequency
- Composed of scalable transmission lines
- Tests accuracy of transmission line modeling

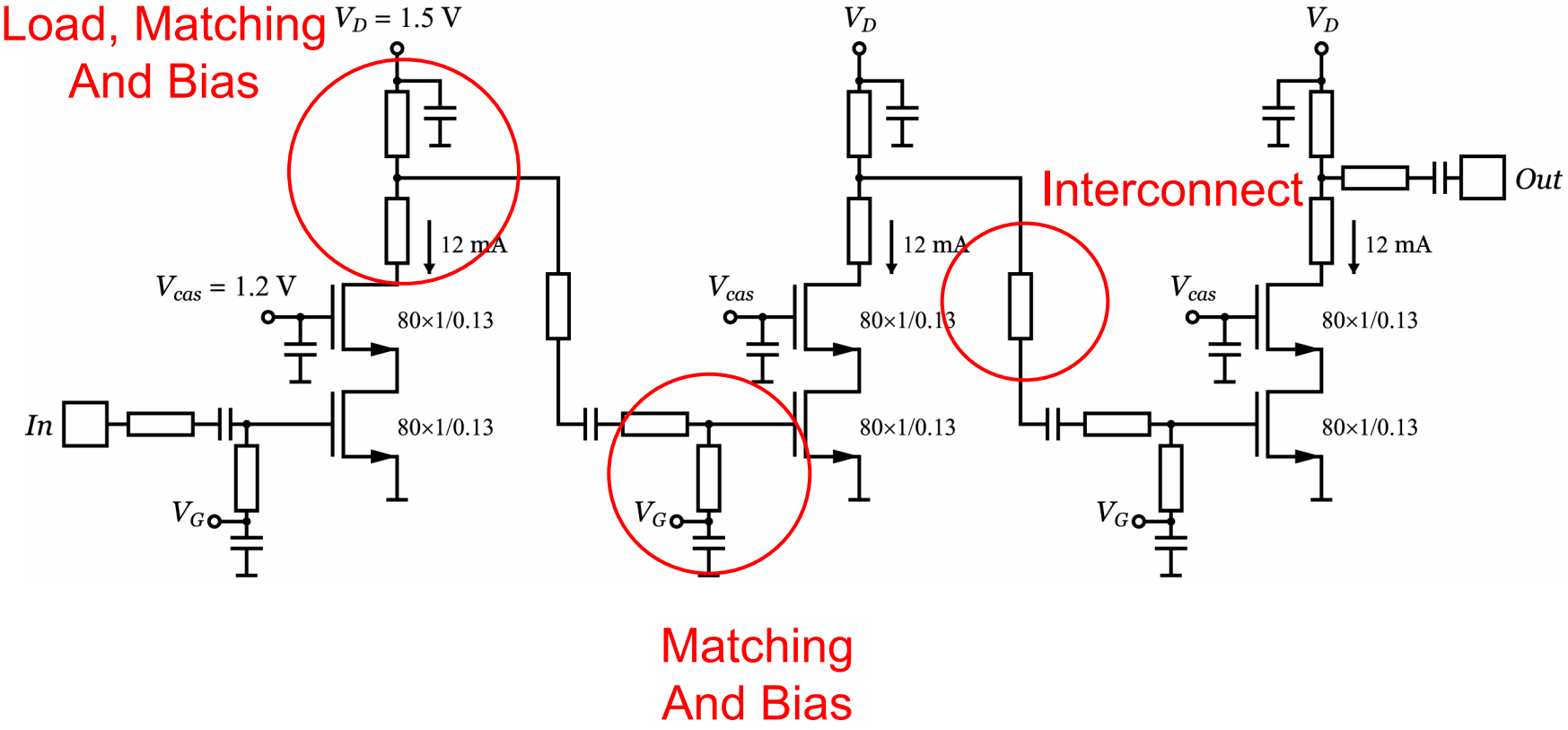
Filter Measurements vs. Models



From the accurate modeling we can conclude

- Negligible coupling between lines
- Bends, junctions, bridges have small effect

Key Passive Devices



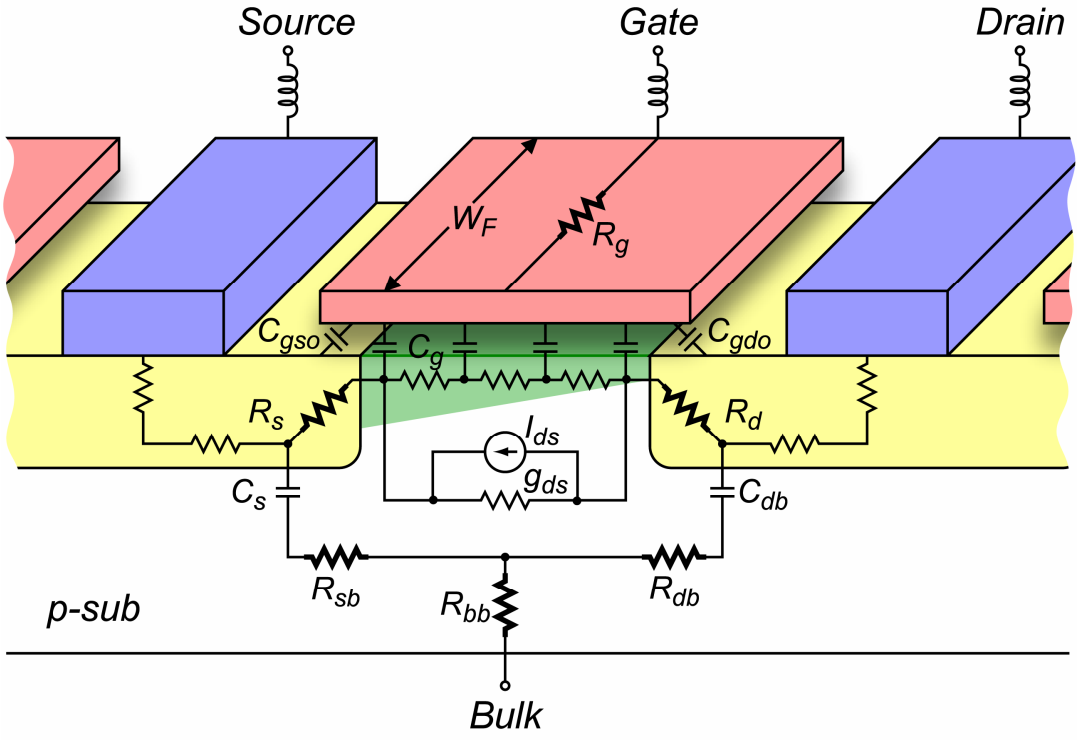
- Short transmission lines (T-lines) are used as inductors (to tune out FET parasitics)
- T-lines are also used for impedance matching, interconnect, and biasing
- Bypass and coupling capacitors and varactors also characterized at 60 GHz

How fast is standard 130-nm CMOS?

First what is the best metric, f_{max} or f_t ?

- f_t , the unity current gain, is useful for estimating circuit bandwidths at low frequency
  - Ignores the parasitic resistive losses
  - Doesn't assume optimal matching
  - Affected by wiring capacitance
- f_{max} , the frequency when the device becomes passive, describes the real limitation
  - Fundamental property of the device
  - Limited by resistive losses that reduce power gain
  - Requires an optimized layout

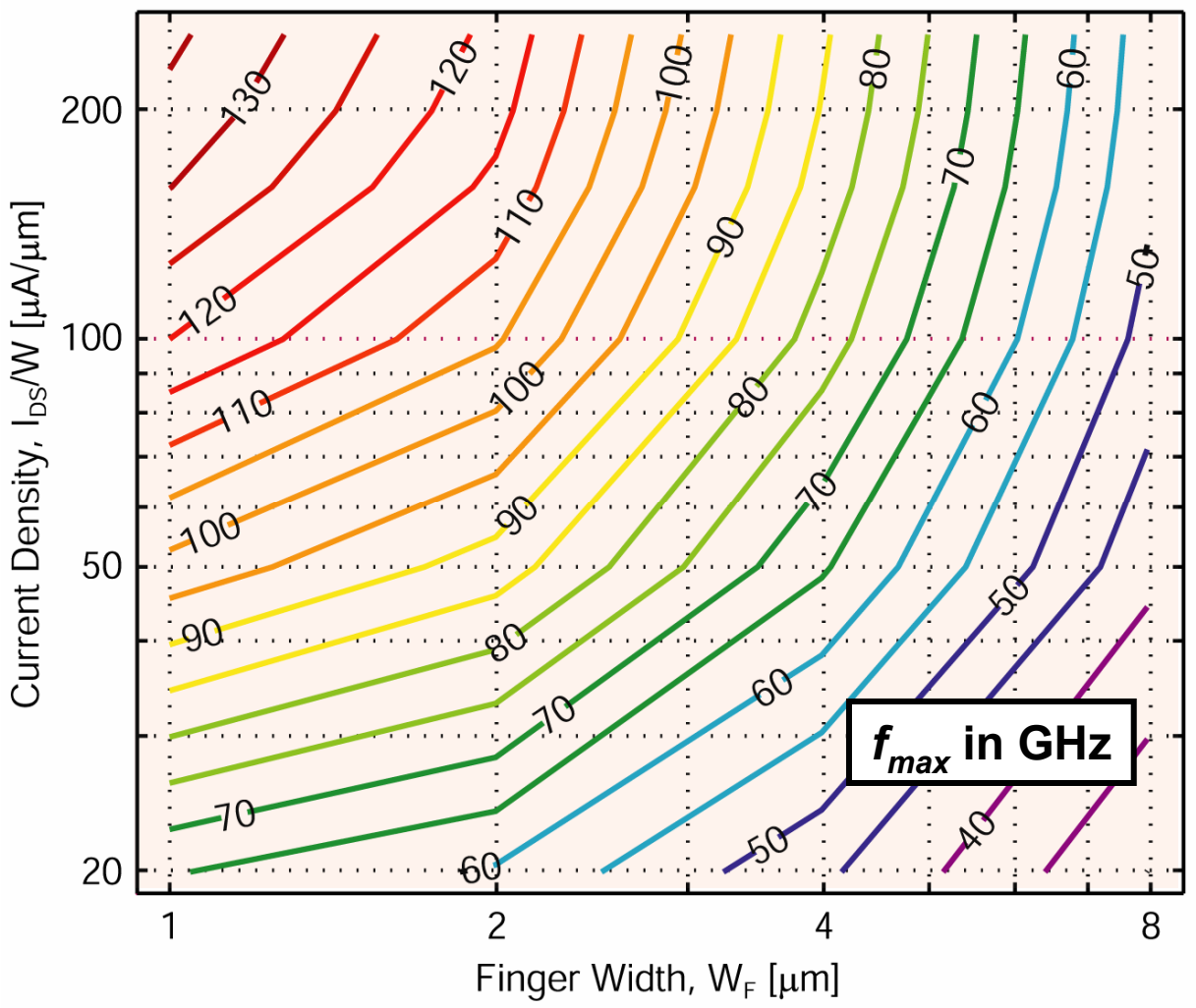
Layout for Maximizing f_{max}

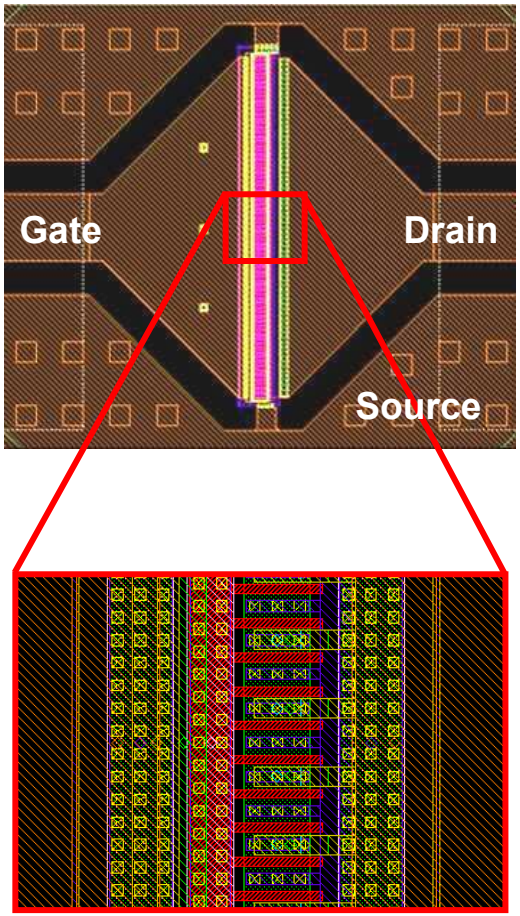


Minimize all resistances

- R_g – use many small parallel gate fingers, <1 μm each
- R_{sb}, R_{db}, R_{bb} – substrate contacts <1–2 μm from device
- R_s, R_d – don't use source/drain extensions to reduce L

f_{max} vs. finger width





Increasing gate resistance ⟶

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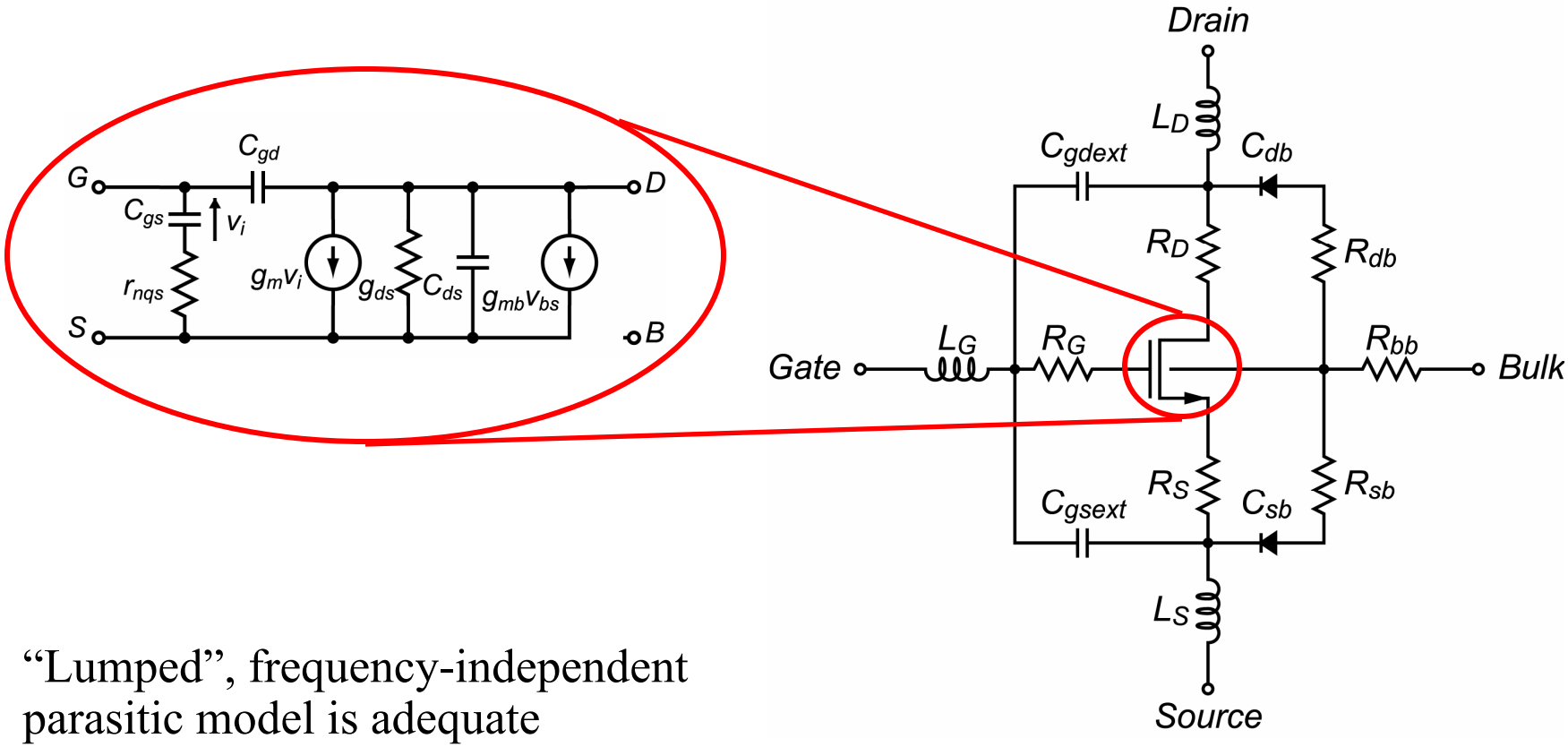
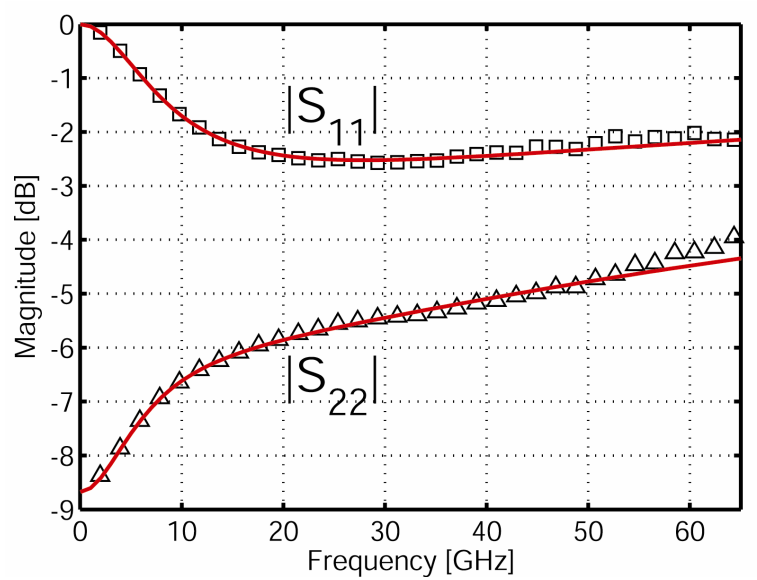
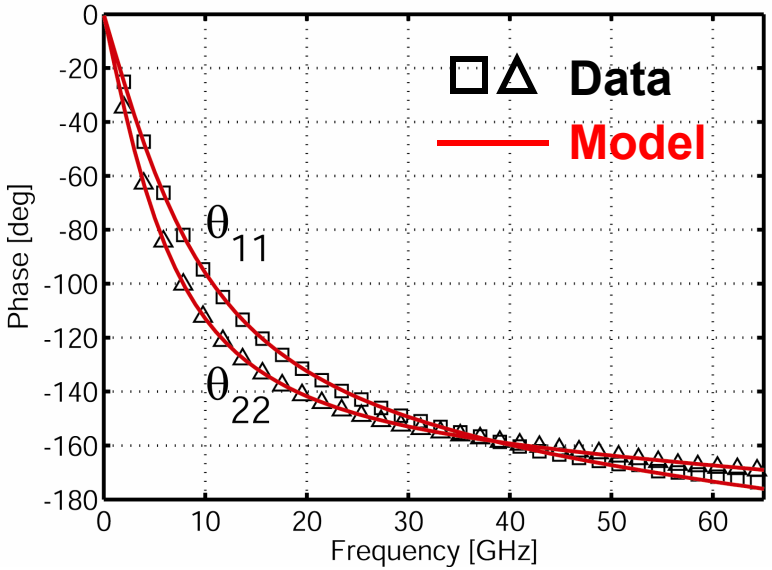
Extended Transistor Modeling

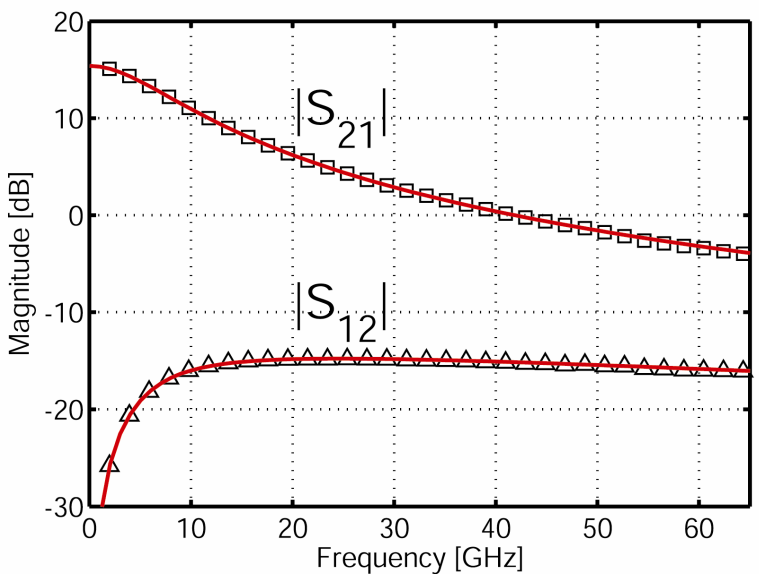


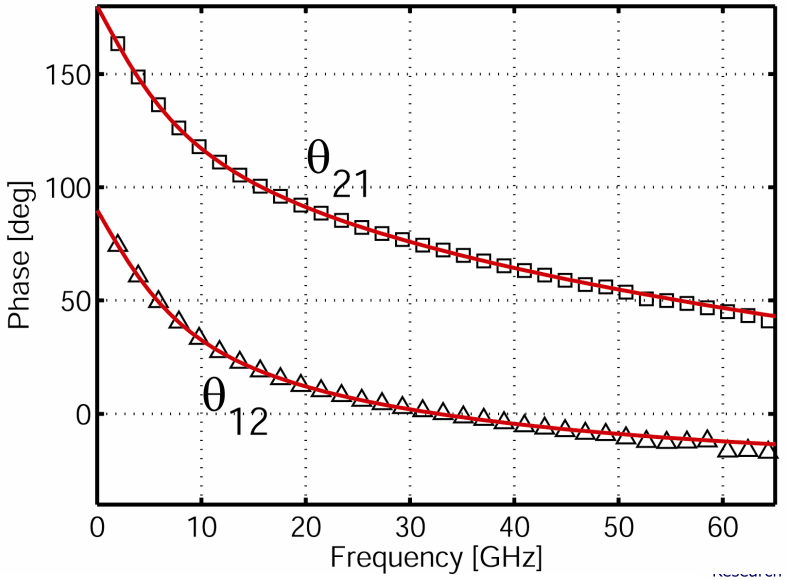
- "Lumped", frequency-independent parasitic model is adequate
- Bias-dependent small-signal transistor model for highest accuracy
- Large-signal BSIM3v3 model for nonlinearities and bias dependence

Small-signal model fitting – 0–65 GHz

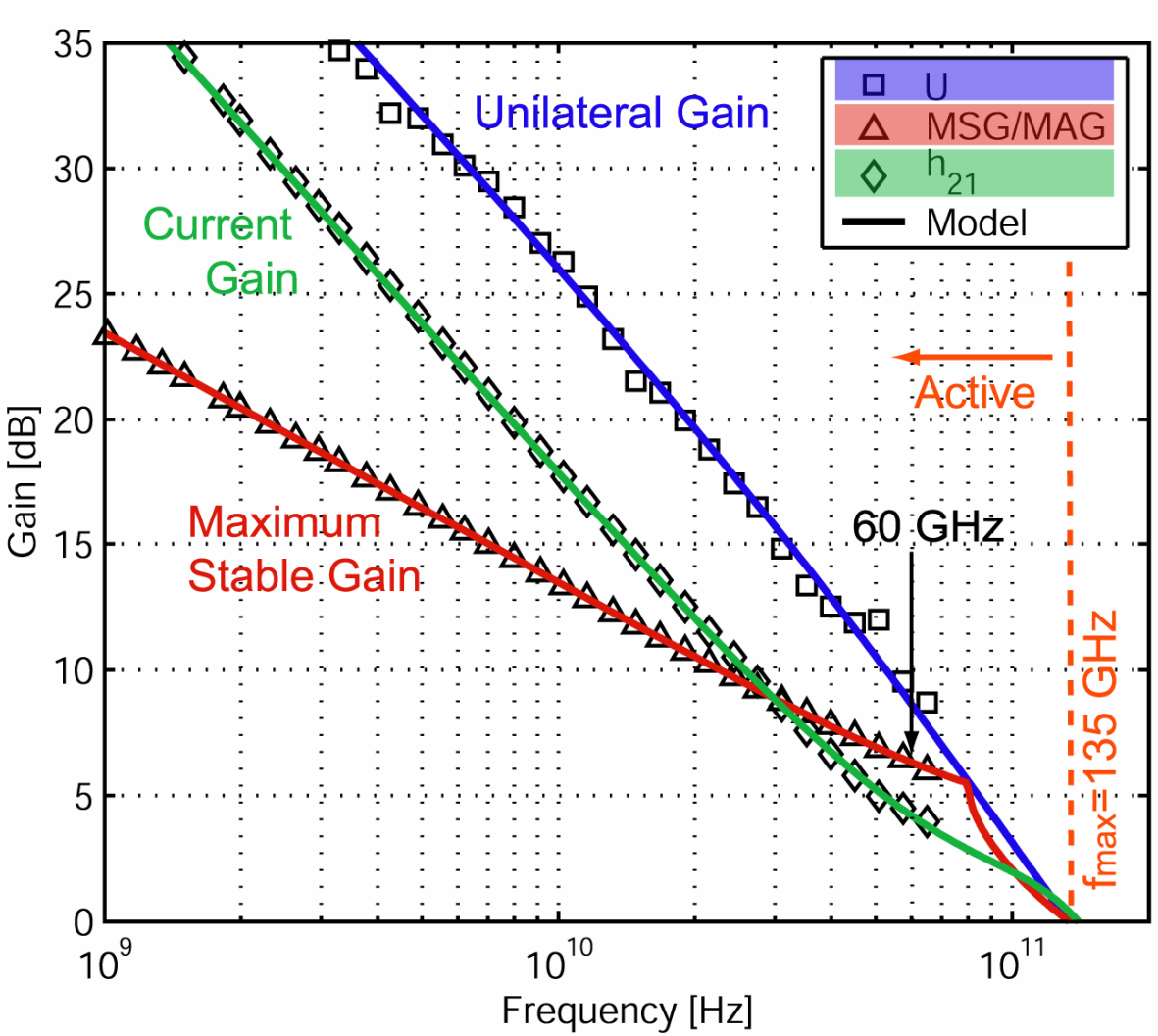


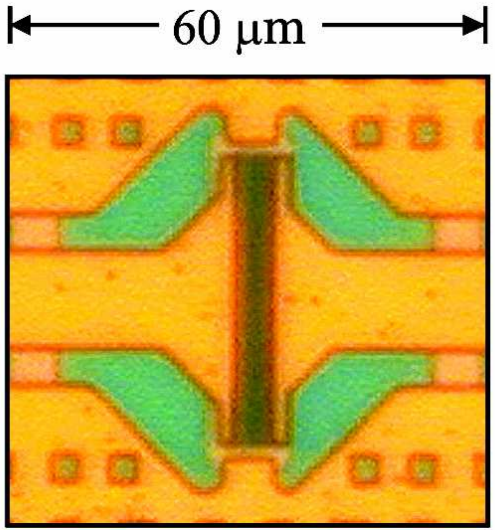






130-nm CMOS Device Performance





V_{GS} = 0.65 V

V_{DS} = 1.2 V

I_{DS} = 30 mA

W/L = 100x1u/0.13u

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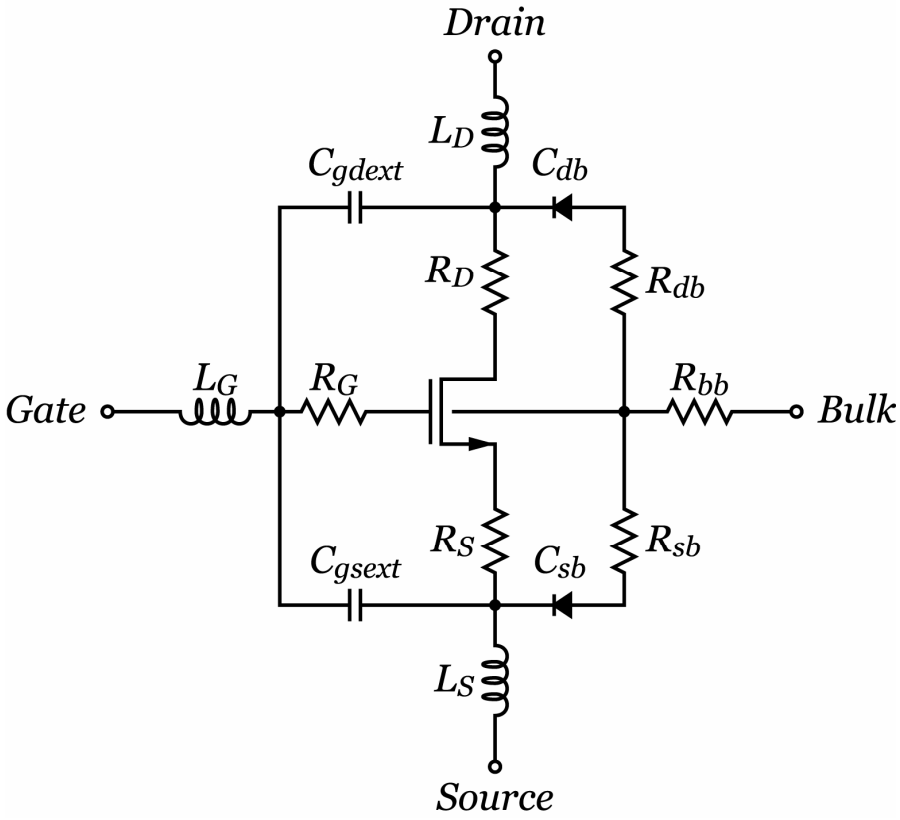
mm-Wave BSIM Modeling

- Compact model with extrinsic parasitics
- DC I-V curve matching
- Small-signal S-params fitting
- Large-signal verification

- Challenges:
  - Starting with a sample which is between typical and fast
  - Millimeter-wave large-signal measurements
  - Noise
  - 3-terminal modeling



Reference: "Large-Signal Millimeter-Wave CMOS Modeling with BSIM3", RFIC'04
Sohrab Emami, Chinh H. Doan, Ali M. Niknejad, and Robert W. Brodersen

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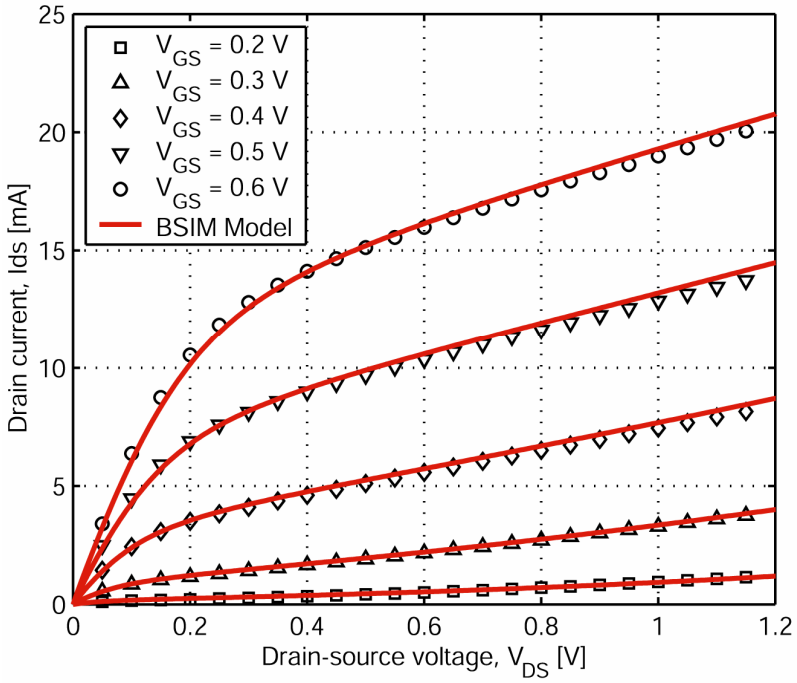
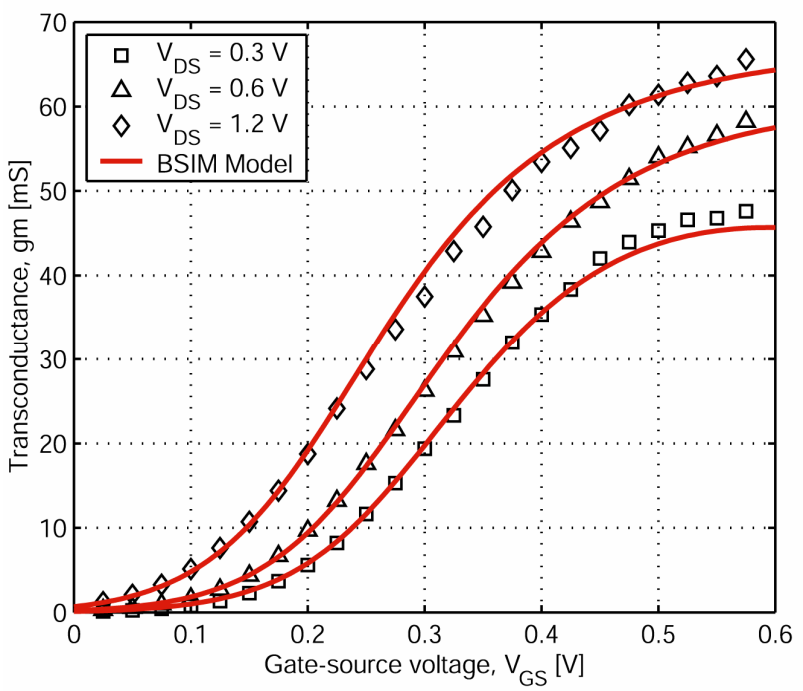
DC Curve Fitting



Measured and modeled IDS vs. VDS.

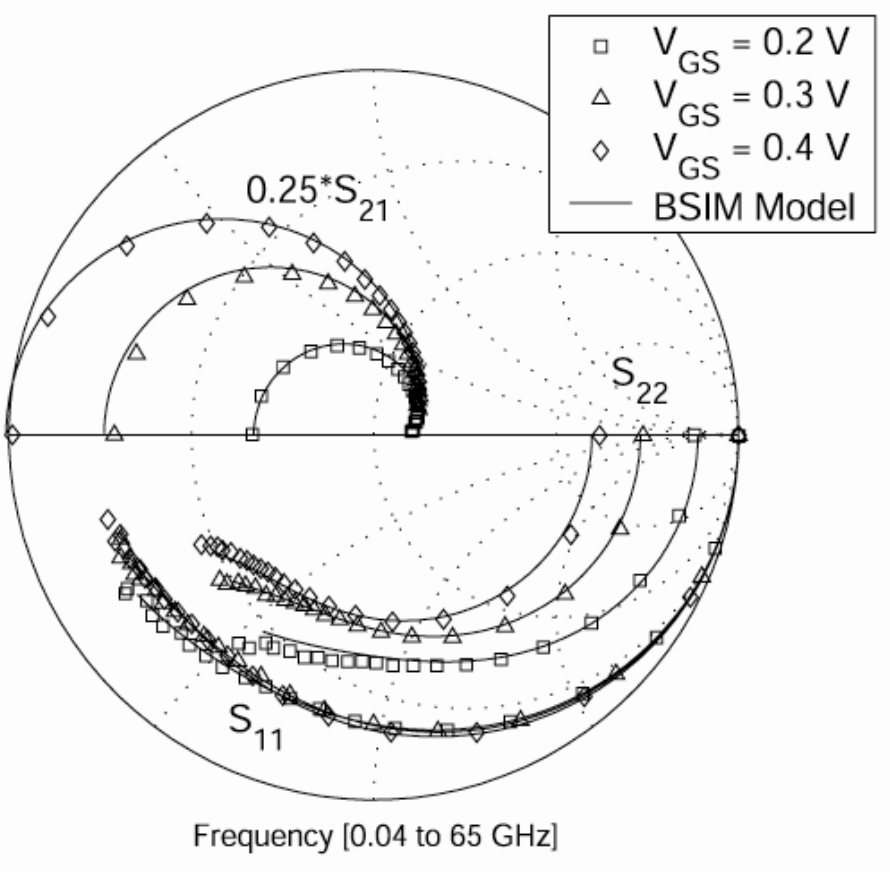


Measured and modeled gm vs. VGS.

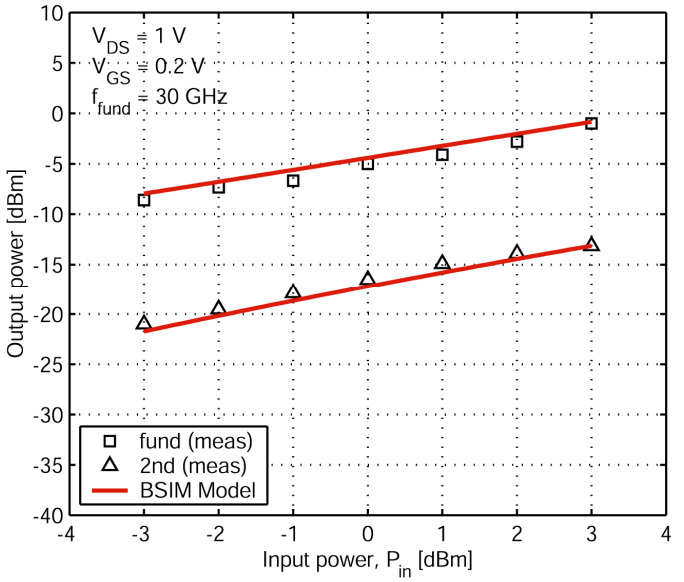
- I-V measurements were used to extract the core BSIM parameters of the fabricated common-source NMOS.

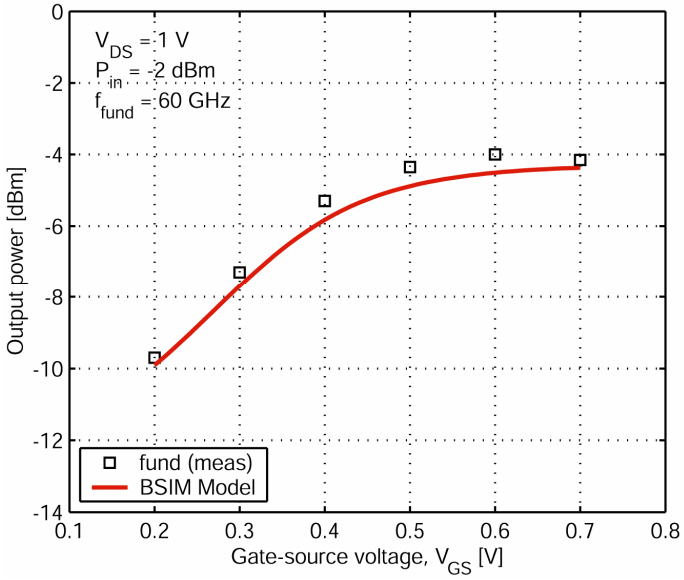
Model Extraction: Small-Signal

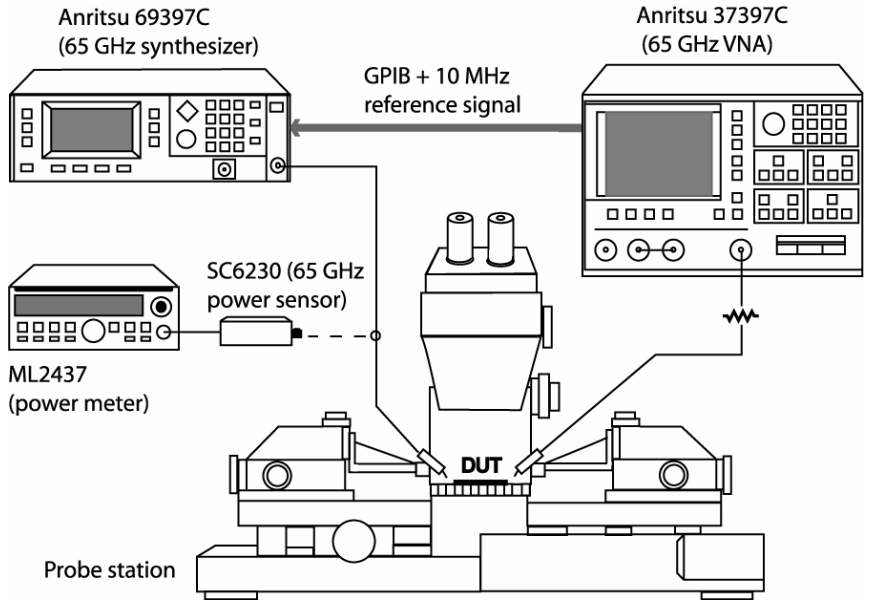
- Extensive on-wafer S-parameter measurement to 65 GHz over a wide bias range.
- Parasitic component values extracted using a hybrid optimization algorithm in Agilent IC-CAP.
- The broadband accuracy of the model verifies that using lumped parasitics is suitable well into the mm-wave region.



Large-Signal Verification







- Harmonics power measurement
  - Class AB operation
  - Large-Signal amplification at 60 GHz

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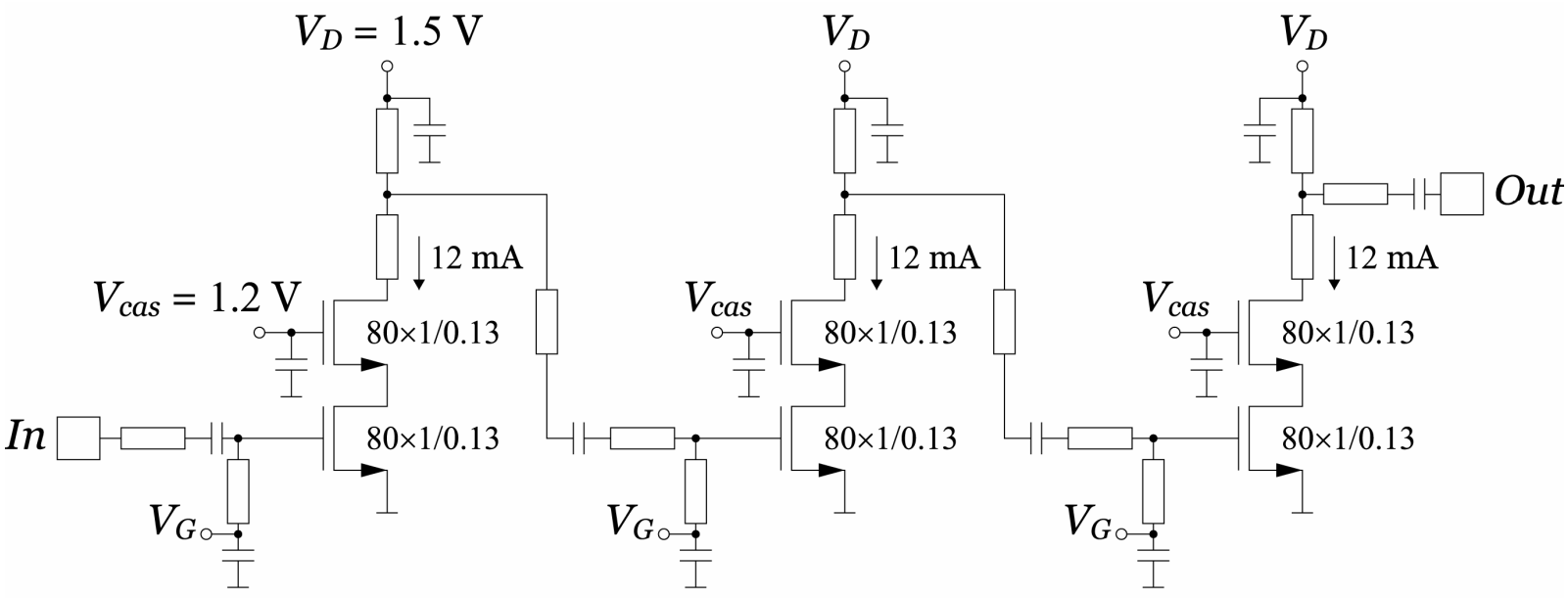
Challenges for 60-GHz Amplifiers

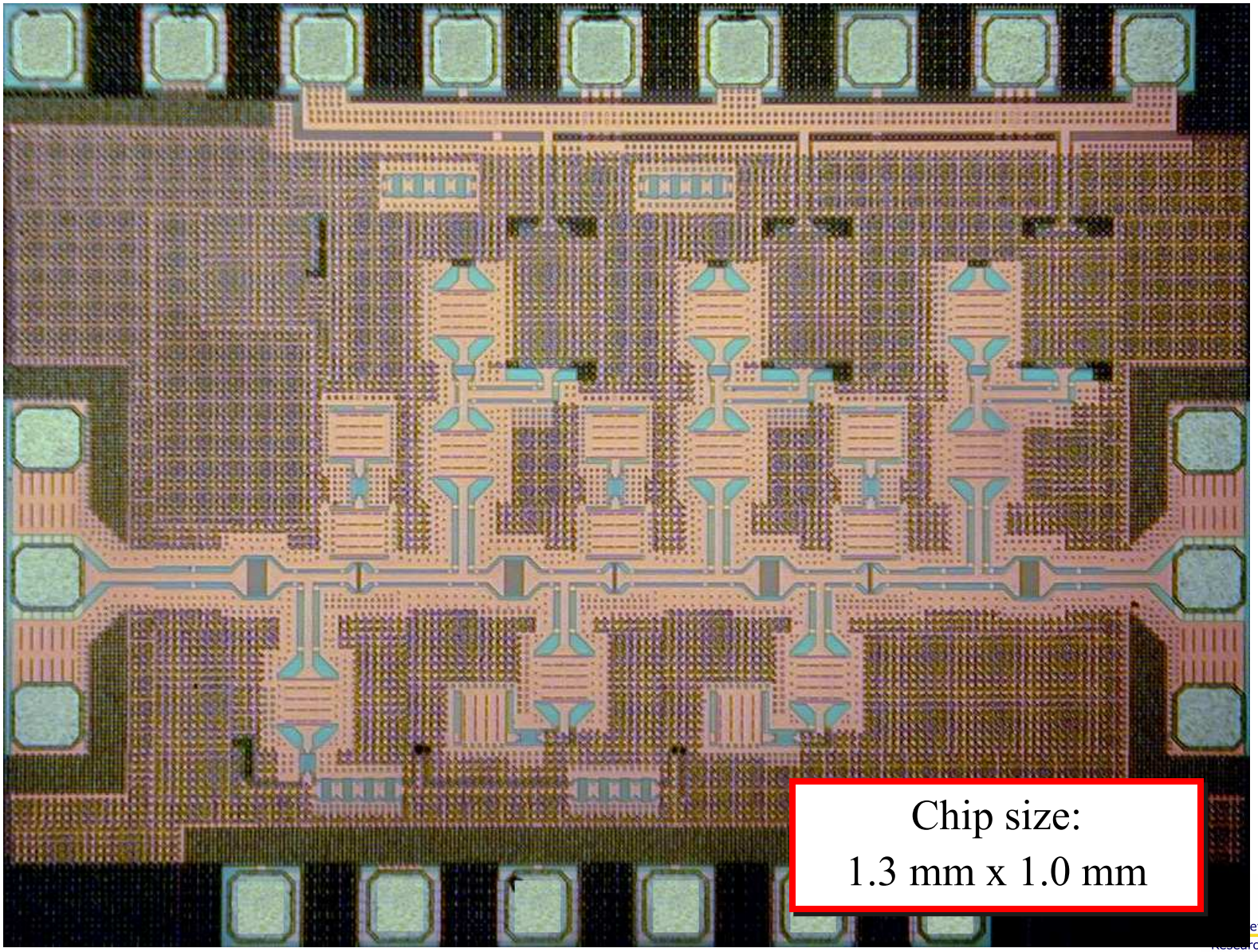
- Low transistor gain at 60 GHz
  - Optimized transistor layout
  - Require accurate device models
- Impedance matching networks
  - Need low-loss passives
  - Scalable models to design complex networks
- Broadband stability
  - Miller capacitance
  - Bias oscillations
- High output power or low noise

60-GHz Amplifier Schematic

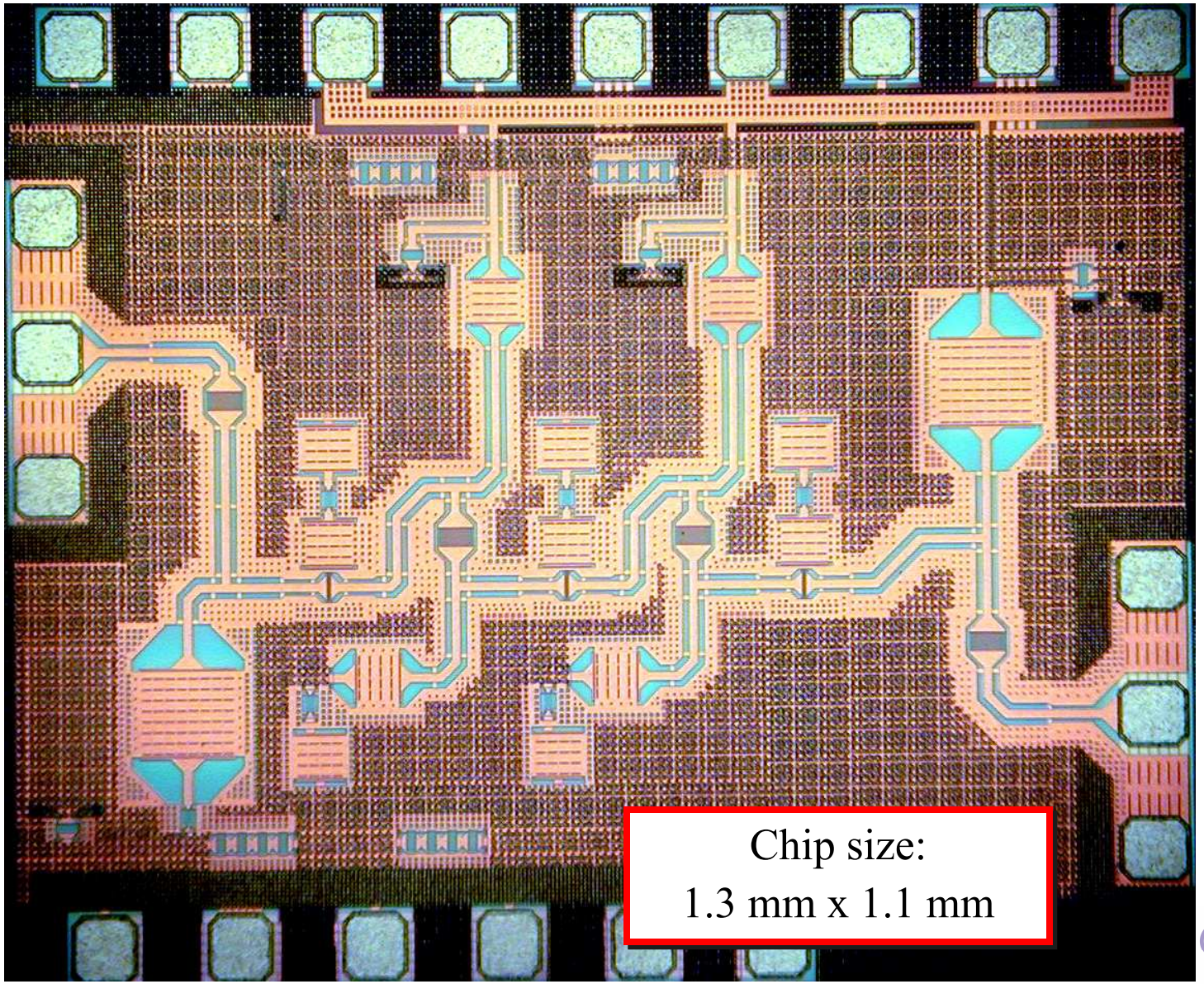


- 3-stage cascode amplifier design
- Cascode transistors improve isolation, stability
- Input/output matching networks designed to match 50 Ω
- Pads are included as part of amplifier
- Designed using only measured components

60-GHz Amplifier Layout



40-GHz Amplifier Layout



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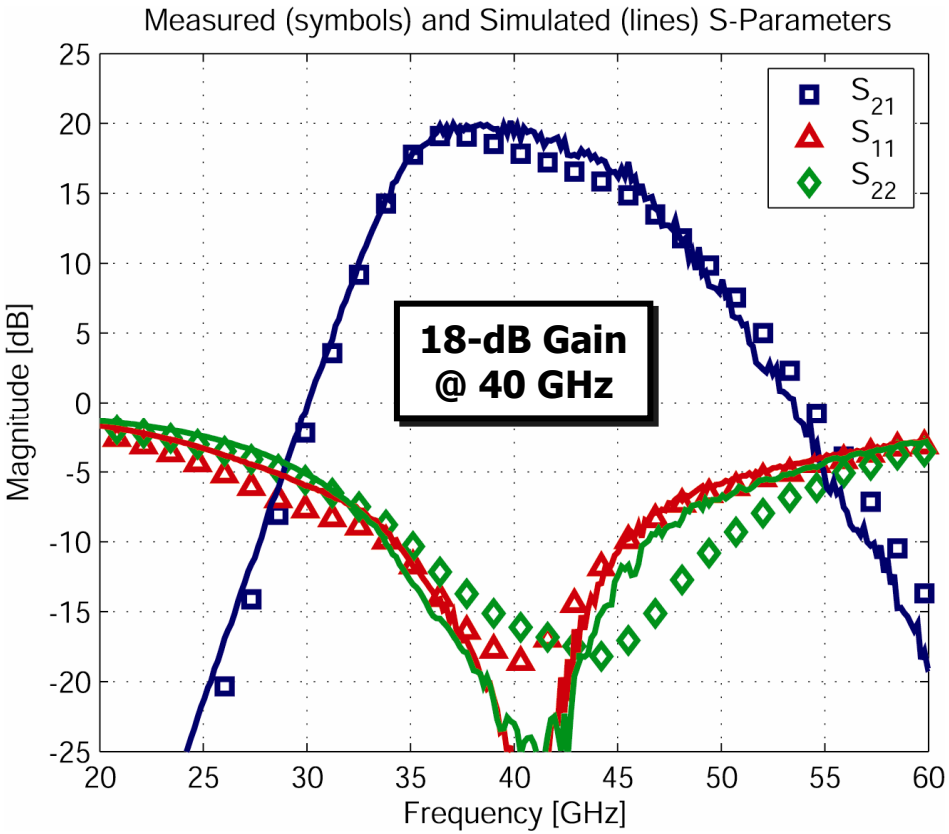
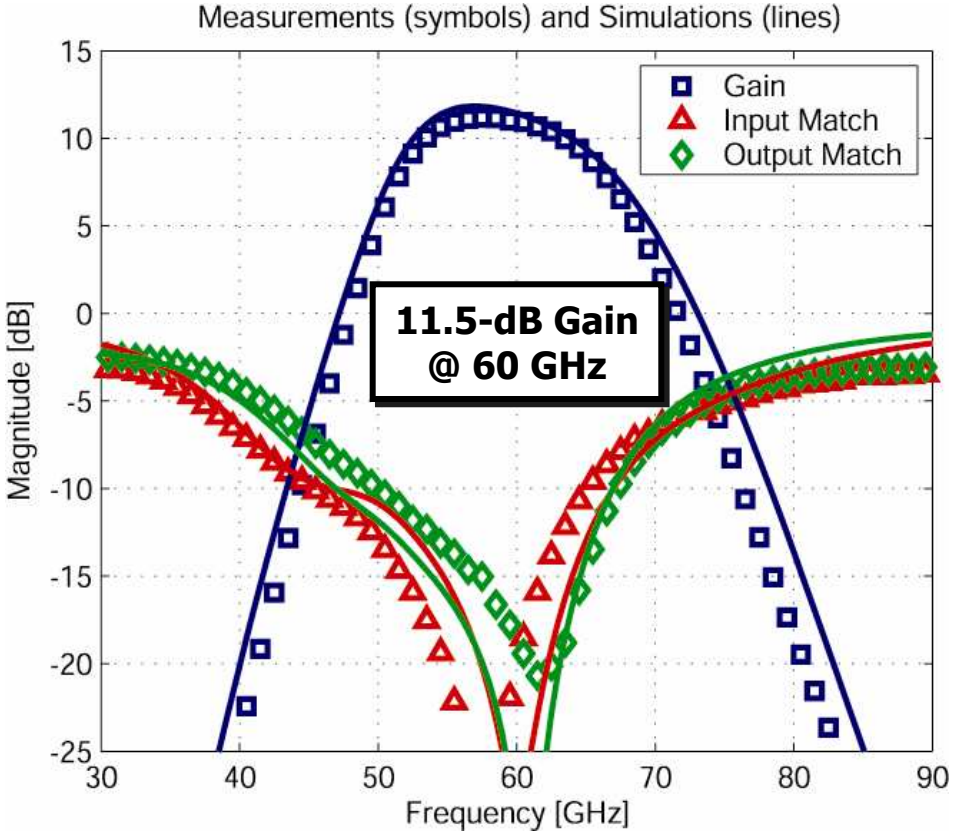
40-GHz and 60-GHz CMOS Amplifiers





- We have developed a design methodology that gives repeatable results for microwave CMOS design
- Power consumption: **36 mW** (40 GHz), **54 mW** (60 GHz)

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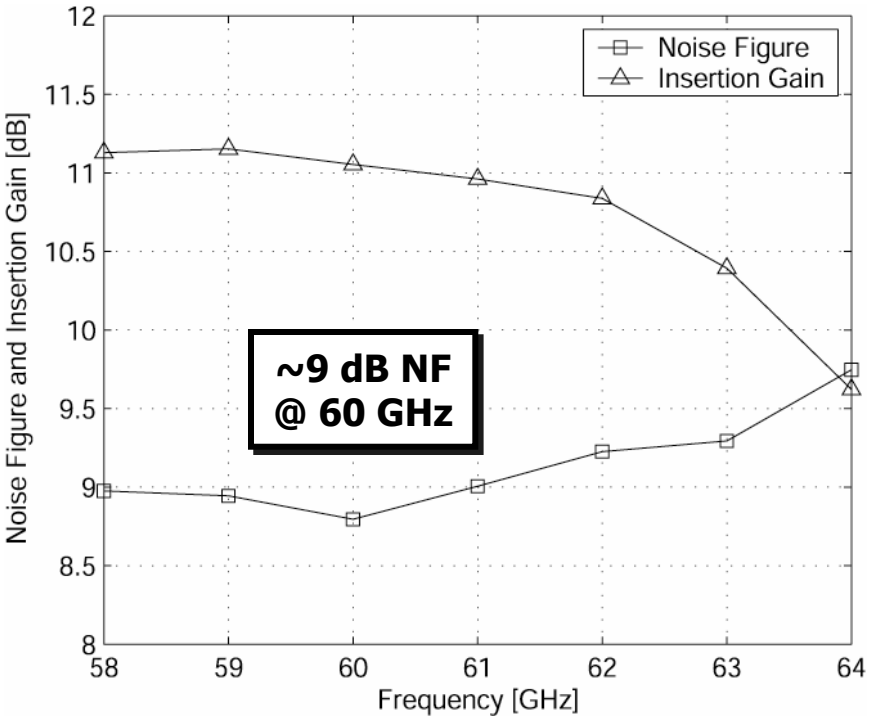
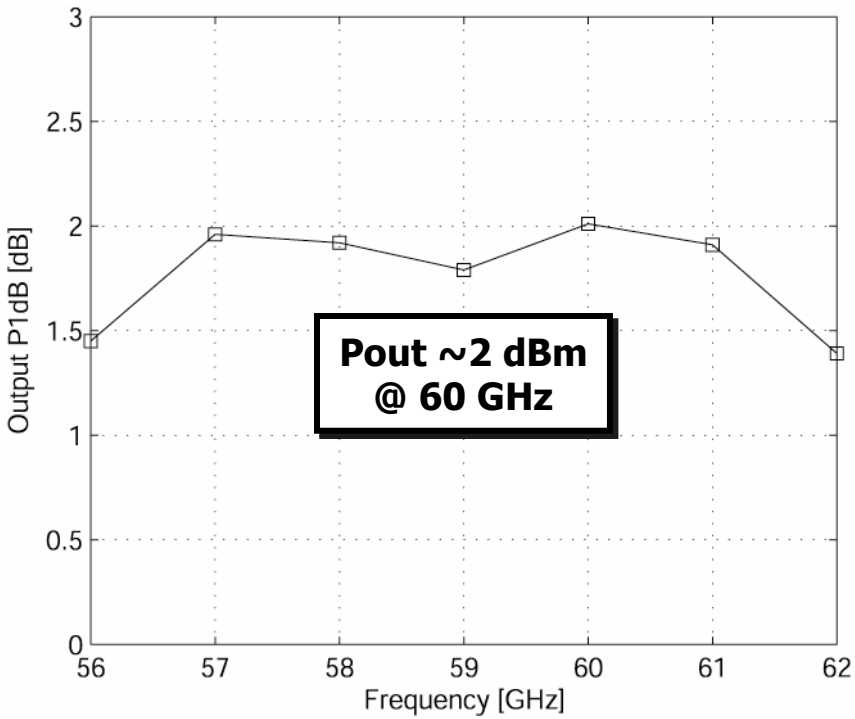
60-GHz Noise Figure and Compression





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