17GHz and 24GHz LNA Designs based on Extended-S-parameter with Microstrip-on-Die in 0.18µm Logic CMOS Technology

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Abstract

In a marked departure from traditional microwave design approaches, we present S-parameter based designs for 17GHz and 24GHz LNAs where the size of active devices is a design's degree of freedom and passives on the CMOS die are significant noise contributors, due to their low Q. Because of the low Q passives, design method includes (a) backing off from the transistor's NFmin, and (b) proper choice of transistor size to minimize length (i.e. losses) of the microstrips-on-die. High performance logic 0.18µm CMOS technology is used, digital layout design rules are enforced and sharp turns are used in all microstrip-on-die passives. The distributed on-die passives have been used to realize robust, low inductance values (as low as 25pH) in a "correct-by-construction" approach. Both LNAs reach NF of 5-6dB, only 2-3dB above the active devices minimum noise figure, the best results known to the authors at these frequency of operation using 0.18µm CMOS technology. IP3 is as high as –3dBm. Both LNAs operate at frequencies around 1/3 of the CMOS transistor's f_t (60GHz).

Introduction

The 17GHz and 24GHz ISM bands can be used for short-range, high data-rate wireless communications. The high frequency also facilitates compact monolithic realizations due to the small footprint of the passives. In this work, we describe fully differential, AGC enabled, LNAs for these bands using 0.18µm logic CMOS technology. The designs and optimizations are based on device S-parameter measurements (*no* CMOS modeling of the transistors is used) and use on-die microstrip-based passives; resulting in substrate/parasitic insensitive structures (due to a metal 1 ground plane), that are correct by construction. Electromagnetic Field solver (for the microstrip on the CMOS die) and microwave circuit simulator (which takes both the transistor S-parameter measured data and the field solver results for the passives) used in the LNA designs are a commercial package by Applied Wave Research (AWR) [1].

Backing off method introduction

Traditional microwave design approaches assume high quality passives. Thus, low noise amplifier designs primarily seek the transistor's NFmin and implement its optimum source (driving) impedance, so far as this does not compromise unacceptably the gain of the amplifier or its input match [2]. In contrast, when passives are implemented on a CMOS die, because of geometric constraints (more on geometric implications for on-die realizations later), their low Q make such an approach sub-optimal. In effect, as presented in this paper, low noise amplifiers are optimally designed if *backing off* from active devices's NFmin is used. This new approach minimizes the final noise figure of the LNA by trading off a small augment in transistor's noise contribution for a much lower noise contribution from the lossy passives.

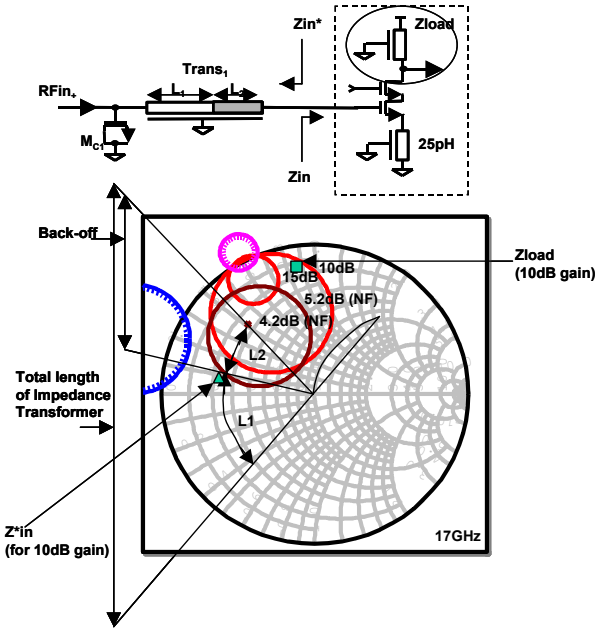


Figure 1: *Backing-off* from active device's NFmin: length of impedance transformer's transmission line is shortened to diminish the noise contributions from lossy passives at the expense of a small augment in the contribution from the active devices, but still producing a lower noise figure for the final LNA.

Figure 1 illustrates how the *backing off* approach is applied to the definition of transmission line length of the impedance transformer ($Trans_1$) in the input matching network (IMN) of the amplifier. Constant gain circles (15dB and 10dB gain, Zload referred) and constant noise figure circles (Z*in referred) for a cascode structure with inductive source degeneracy is depicted. Note that if the design of the input matching network were done with high-quality passives the length of the impedance transformer would have been as close to *L1+L2* as an acceptable input mismatch would allow. However, once low-Q passives are used, making the length of Trans1 be shortened to *L1*, despite some augment in the cascode structure's noise, leads to smaller noise figure for the final low noise amplifier (LNA). Moreover, the pair Zload and Zin* for 10dB gain, identified in figure 1, stresses that *backing off* can lead not only to a lower noise figure but can also lead to minimal mismatch at the

input port of the amplifier. In general, the amount of *back off* is function of how low the Q of the passives is and how slowly the active devices' noise figure changes as their driving source moves away from their optimum (i.e. how small the active device's noise parameter Rn is). The disposition of constant gain circles, constant noise circles and stability circles in the Smith-chart will change with transistor size, amount of source inductive degeneracy and frequency of operation of the LNA. In the designs presented in this paper, for every step in the optimization process, *backing-off* is always checked around every design point iteration.

Active device size and circuit description

We begin by experimentally quantifying the RF performance and NFmin, as a function of size and gate overdrive for Intel's logic 0.18µm CMOS transistors, with widths from 26µm to 400µm. The baseline characteristics for these devices are shown in table 1.

Table 1: Baseline characteristics of NMOS W/L=250/0.18, T=25°C.

Vg (V)	Vd (V)	freq (GHz)	Fmin (dB)	$\|G_{opt}\|$	$\angle G_{opt}$ (°)	R_n (/50)	Ft (GHz)	Fmax (GHz)
0.7	0.7	17	2.2	0.8	117	0.35	60	90
0.7	0.7	24	2.7*	0.8*	159*	0.35	60	90

*** extrapolated from experimental data covering from 2GHz to 20GHz.**

The maximum unilateral power gain, Gmax,u, for a NMOS transistor (fig. 2a) in this technology grows significantly from 0 to 200mV, but the increase saturates above these values of gate overdrive (Vgs-Vt). Assuming that up to 50mV variations in Vt for this devices must be absorbed in a robust design, an overdrive of 200mV is chosen as the required design point. NFmin (fig. 2b) tends to change only marginally with device size, favoring larger devices below 17GHz and smaller devices above this frequency. Constant-gain circles tend to be smaller for the same gain with increasing device sizes (fig. 2c), which limits the choice of load impedance values for oversized devices. This limit, in combination with the need to have appropriately sized transmission lines for the input matching network - IMN (to reduce the noise contributions from passives), resulted in our choosing a width of 250µm for the active devices for both 17GHz and 24GHz LNAs (revisited in the next section). The chosen device is conditionally stable, and its cascode configuration, also conditionally stable (fig. 3), has stability factor K = 0.34, which produces stability circles that significantly cut the Smith-chart. Inductive source degeneracy is used for easing the design of the IMN as in traditional microwave design [2], and also for improving the stability factor of the amplifier's basic two-port element (cascode + inductor degeneracy). Note that even though a cascode structure diminishes the feedback from output to input, this feedback is still significant at 17/24GHz, as implied by the source stability circle cutting the Smith-chart ([3]). Consequently, the choice of load reflection coefficient does affect the source reflection coefficient required for input matching (contrary to the common CMOS design practice of ignoring such feedback [3,4]). A small 25pH inductor is used for source degeneracy. Larger inductive degeneracy degrades this cascode's stability. This inductor motivates the use of distributed elements in the LNA design, as a shorted 50 ohms on-die transmission line develops this inductor value at only 64µm and 61µm (for 17GHz and 24GHz resp.) from the shorted end. In contrast to a lumped 25pH element (which would have too small a size), these distributed element sizes are robust with respect to perturbations caused by interconnect segments from the inductor to the active devices.

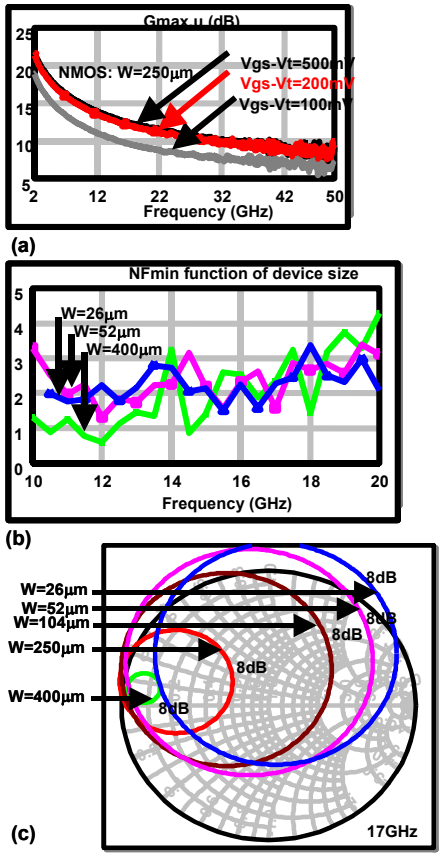


Figure 2: RF characterization of 0.18µm digital CMOS: (a) Gmax,u as a function of (Vgs-Vt) and frequency; (b) NFmin and (c) gain as a function of device size.

All the distributed elements in both LNA designs are used in combination with strategically placed lumped capacitors (realized using MOS caps). This minimizes the length of every microstrip in the design. Both 17GHz and 24GHz LNA designs share essentially the same topology and design process, thus only the 17GHz design is explained here. We have used a 2-stage topology to minimize input mismatch over gain variations produced by the AGC (a shunting transistor at the differential output of the second stage). Half-circuit topology (figs. 4,5) shows inductances Lload1 and Le constructed from 50 ohms microstrip stubs shorted at one end and made long enough to develop the required inductance values. Lload2 is constructed from a shorted 100 ohm microstrip stub. The change to 100 ohms microstrips (finer metal trace) produced a shorter stub (for the same required inductance) allowing it to be nested inside impedance transformer Trans2. Trans2 (realized as a 50 ohms microstrip) transforms the input impedance of the amplifier's second stage into a suitable impedance at the output of the amplifiers' first stage. This impedance, in

parallel with the inductance produced by Lload1, realizes the required load reflection coefficient for 10dB gain in the first stage. Trans1 transforms the amplifier's first stage input impedance into a match with 50 ohms, once capacitor C1 (MOS cap, MC1, figs 4,5) is placed in parallel. Bias is brought to the gate of second stage's transistor M3 by a 200 ohms ¼ wavelength, Mstb, which is ac-shorted at one end. This presents a large impedance (relative to 200 ohms) at the gate of M3, and consequently does not disturb the amplifier's inter-stage impedance transformation.

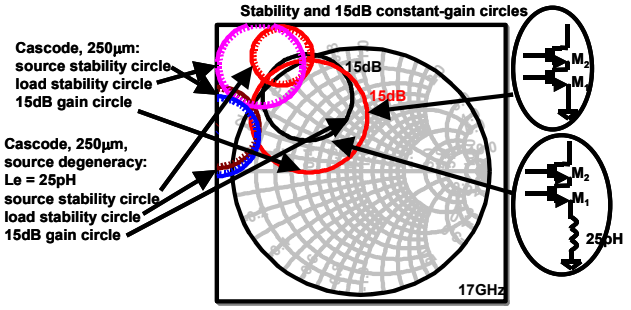


Figure 3: Comparison: cascode (250µm-wide, both devices) with and without 25pH inductive source degeneracy at 17GHz. Higher inductive degeneracy renders cascode more unstable.

Active device size and passive length

Low Q microstrip-based passives constructed on the CMOS die have strong contributions to the final noise figure. The low Q is a geometric imperative, as Q of microstrips follows $Q \propto h\sqrt{\sigma f}$ [5],where h is the height of the microstrip, σ is the conductivity of the microstrip, and f is the frequency of operation. In comparison to board realizations, the height of the microstrips reduce from 0.1mm to around 5µm in the CMOS die, with a corresponding Q value reduction from the high hundreds to values smaller than 10, at 17GHz, for microstrips on the CMOS die.

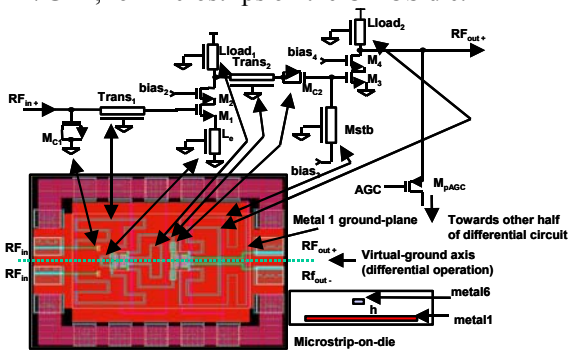


Figure 4: 17GHz LNA: simplified half-circuit schematic and fully differential layout.

We have identified the length of Trans1 as the major contributor to the NF among the passives. Consequently our optimization methodology involves the simultaneous sizing of the active devices and Trans1 in order to minimize the LNA's NF, at the same time we search for *backing off* at every design iteration. The primary goal being minimum noise figure with gain above 10dB, the transistor size cannot be too small since it leads to longer Trans1 microstrip and a consequent increase in losses with a resulting degradation of NF. A too large transistor size diminishes the overall RF/microwave performance of the active device and thus lowers the final amplifier gain (fig. 1). A 250µm wide device is chosen as the optimum width for the 0.18µm CMOS technology used.

A noteworthy point is that the LNA power dissipation is function of both the size and bias current used. Once the bias is set for robustness via Vgs-Vt= 200mV, the final noise figure cannot be traded off with power dissipation by adjusting the device size. This is because the smaller device will require longer and thus lossier passives; and larger devices suffer lower RF/microwave performance as mentioned above.

If power becomes a strong concern, the best strategy is to search for the lowest bias current (lowering Vgs-Vt), while still attending the gain conditions. This will favor using smaller devices sizes than 250µm, and the designer will need to accept reduced robustness against CMOS process variations.

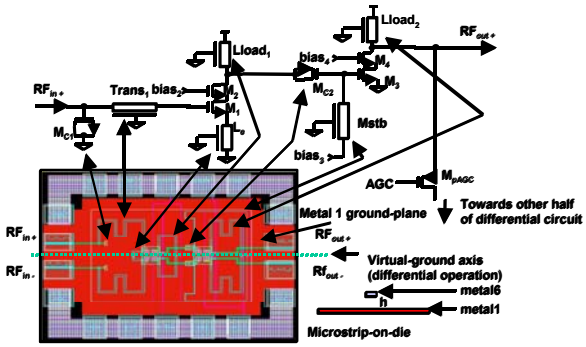
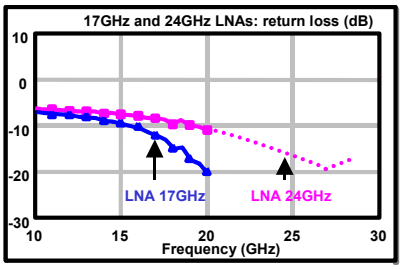


Figure 5: 24GHz LNA: simplified half-circuit schematic and fully differential layout.

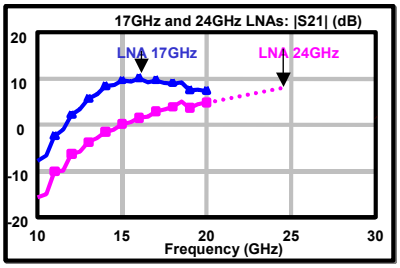
Layout aspects and performance

The sharp turns (necessitated by compatibility with digital CMOS) degrade the intrinsic Trans1 losses to ~1.5dB, which consequently also degrades the final noise figure by the same amount. The differential realization exploits the virtual ground along the axis of the LNAs, and all shorted microstrip stubs start from that axis (figs. 4,5). Metal 6 is used for the microstrips traces, metal 1 is used for the ground-plane and all bias voltages are brought to the center of the LNAs using metal 2 traces. In order maintain the axial symmetry of the design, bias lines are extended across the whole width of layout, even though their electrical connection to the circuits are made only at the central axis. In order to minimize coupling, the inter trace separation, s, is set at s=10 h, where h is the height of the trace above the metal 1 plane (fig 4,5). AGC is operated by transistor MpAGC by shortening the differential output lines, which does not disturb the LNA bias voltages, or those of the next element in the receiver chain. Figure 6a,b shows together return loss and |S21| (dB) for both 17GHz and 24GHz LNA. Measured results are summarized in Table 2. Both LNA's achieve a NF of 5-6dB which is only 2-3dB higher than the transistor's NFmin. Electromagnetic Field solver simulations showed 1.0-1.5dB of the final LNA's noise figure came from the sharp turns on the microstrips on die. The 24GHz LNA is characterized with measurements up to 20GHz (NF measurement system limit) and its performance extrapolated to 24GHz by

simulations/analogy from the fully characterized 17GHz LNA behavior. The IP3 of –3dBm is extrapolated based on our previous device and LNA measurements at lower frequencies. All the other results are from at frequency measurements. Die photo figure 7. *Backing off* technique is responsible for bringing the LNAs' noise figures down to 5-6dB. Not using this technique would have led to noise figures approximately 1.5dB higher.



(a)



(b)

Figure 6: 17GHz and 24GHz LNAs together: (a) return loss; and (b) |S21| (dB) as a function of frequency. Simulation results are within 5% to 10% of these experimental results.

Table 2: Summary of experimental results

	Digital CMOS Techno-logy	Transistor size (W)	Gate over-drive	Current per cascode	IP3	Return Loss	Noise Figure	Gain (Z21/Z11)
17GHz LNA	0.18 µm	250 µm	200mV	47mA*	-3dBm	-12dB	5.2dB	12dB
24GHz LNA	0.18 µm	250 µm	200mV	47mA*	-3dBm	-14dB **	6.0dB **	10dB **

* Under (Vgs-Vt)=200mV for robustness against up to 50mV of variations in Vt.
** Extrapolated from experimental results up to 20GHz. Noise Figure Measurement system limitation.

Conclusions

We have described a comprehensive, S-parameter based optimization of fully integrate LNAs at 17 and 24 GHz using a *backing off* approach and device sizing aimed at minimizing the added noise contributions of active and passives to the final LNA noise performance at the same time. This departure from traditional microwave approaches is prompted by the low Q of passives implemented on the CMOS die. The microstrip-on-die used in the designs have low Q because of their small geometric dimensions even though their dielectric is high-quality low loss SiO_2 (CMOS backend interlayer). Active device behavior was fully characterized from measured S-parameter. High-performance digital CMOS layout rules were imposed, and the resultant sharp turns in the microstrips-on-die, led to additional 1.0-1.5dB degradation in the final measured noise figures. Differential layout allowed for exploitation of virtual grounds along the longitudinal axis of the LNAs' layout. The use of a ground plane in metal 1 (used in realizing the microstrips-on-die) brings the additional benefit of providing for isolation from substrate noise coupling onto passives. Distributed-element-based inductances and impedance transformers used in both 17GHz and 24GHz LNA designs, led to a correct-by-construction approach to passive components (parasitic components are automatically absorbed in the distributed elements, self-resonance issues are eliminated and multi-mode operation is avoided by adjusting of the microstrips' transversal dimensions in a straightforward manner). This results in a robust implementation of inductances as small as 25pH. Although using distributed elements takes more area than lumped passive implementations, the robustness properties described above allow for seamless scaling upward to millimeter wave frequencies. 17GHz and 24GHz LNA's achieve 5-6dB noise figures, only 2-3 dB above the used active device's NFmin,. To the best of our knowledge, these are the lowest reported on 0.18µm CMOS at these frequencies. The LNA gains above 10dB, with IP3 as high as –3dBm. Best 50 ohms input impedance match is slightly moved to higher frequencies (fig. 6) due to a small variation in the CMOS process from individual transistor measurements used in the designs to the final process used for the LNAs' tapeout. Nevertheless, input matching represents smaller than –12dB of return loss in which is more than adequate for the frequencies involved. *Backing off* technique reduced by approximately 1.5 dB the final LNAs' noise figure.

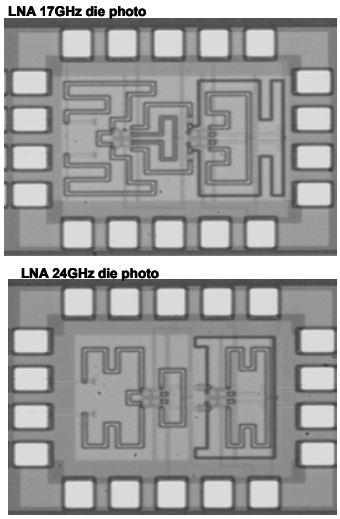


Figure 7: Die photo: 17GHz and 24GHz LNAs both LNAs,

Acknowledgments

D. Martin and K.A.Truong for outstanding layout efforts; S. Pawlowski and S. Borkar, for support in this project.

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