More Theorems

T6	$B \cdot C = C \cdot B$	
T6'	$B + C = C + B$	Commutativity
T7	$(B \cdot C) \cdot D = B \cdot (C \cdot D)$	
T7'	$(B + C) + D = B + (C + D)$	Associativity
T8	$(B \cdot C) + (B \cdot D) = B \cdot (C + D)$	
T8'	$(B + C) \cdot (B + D) = B + (C \cdot D)$	Distributivity
T9	$B \cdot (B + C) = B$	
T9'	$B + (B \cdot C) = B$	Covering
T10	$(B \cdot C) + (B \cdot \overline{C}) = B$	
T10'	$(B + C) \cdot (B + \overline{C}) = B$	Combining
T11	$(B \cdot C) + (\overline{B} \cdot D) + (C \cdot D) = B \cdot C + \overline{B} \cdot D$	
T11'	$(B + C) \cdot (\overline{B} + D) \cdot (C + D) = (B + C) \cdot (\overline{B} + D)$	Consensus
T12	$\overline{B_0 \cdot B_1 \cdot B_2 \ldots} = (\overline{B_0} + \overline{B_1} + \overline{B_2} + \cdots)$	
T12'	$\overline{B_0 + B_1 + B_2 + \cdots} = (\overline{B_0} \cdot \overline{B_1} \cdot \overline{B_2} \cdots)$	De Morgan's Theorem

- The theorems are the usual things we're familiar with from algebra, including commutativity, associativity, and distributivity. There's also covering, combining, and consensus, which are new.
- De Morgan's Theorem is extremely useful and should be studied carefully.

$\overline{A\,B} = \overline{A} + \overline{B}$

T8'

$(B+C)(B+D) =$

$B + CB + BD + CD$

$B + B(C+D) + CD$

$B(1 + C + D) + CD$

$B(1) + CD$

$B + CD$

Equation Minimization

- Using the Axioms and Theorems of Boolean Algebra, we can simplify expressions. For example

$$y = \overline{A}\,\overline{B}\,\overline{C} + A\overline{B}\,\overline{C} + A\overline{B}C$$

- Can be simplified using distribution in the first two terms

$$y = \overline{B}\,\overline{C}(A + \overline{A}) + A\overline{B}C$$

- But $A + \overline{A} = 1$ and anything times 1 is itself

$$y = \overline{B}\,\overline{C}(1) + A\overline{B}C = \overline{B}\,\overline{C} + A\overline{B}C$$

- Can we do better? Notice the simplification resulted because the first two terms only differed by 1 bit, A. But the last two terms also differ in only 1 bit, C. We could have combined these two terms as well, giving us the same complexity in the minimized term.
- But we can also be clever and duplicate the middle term! That's because $A + A = A$. Show that we then can get down to

$$y = \overline{B}\,\overline{C} + A\overline{B}$$

$$y = \overline{A}\,\overline{B}\,\overline{C} + A\,\overline{B}\,\overline{C} + A\,\overline{B}\,\overline{C} + A\,\overline{B}\,C$$

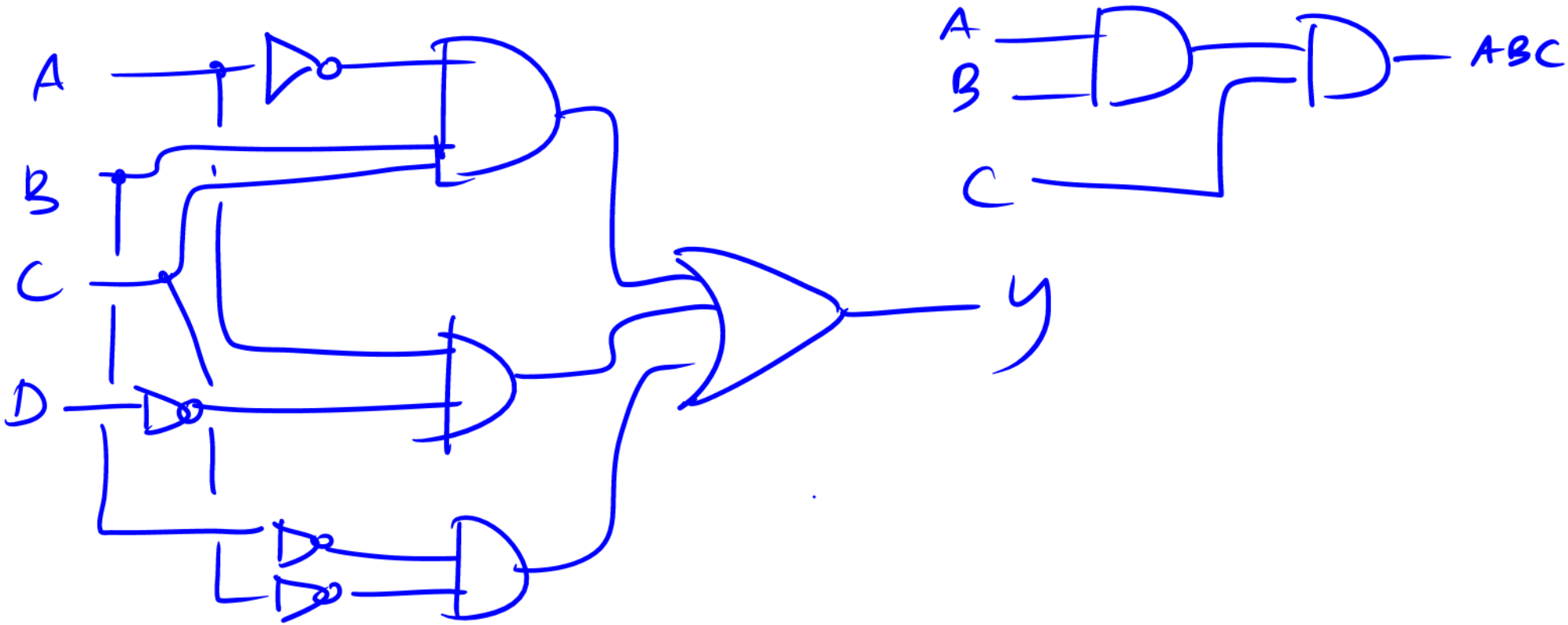
$$y = \underbrace{(\bar{A} + A)}_{1}\,\bar{B}\,\bar{C} + A\,\bar{B}\,\underbrace{(C + \bar{C})}_{1}$$

$$y = \bar{B}\,\bar{C} + A\,\bar{B}$$

From Logic to Gates

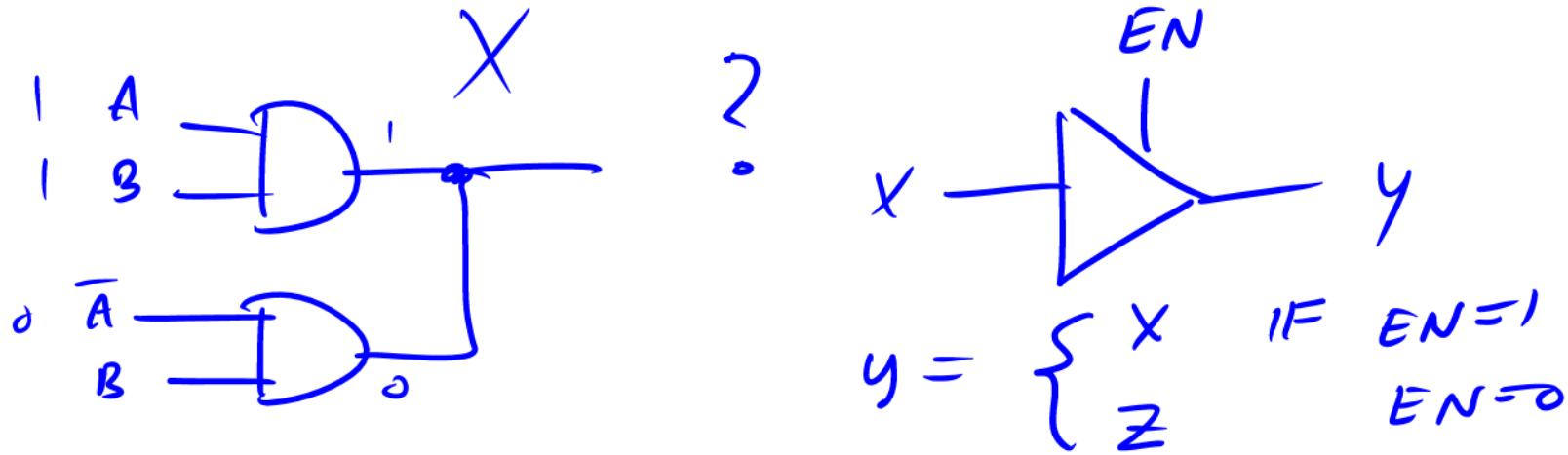
- It's now very easy to see how we can synthesize any Boolean expression using logic gates. For instance, to realize an expression in sum of products terms, we first form the miterms using AND gates and then we OR the outputs.

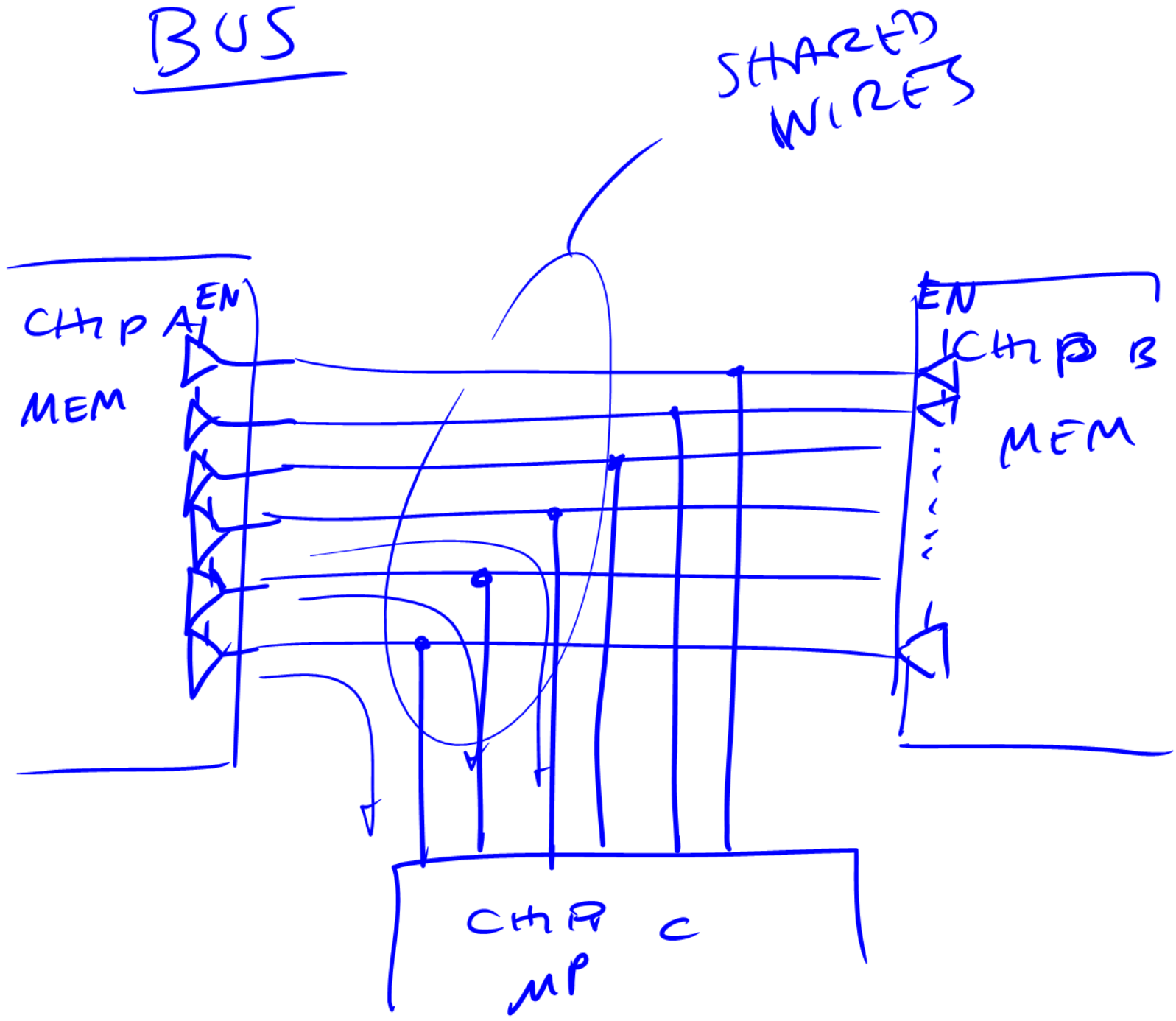
$$y = \bar{A}BC + \bar{C}\bar{B} + A\bar{D}$$



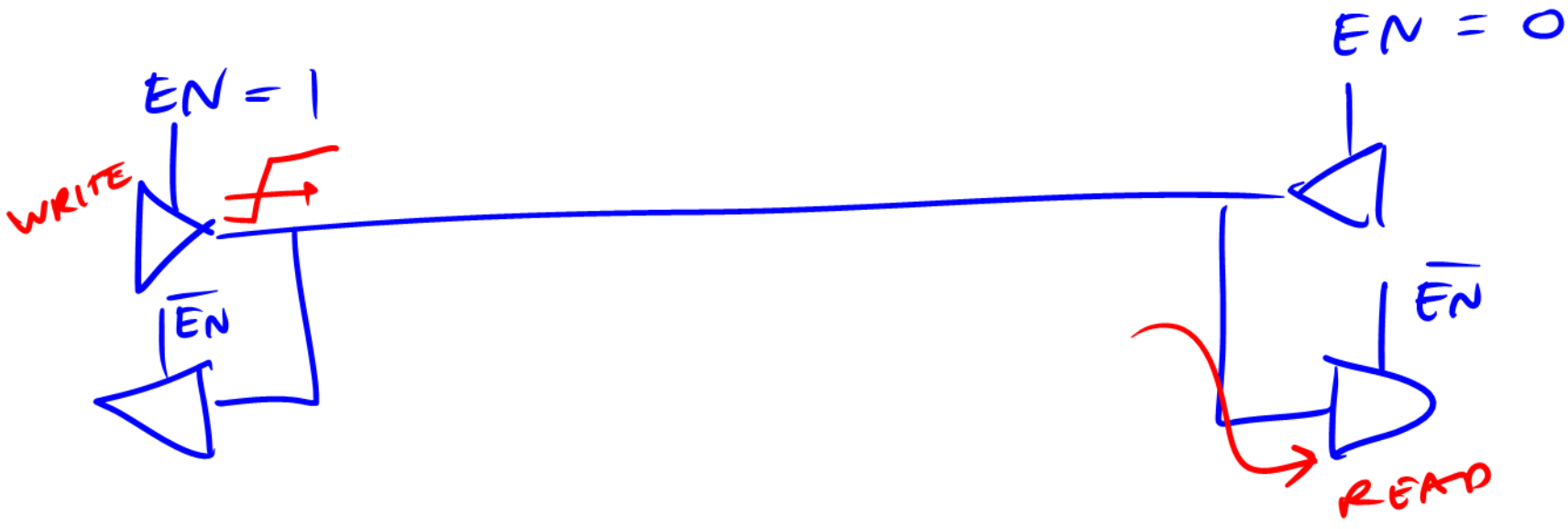
Other Possible Ouputs

- When an illegal output occurs in a logic gate, we denote that as 'X'. Suppose we have a circuit where there is a contention between two logic gates. The output will then be an illegal output (not a well defined '0' or '1') and the circuit may not function correctly or as expected.
- The same notation is used for a "don't care" output, in other words if we don't care about a particular output, so be careful.
- Many logic gates have an "enable" input that can put the output into a third state, known as a floating or high impedance (high-'Z') state. This is known as a 'Z' state for this reason.
- A common block with this functionality is a tristate buffer. This is very useful in busses and other circuits where multiple gates drive the same output. Now a contention is not longer present as long as only one gate is enabled.



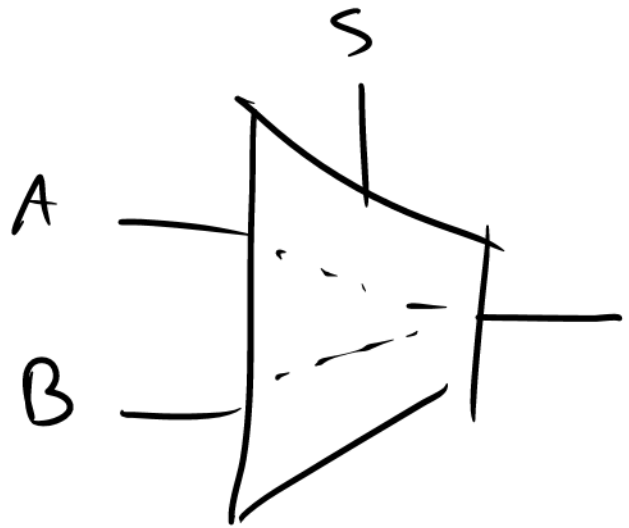

BUS
SHARED WIRES
EN
CHIP A
MEM
EN
CHIP B
MEM
CHIP C
MP

BI-DIR BUS



MUX

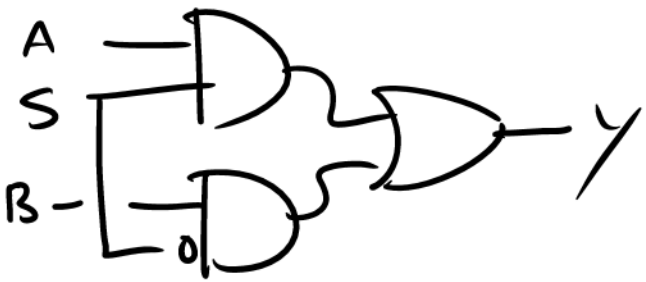
- A MUX or multiplexer simply selects one of its inputs based on the “select” input. You can think of it as a three input logic gate with the truth table shown below.
- A MUX can be implemented using a two-level logic, or using tri-state buffers.



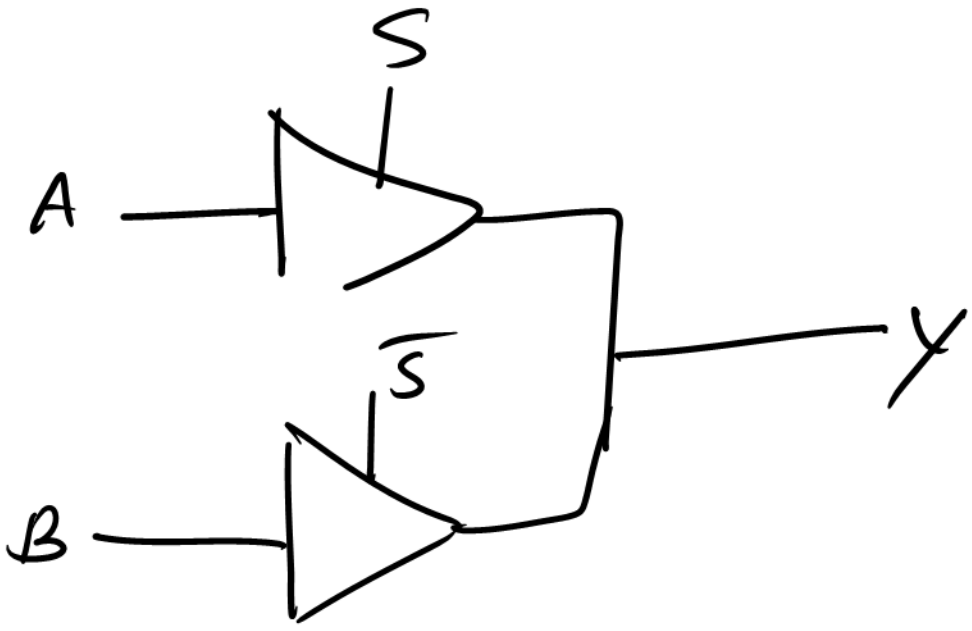
$$Y = \begin{cases} A & S = 1 \\ B & S = 0 \end{cases}$$

A	B	S	Y
A	B	1	A
A	B	0	B

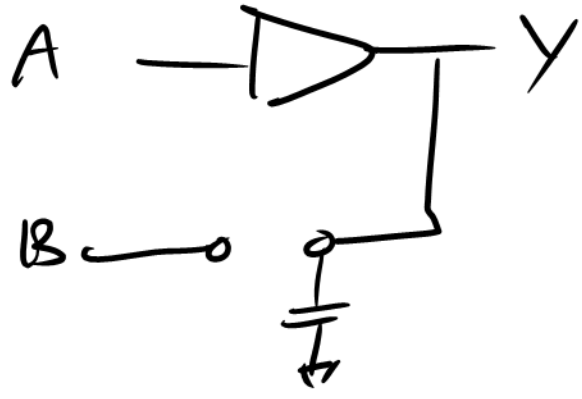
$$y = A \cdot S + B \cdot \bar{S}$$



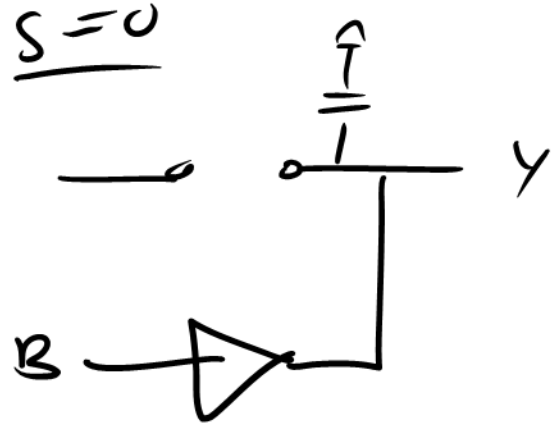
ANOTHER MUX (TRI-STATE BUFFER)



S=1

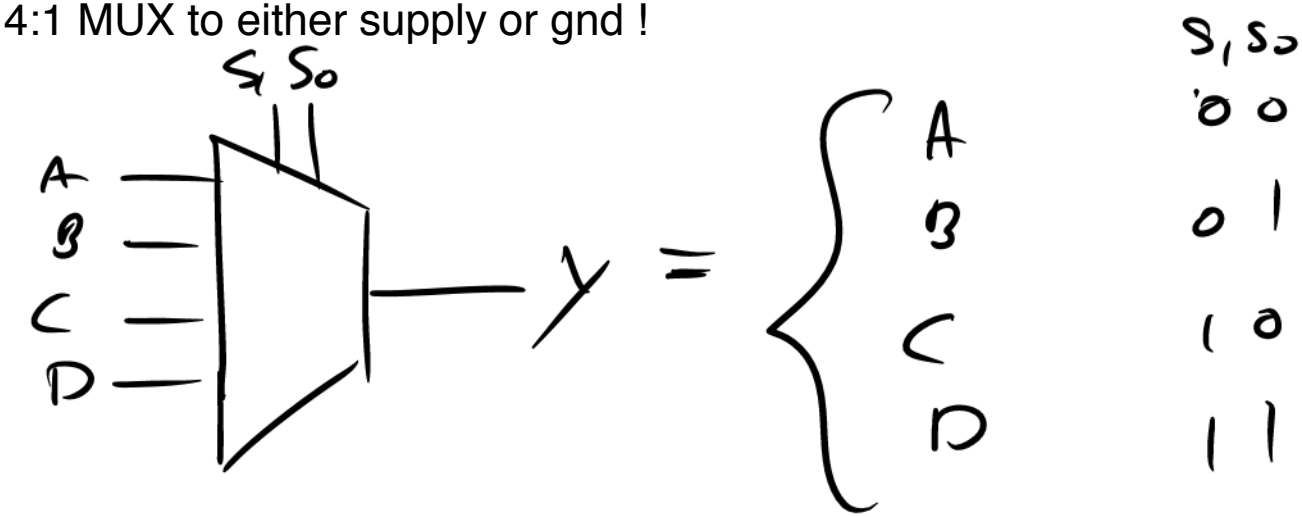


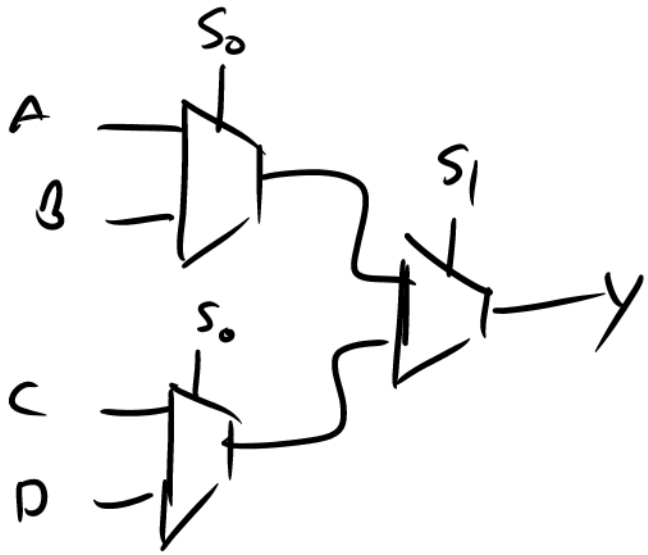
S=0



4:1 MUX

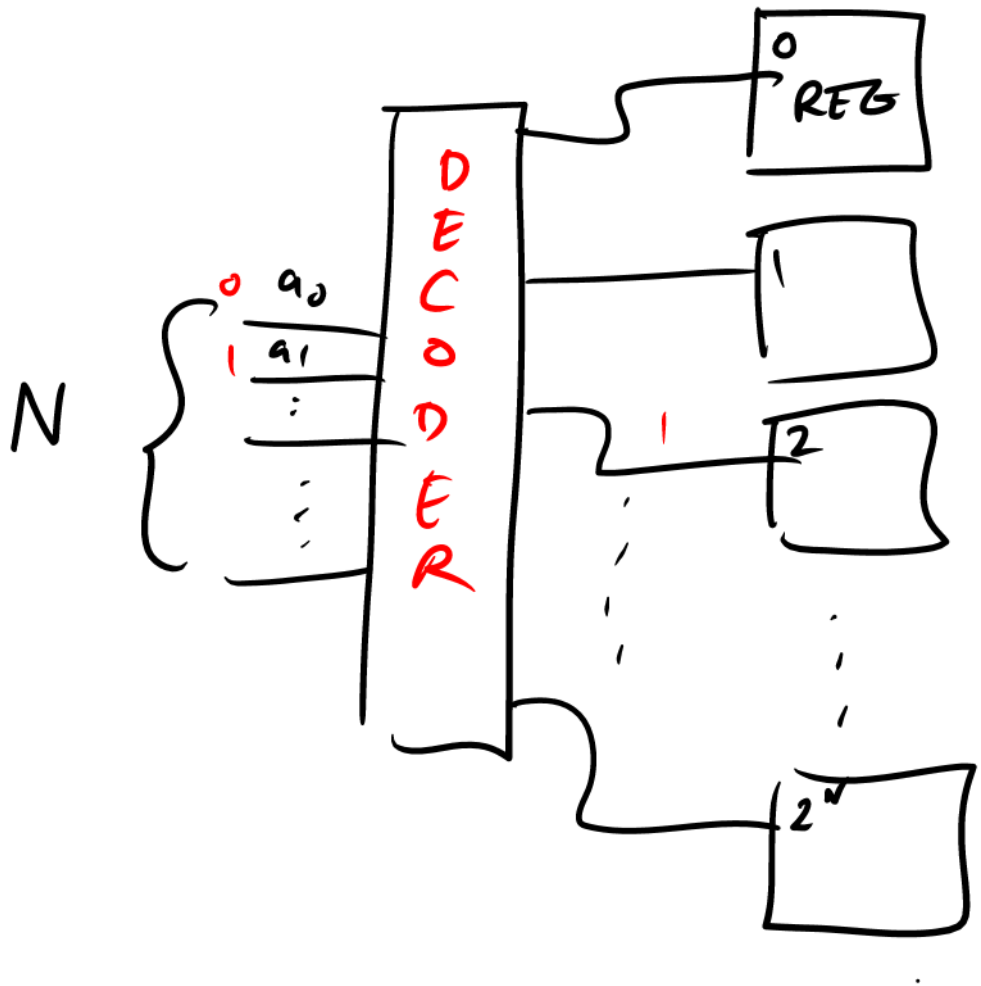
- Higher order MUX circuits are also handy and can be realized in different ways.
- Notice that any truth table with 2 inputs can be realized by connecting the inputs of the 4:1 MUX to either supply or gnd !

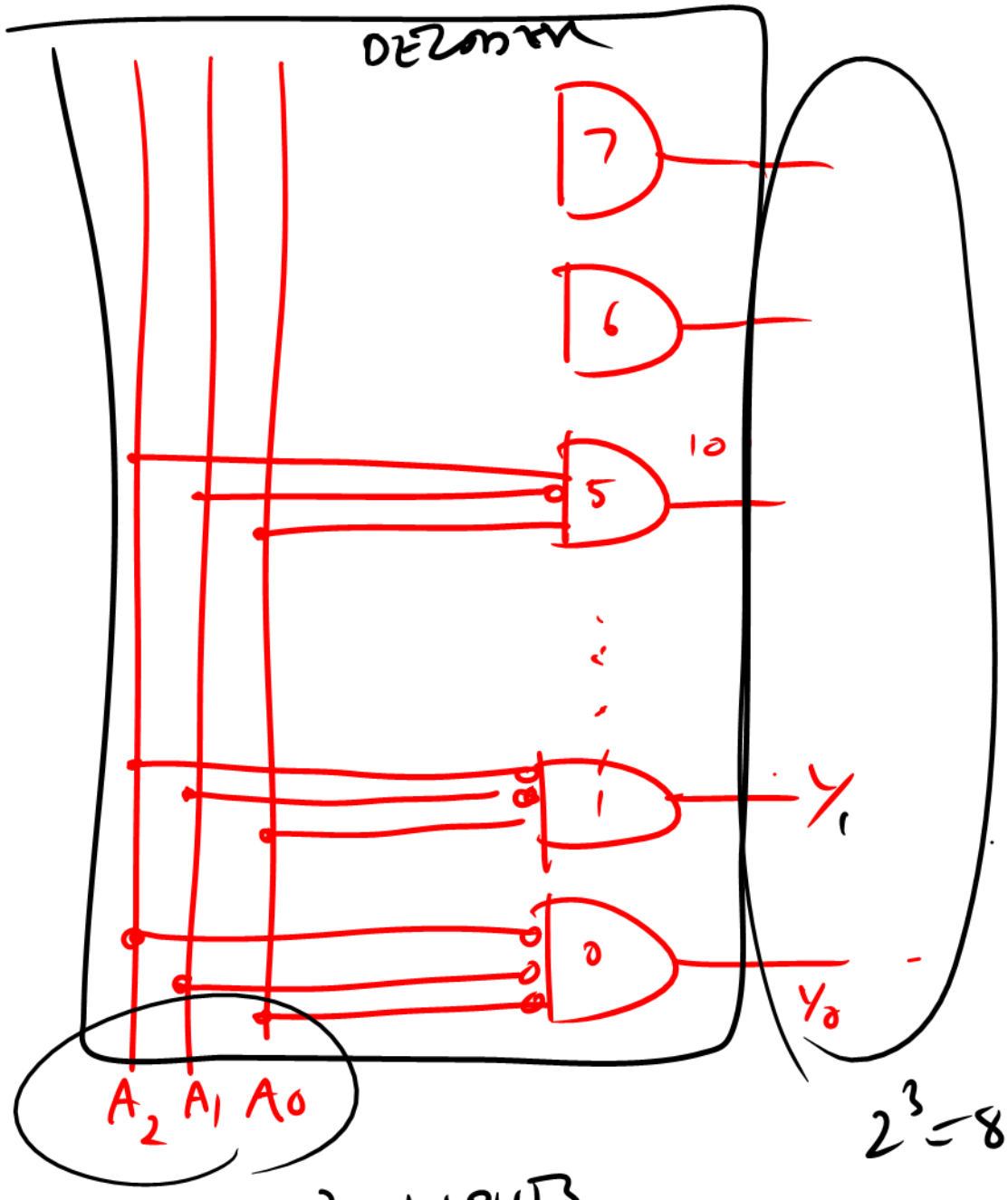




Decoders

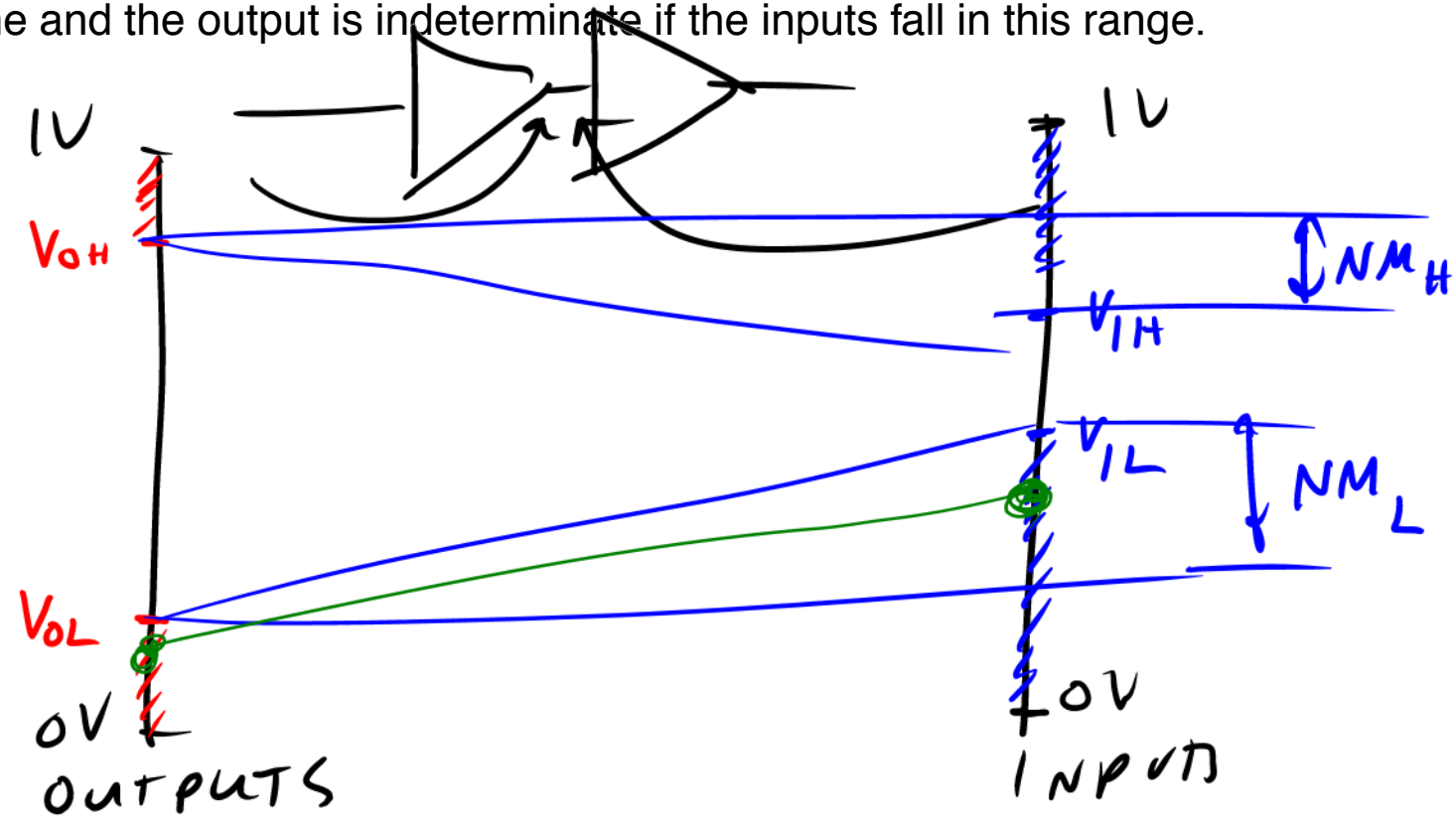
- A decoder is very handy when building a memory. There are N inputs and 2^N outputs. Only one output is selected at a time.

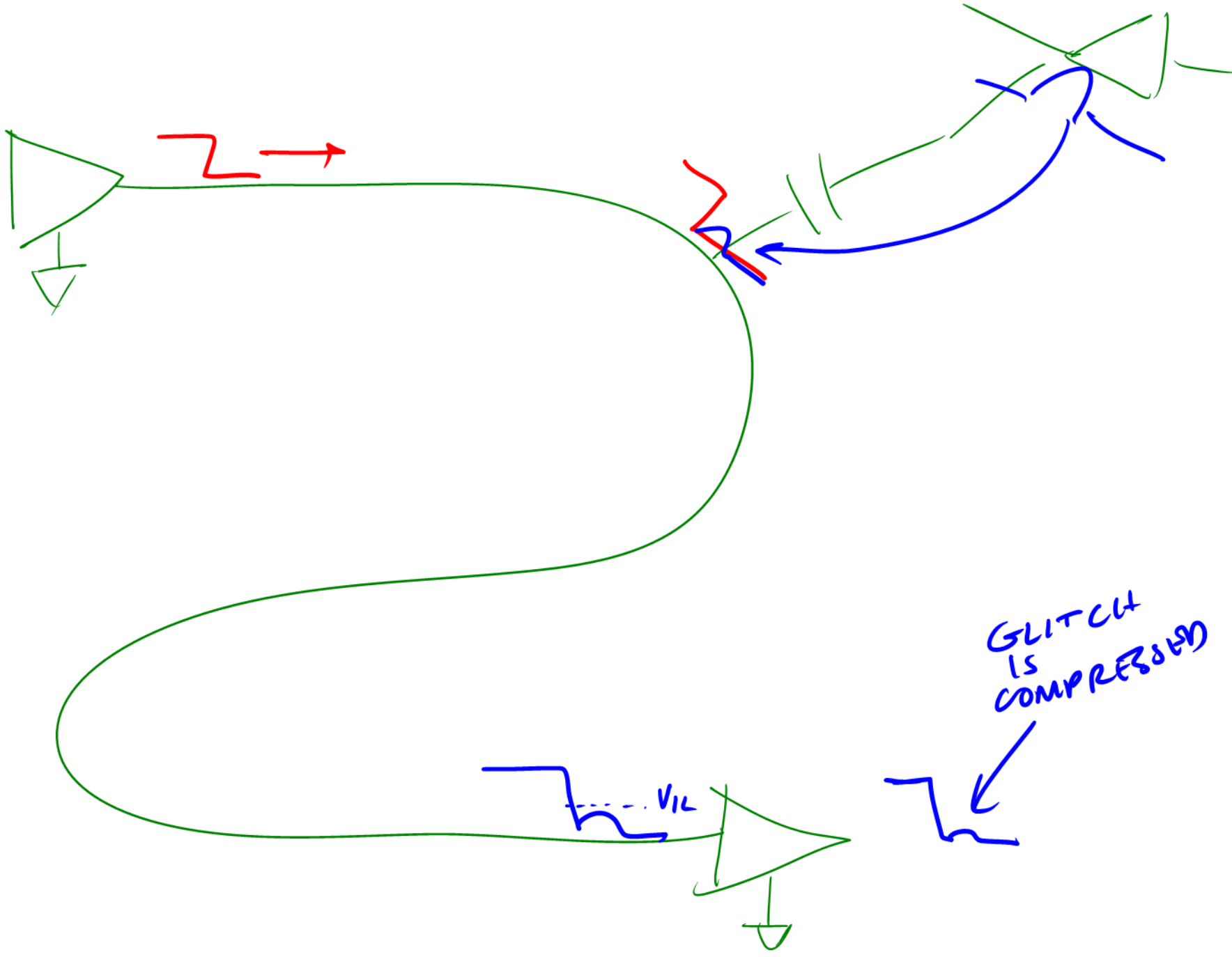



DECODER
7
6
5
4
1
0
Y_1
Y_0
A_2 A_1 A_0
3 - INPUTS
$2^3 = 8$ OUTPUTS

Logic Levels

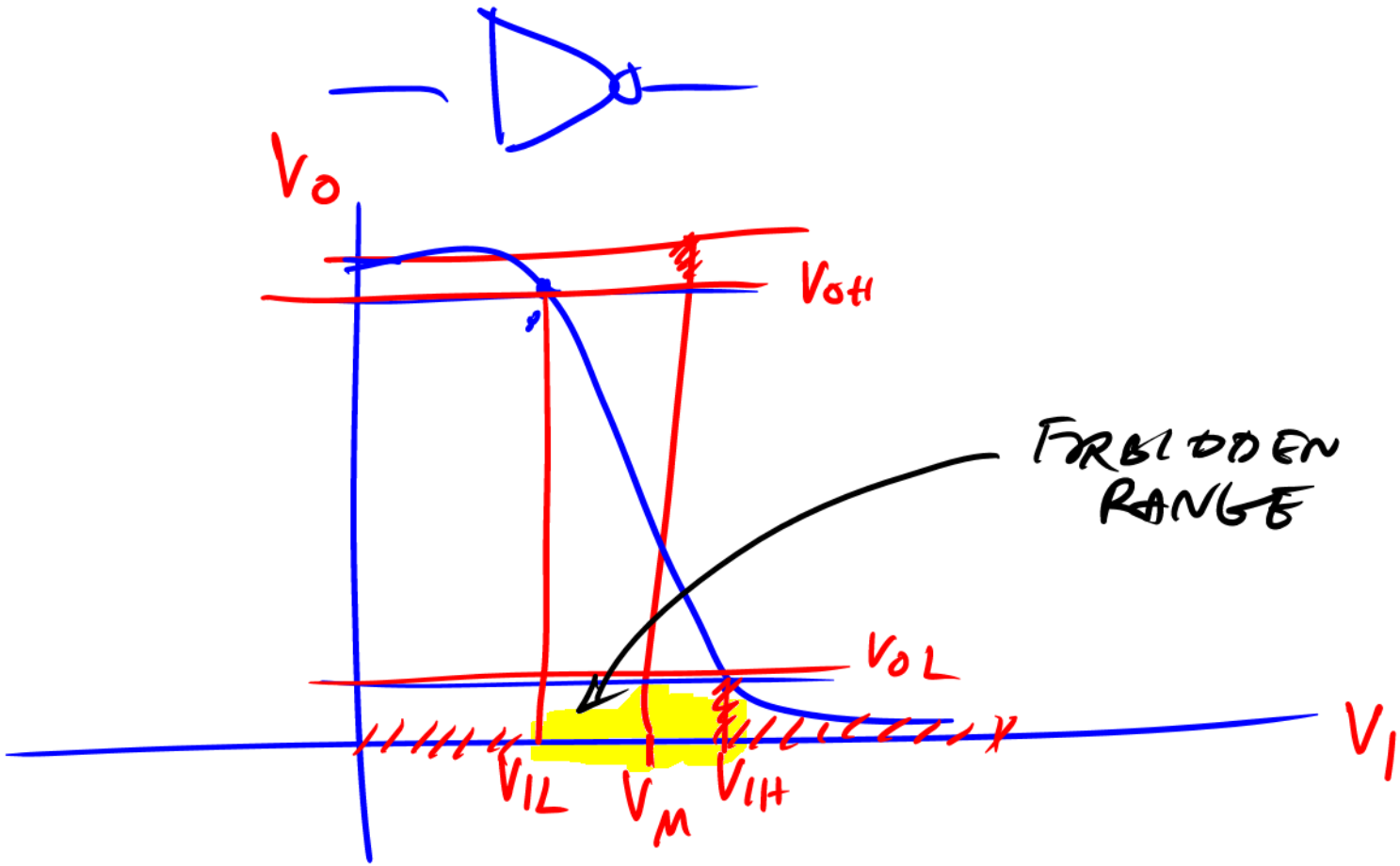
- In a real circuit, the actual voltage waveforms take on a continuous range of values. In order for our digital abstraction to work, we have to define the valid range of logic levels that we will interpret as a zero or one.
- Consider one gate driving another gate. For the driver gate, we call the V_{OH} the smallest valid "high" output. Likewise, we call V_{OL} the largest valid "low" output.
- For the receiver gate, we call the smallest valid "high" input level V_{IH} and the largest valid "low" input level V_{IL}. Any input outside this range are in the forbidden zone and the output is indeterminate if the inputs fall in this range.




GLITCH
IS
COMPRESSED
VIL

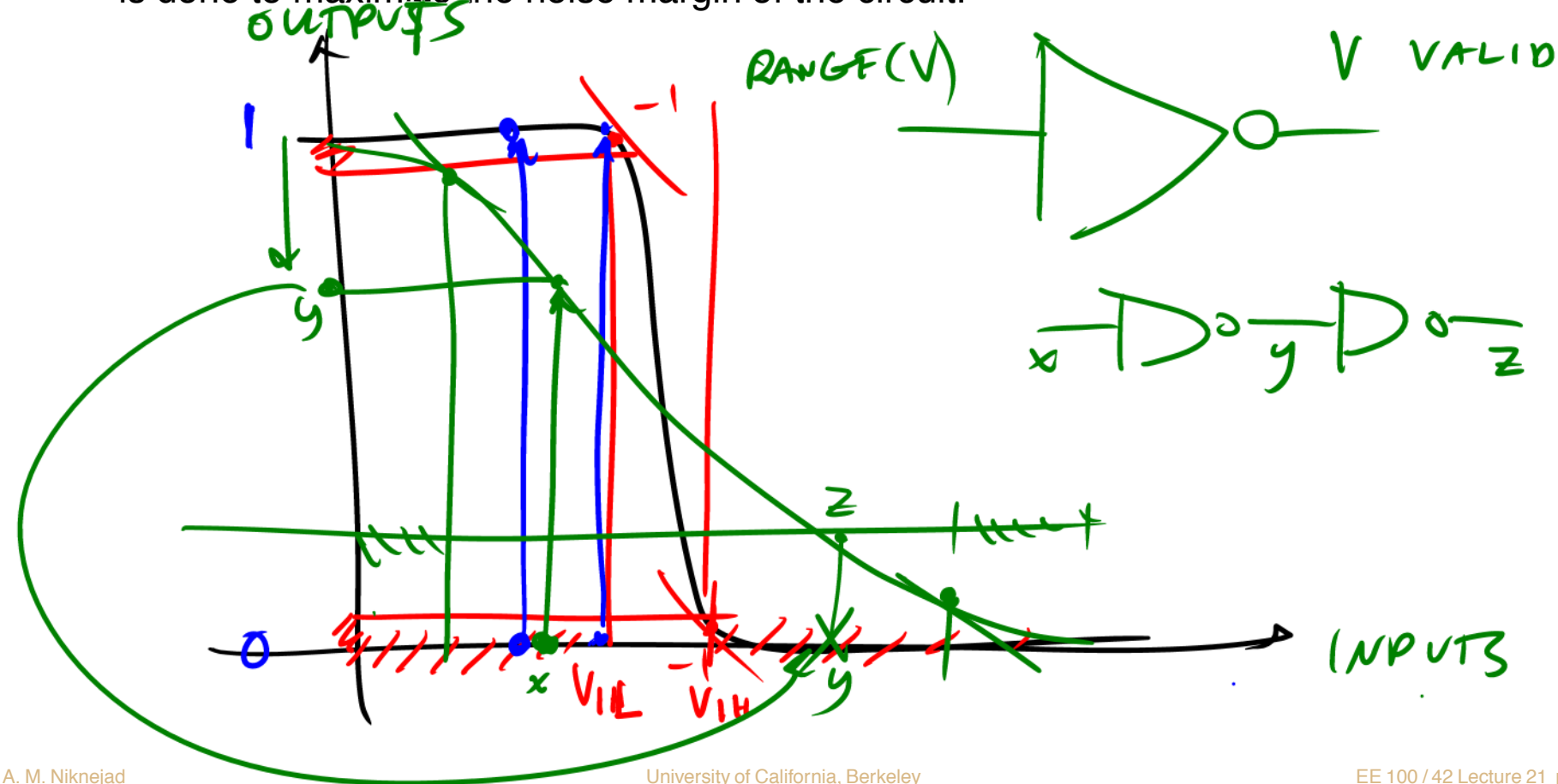
Noise Margin

- Notice that if $V_{OL} < V_{IL}$ and $V_{OH} > V_{IH}$ we have some *noise margin* in our circuit. In other words, the output of one gate can vary by as much as $NM_H = V_{OH} - V_{IH}$ and the data will still be valid on the high side. Likewise, the low side noise margin is $NM_L = V_{IL} - V_{OL}$.
- This is an important concept because it means that digital logic gates "clean up" their inputs and allow cascading of gates to occur without ever worrying about the NM decreasing. In fact, quite the opposite happens.

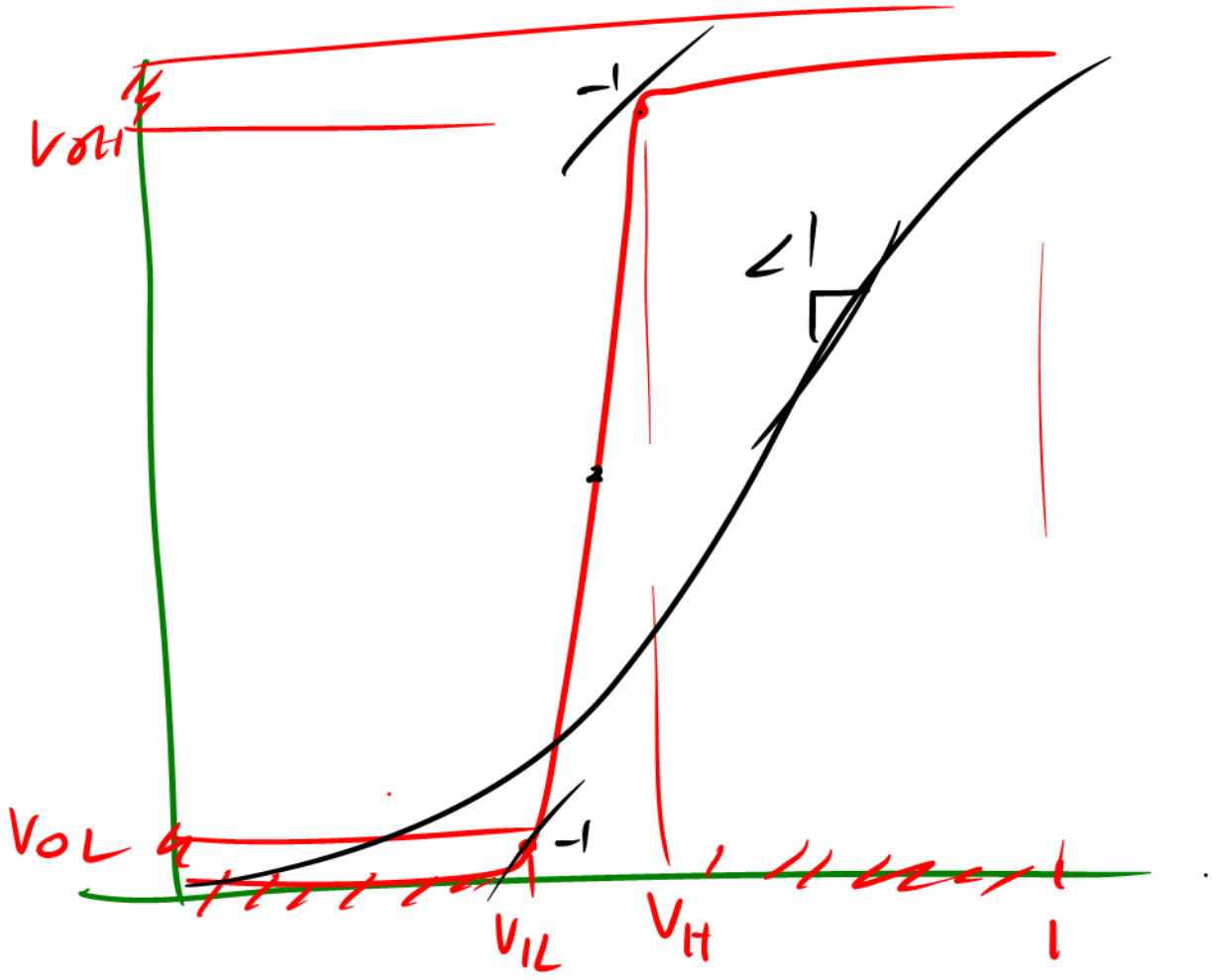


DC Transfer Characteristic

- The transfer characteristics for an ideal logic inverter and a real inverter are shown below. Note that for an ideal inverter there's a threshold voltage at the midpoint. If the signal is below the midpoint, the output saturates to the supply. If it's above, it saturates to the ground potential.
- A real curve as a transition region in which the output voltage is not well defined (high or low). This is the forbidden region for the gate.
- The V_{OH} and V_{OL} are defined by the points where dV_o/dV_i is equal to -1. This is done to maximize the noise margin of the circuit.

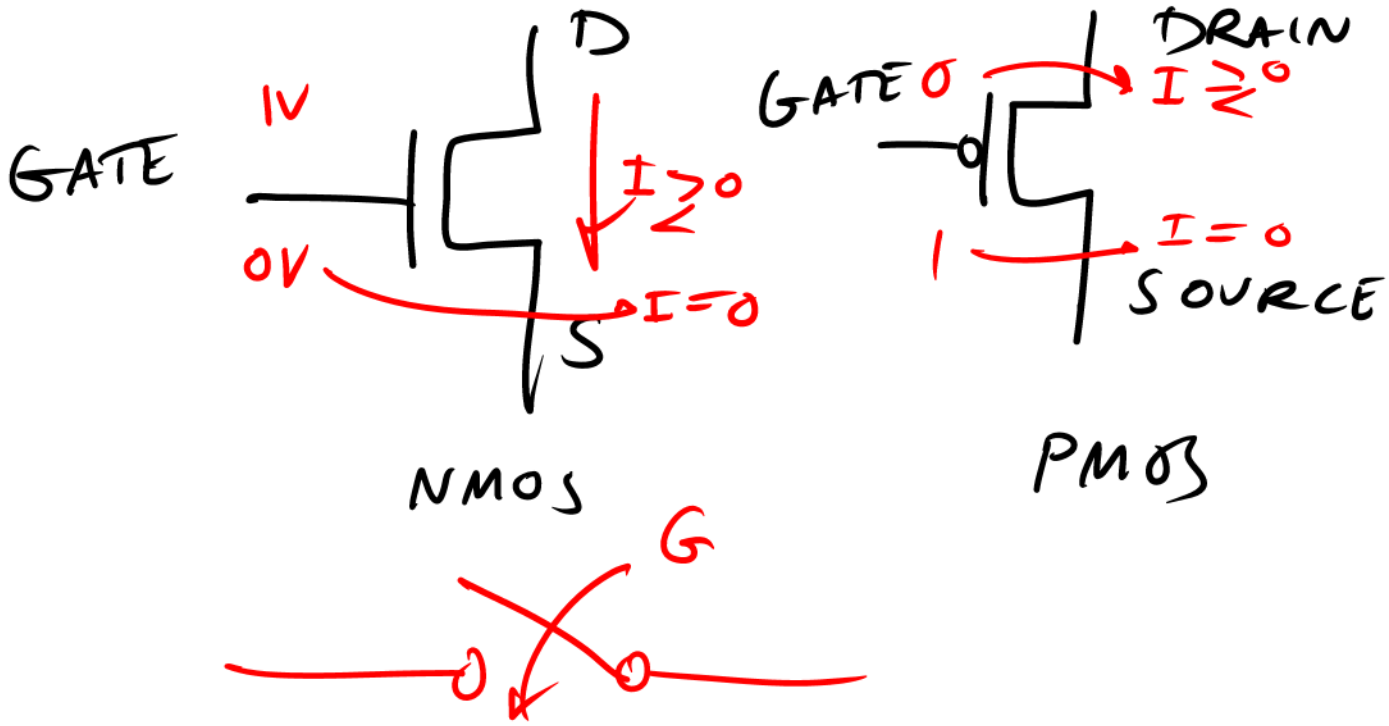


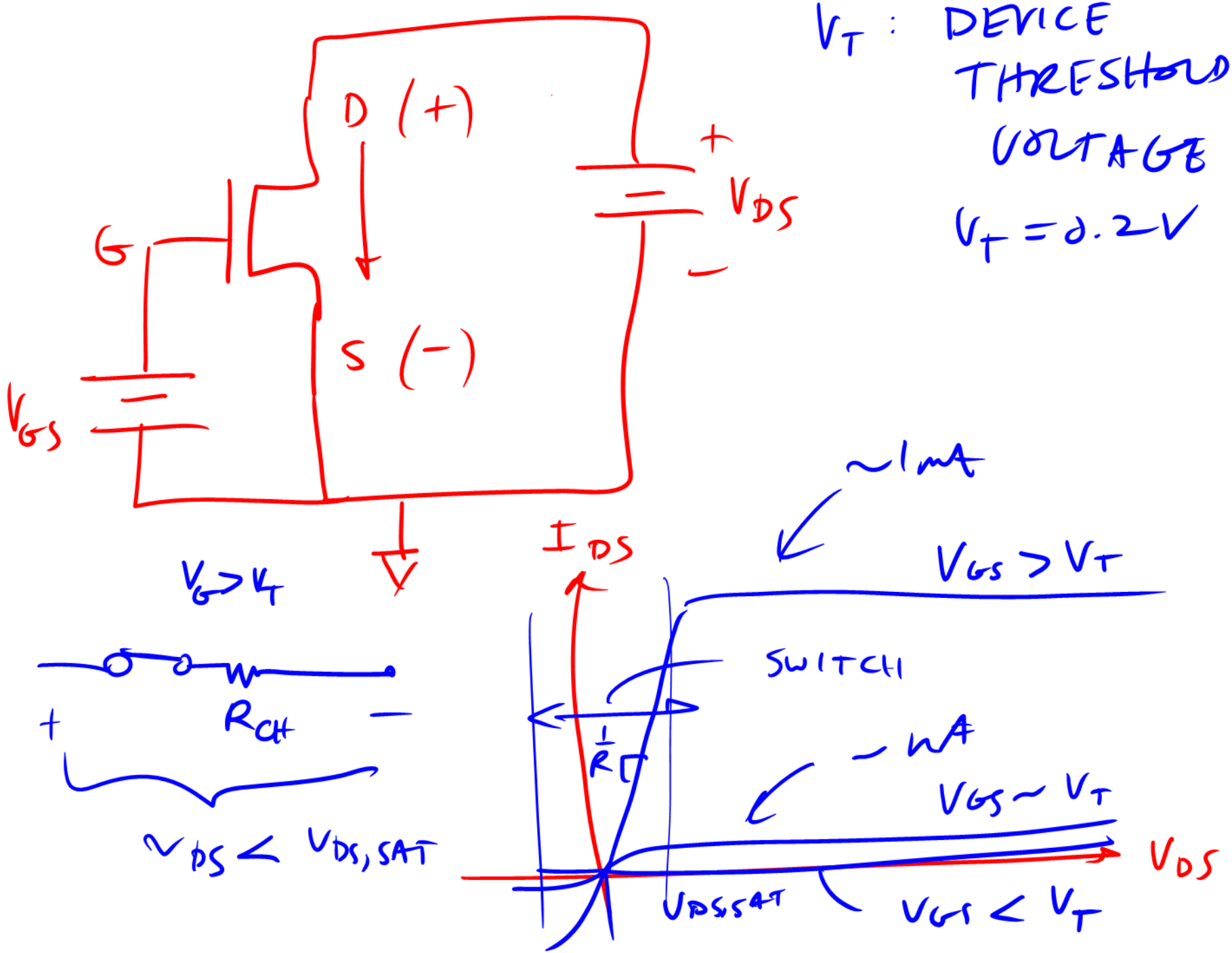
Good BUFFER



CMOS Transistors

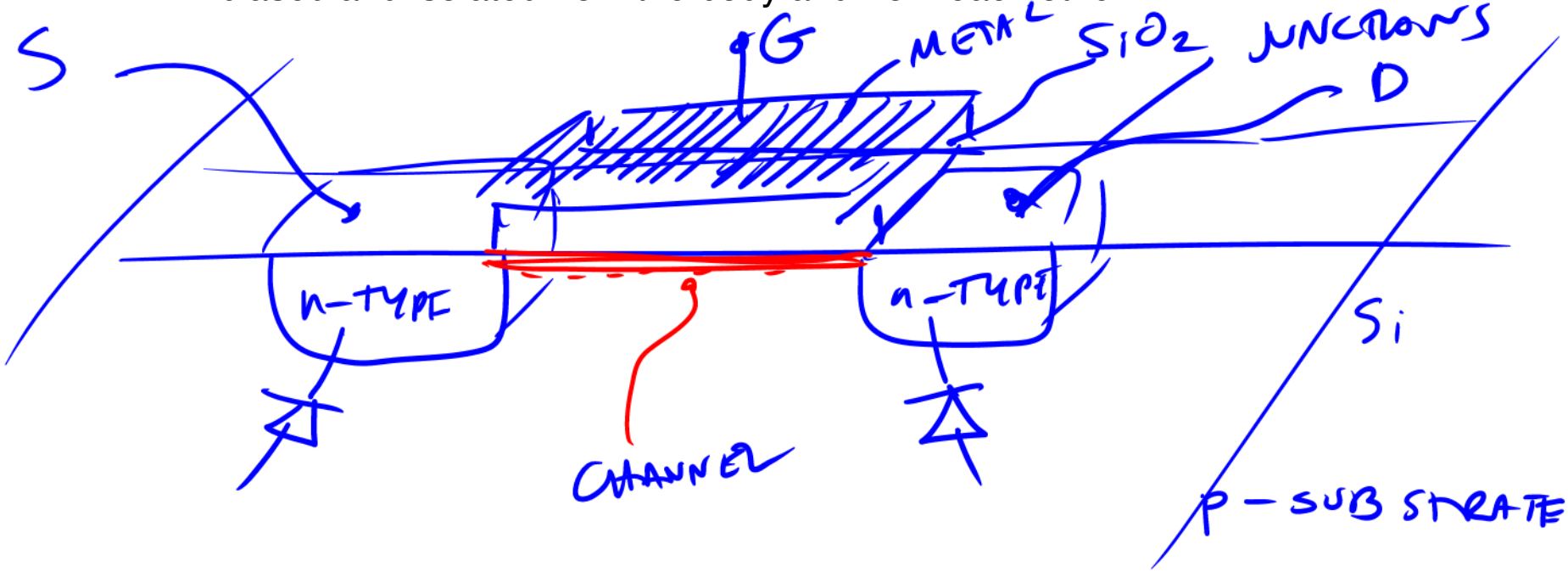
- The vast majority of logic gates today are built from silicon CMOS transistors. CMOS transistors have been the driving force of electronic miniaturization and power scaling for the past few decades.
- CMOS transistors are used to make logic gates, memory cells, and buffers and amplifiers.
- The level of integration has been growing exponentially for the past four decades and today you build a chip with 1 billion transistors!




V_T : DEVICE THRESHOLD VOLTAGE
$V_T = 0.2V$
D (+)
S (−)
G
V_{GS}
V_{DS}
+
−
$V_G > V_T$
I_{DS}
~1mA
$V_{GS} > V_T$
SWITCH
R_{CH}
+
−
$\frac{1}{R_{CH}}$
~0A
$V_{GS} \sim V_T$
V_{DS}
$V_{DS} < V_{DS,SAT}$
V_{DSSAT}
$V_{GS} < V_T$

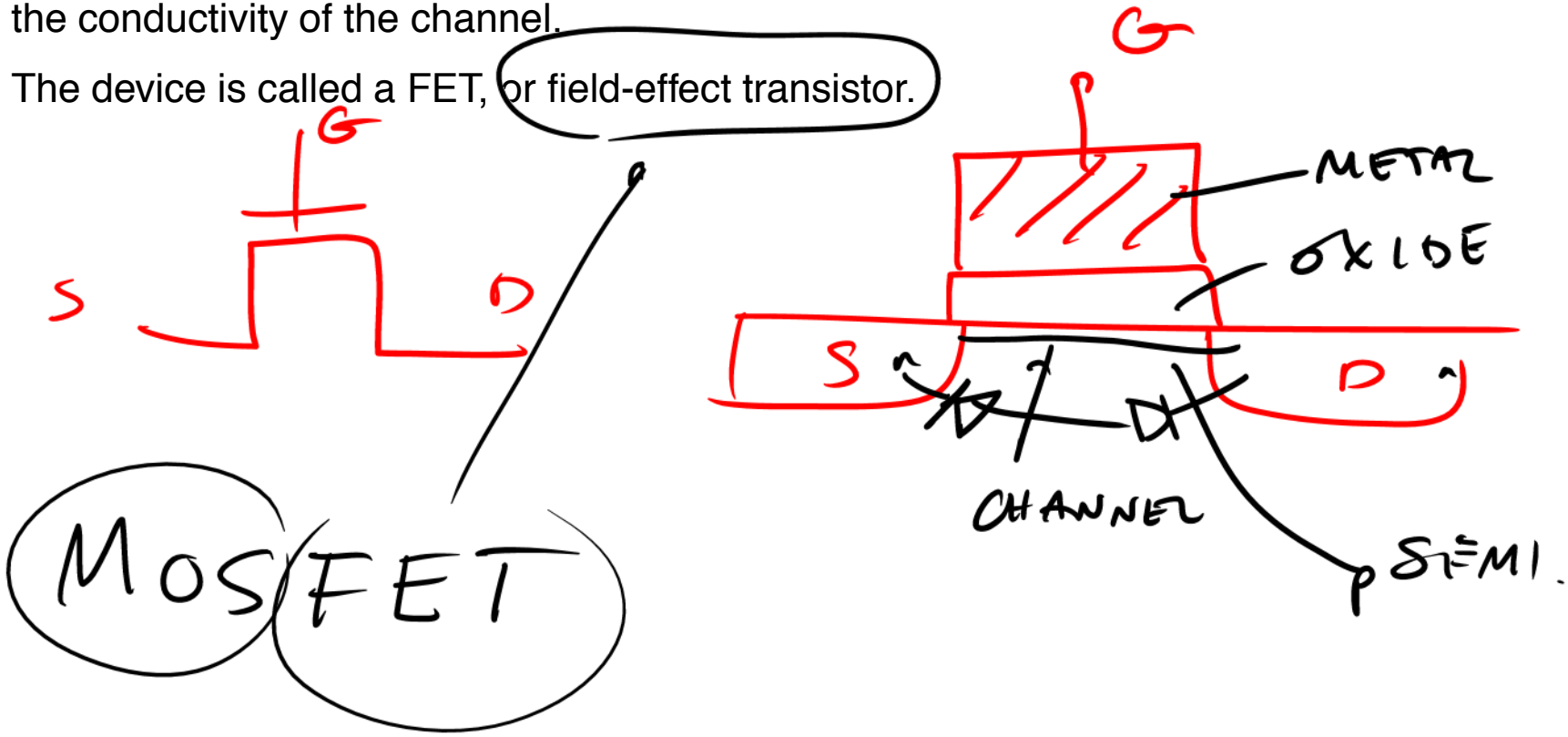
Fabrication

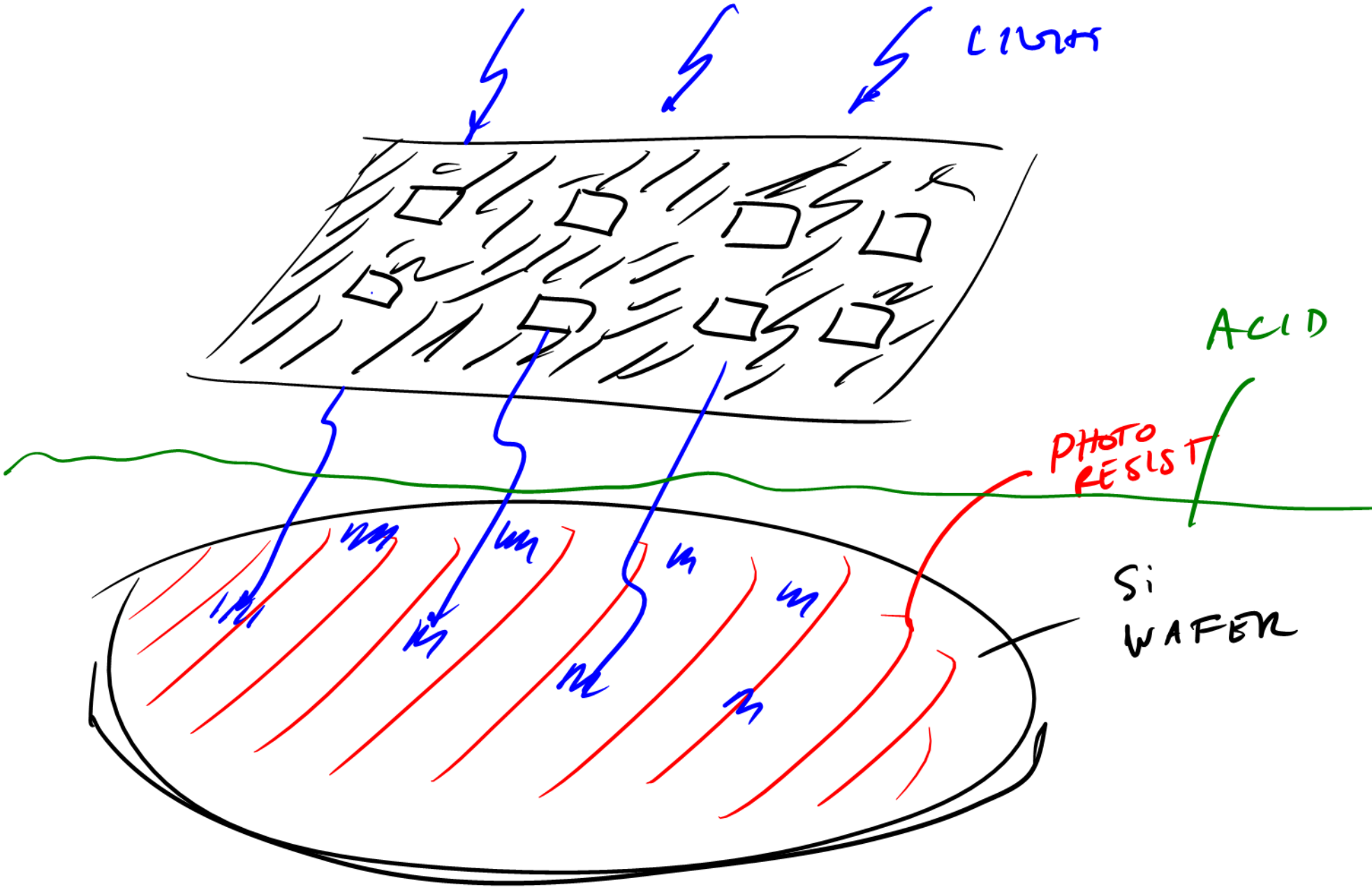
- CMOS stands for Complementary MOS, and MOS stands for Metal-Oxide-Silicon. A MOS sandwich is the basic structure which forms a capacitor between the gate and the body of the transistor. The structure is fabricated by lithographically defining an opening in the silicon where the native SiO_2 oxide is grown. A p-type silicon is usually used for the body.
- To complete the transistor, two new terminals are added, the source and drain. The source and drain are grown by doping openings in the silicon adjacent to the gate. Under normal operating conditions, the body biased at the most negative potential (ground), and that means that the source/drain junctions are reverse biased and isolated from the body and from each other.

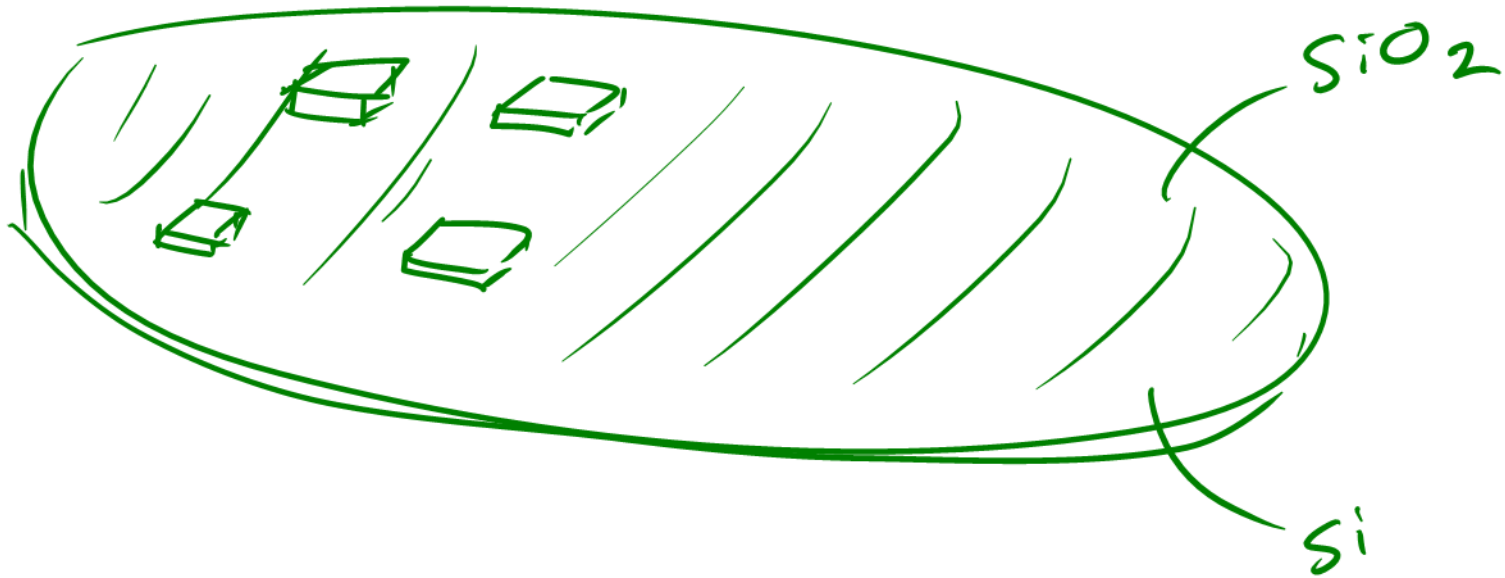


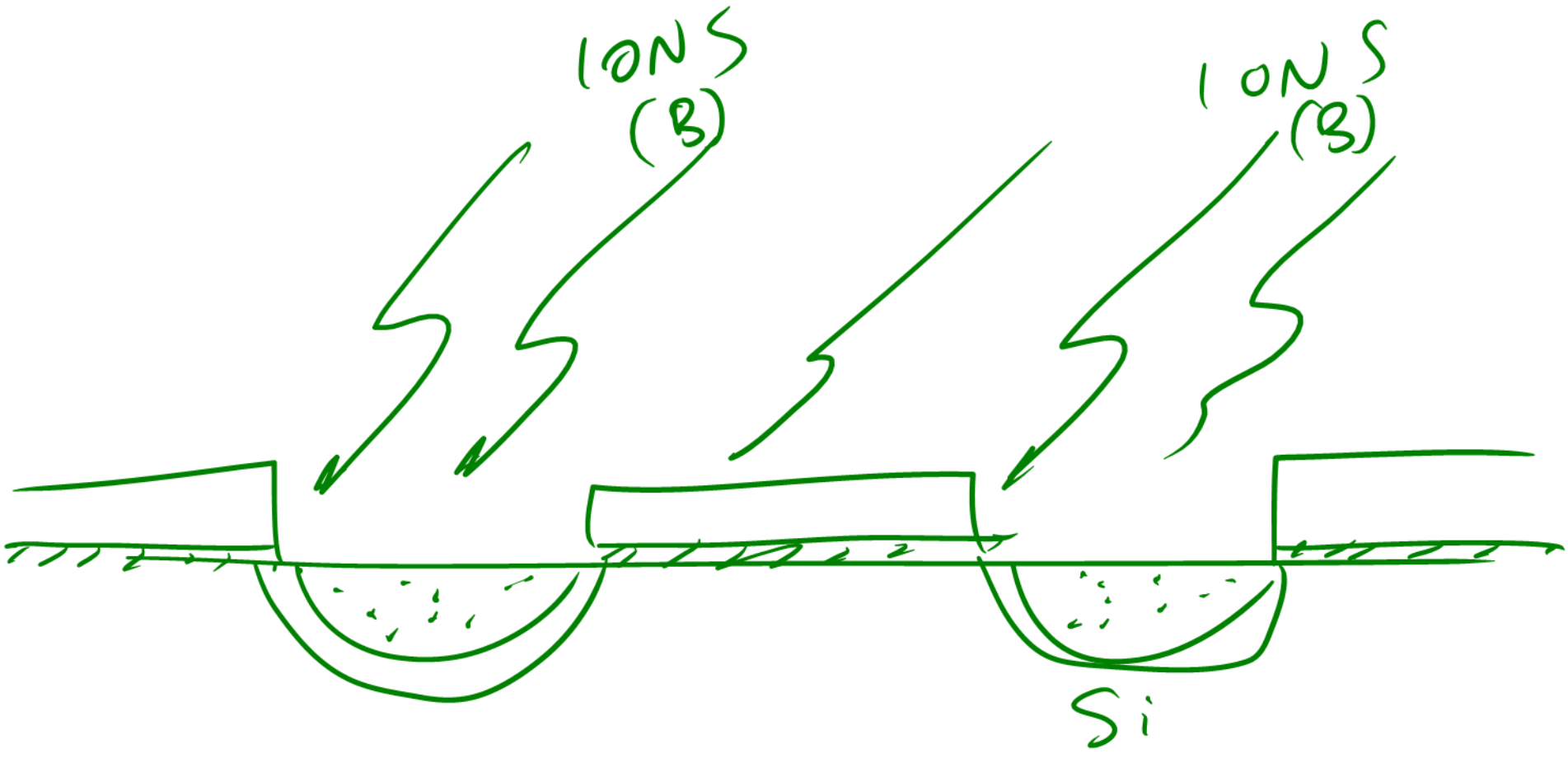
nMOS Operation

- Ignoring the gate terminal for now, since the source/drain form two back to back diodes, no current can flow through the device.
- If a positive voltage is applied at the gate terminal, it begins to attract negative charge carriers to the surface. It's a capacitor after all and in equilibrium we would expect the positive charge on the gate to be balanced by negative charge at the surface of silicon. Thus we can say that a "channel" begins to form due to the field-effect of the gate terminal.
- If the voltage is made sufficiently large, the channel becomes conductive enough that current can flow from the source to the drain. Thus the gate voltage modulates the conductivity of the channel.
- The device is called a FET, or field-effect transistor.




LIGHT
ACID
PHOTO RESIST
Si WAFER


SiO2
Si


IONS
(B)
IONS
(B)
Si