TOPICS

1. Q, I, V, $P = I \cdot V$, E

$$I = 1A \cos \omega t$$
$$V = 5V \cos(\omega t + 45^\circ)$$

} P_{av}, Q ↑ REACTIVE POWER

2. KVL, KCL
3. NODAL ANALYSIS (ON EXAM)
4. RESISTIVE DIVIDERS (ON EXAM)*
5. NORTON/THEV. (ON EXAM)*
6. LINEARITY & SUPERPOSITION
7. AMPS / OP-AMPS (ON EXAM) / MT #1

MT 2

1. CAPACITANCE (EQ) $Q = CV$ $E = \frac{1}{2} C V^2$ / CHARGE SHARING

2. RC CIRCUITS (ON EXAM)

SWITCHES, TIME VARYING SOURCES (STEP FUNC, SINE, OTHERS) → AC

3. AC CIRCUITS / PHASORS (ON EXAM)

4. FILTERS (EQ)

5. AC POWER

6. DIODES → • RECTIFIERS (AC → DC) HW, FW
• PEAK DETECTORS
• LEVEL RESTORE
• CLIPPERS

} ON EXAM

DIGITAL

1. BINARY SIGNALS / BIN. REP.
2. LOGIC GATES / NOISE MARGIN
3. BOOLEAN ALGEBRA (AXIOMS / THMS)

   DMT (ON EXAM)

4. CMOS TECHNOLOGY
5. CMOS TRANSISTORS → AS SWITCHES (ON EXAMS)
   - NMOS MAKE STRONG ZEROS
   - PMOS MAKE STRONG ONES
6. TRUTH TABLE ↔ BOOLEAN EXPRESSION
   ↔ GATE LEVEL ↔ CMOS CIRCUIT
   (ON EXAM)

- SEQUENTIAL CIRCUITS (MEMORY)

BISTABLE CIRCUITS

- LATCHES } DIFF.
- FLIP-FLOPS }

- STATE TRANSITION DIAGRAM
- STATE TRANSITION LOGIC

} (E.Q.)

6Q

1) EASY PROBLEMS

2) NODAL ANALYSIS / AC (PHASORS)

3) RC PROBLEM (THEV/NORTON)

4) DIGITAL : LOGIC, TABLE ↔ BOOL ↔ GATES ↔ CMOS

5) AMP/OP-AMPS

6) DIODES