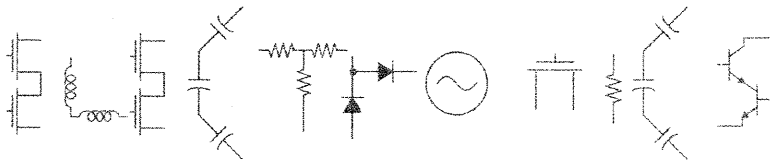


SOLUTIONS

Name:
SID:
EE42 OR EE100

University of California, Berkeley *Spring 2010*
EE 42/100 *Prof. A. Niknejad*

Final Exam (closed book)
Wed•••day, May 12, 2010

Guidelines: Closed book. You may use a calculator. Do not unstaple the exam. In order to maximize your score, write clearly and indicate each step of your calculations. We cannot give you partial credit if we do not understand your reasoning. Feel free to use scratch paper but transfer your final answer to the exam.

Electron charge $q = 1.60217646 \times 10^{-19}$ C.

KCL: Kirchhoff's Current Law states that the net current flow into a node (or super-node or any closed surface) is zero.

$$\sum I_k = 0$$

KVL: Kirchhoff's Voltage Law states that the net voltage drop around any loop is zero.

$$\sum V_k = 0$$

Power flow into a component: (positive means power is absorbed or dissipated.

$$P = I \cdot V$$

Ohm's Law:

$$V = I \cdot R$$

or

$$I = G \cdot V$$

where $G = R^{-1}$.
Power dissipated in a resistor:

$$P = I^2 R = V^2 G$$

Resistors in series add:

$$R = R_1 + R_2 + \cdots$$

Conductances in parallel add:

$$G = G_1 + G_2 + \cdots$$

For two resistors in parallel, this implies

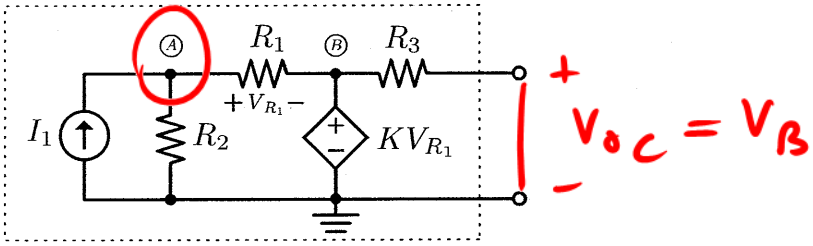
$$R_{||} = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2}}$$

When a chain of resistors are in series and connected to a voltage source, the voltage across the kth resistor is given by the voltage divider forma

$$V_k = V_s \frac{R_k}{R_1 + R_2 + \cdots}$$

SID:

1. (15 points) Consider the following linear circuit consisting of a linear dependent source and an independent current source.



(a) (5 points) Find the open circuit voltage V_{oc} using KVL. Setup the node equations by using the nodes A and B as shown.

KCL @ A

UNK

$$-I_1 + \frac{V_A}{R_2} + \frac{V_A - V_B}{R_1} = 0$$

$$V_B = K V_{R_1} = K(V_A - V_B)$$

$$(K+1) V_B = K V_A$$

WRITE DEP SOURCES IN TERMS OF NODAL VOLTAGES

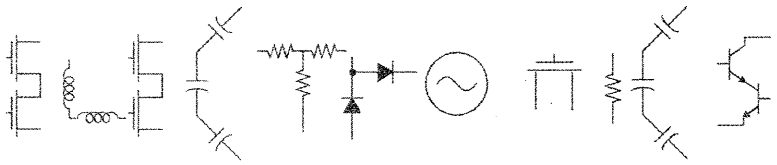
$$V_B = \frac{K}{K+1} V_A$$

$$V_A - V_B = \frac{1}{K+1} V_A$$

$$V_A \left(G_2 + \frac{G_1}{K+1} \right) = I_1$$

$$V_A = \frac{I_1}{G_2 + \frac{G_1}{K+1}}$$

$$V_B = V_{oc} = \frac{K}{K+1} \cdot \frac{I_1}{G_2 + \frac{G_1}{K+1}} = \frac{K I_1}{(K+1) G_2 + G_1}$$



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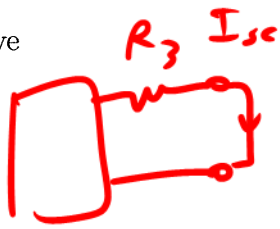
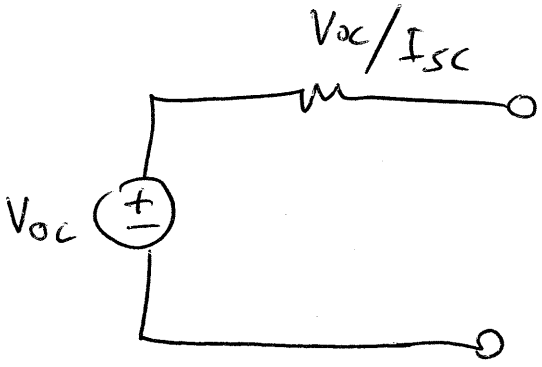
(b) (3 points)Find the short circuit current (I_{sc}). *Hint:* Try to reuse the above calculation.



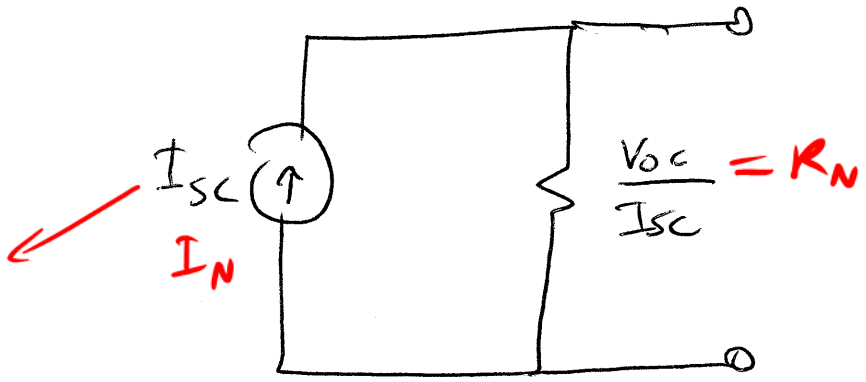
$$I_{SC} = \frac{V_B}{R_3} = \frac{K I_1}{(K+1)G_2 + G_1} G_3$$

* THE SC DOES NOT CHANGE EITHER EQ FROM PART (a) SINCE WE DID NOT DO A KCL ON THE DEPENDENT VOLTAGE SOURCE

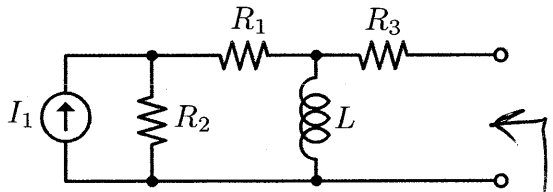
(c) (2 points) Draw the Thevnin Equivalent circuit and label the elements using V_{oc} and I_{sc}.



(d) (2 points) Draw the Norton Equivalent circuit and label the elements using V_{oc} and I_{sc}.

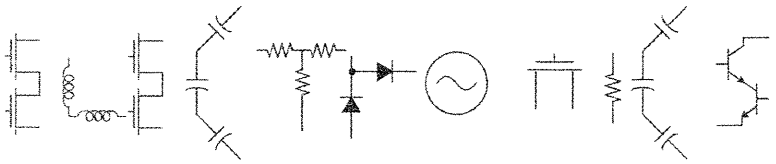


(e) (3 points) Suppose the circuit is modified as shown below. The dependent source is replaced with an inductor. Using Phasors, find the Norton equivalent impedance directly. You may express your answer using the series and parallel operators.



$$Z = R_3 + j\omega L \,||\, (R_1 + R_2) \leftarrow$$

$$= R_3 + \frac{j\omega L (R_1 + R_2)}{j\omega L + R_1 + R_2}$$



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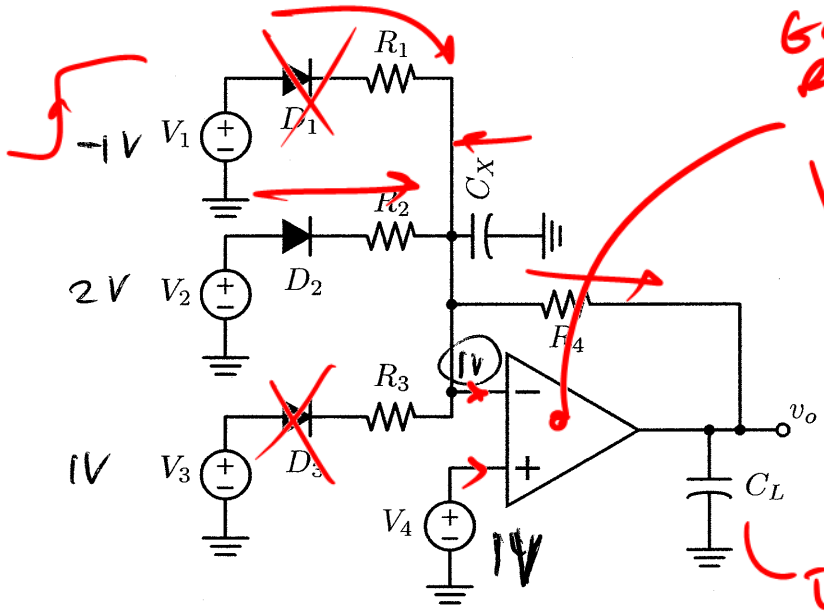
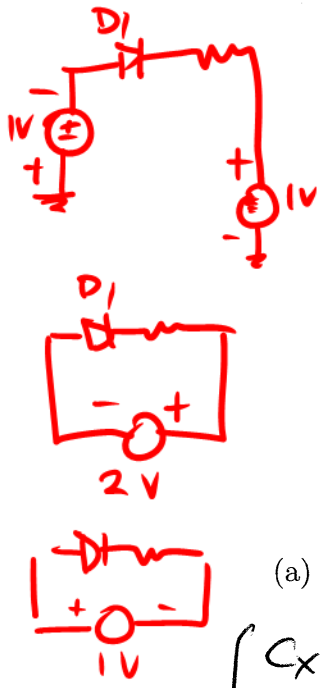
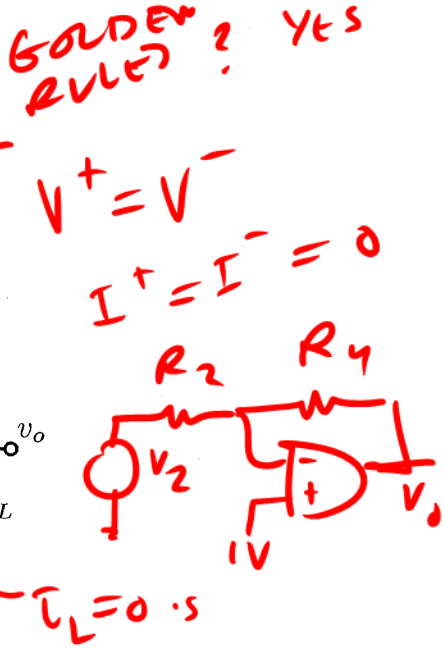
2. (15 points) Consider the following circuit with ideal diodes D1-D3 connected to DC voltage sources. The op-amp is ideal and drives a load capacitor $C_L = 1\mu$F. $R_1 = R_2 = R_3 = R_4 = 1\,\text{k}\Omega$. Suppose $V_1 = -1$V, $V_2 = 2$V, $V_3 = 1$V, and $V_4 = 1$V and that the capacitor C_X and C_L are initially discharged.







(a) (2 points) Which of the diodes are ON/OFF? Does the capacitor C_X play a role in the circuit? Why or why not?

[C_X PLAYS NO ROLE SINCE IT'S ON A VIRTUAL GROUND → BOTH END ARE AT A FIXED POTENTIAL]

D_2, D_3 ON D_1 OFF

(b) (5 points) Use superposition to calculate the V_o as a function of V_1, V_2, V_3, and V_4.

$$V_o = \frac{(V_2 - V_4)}{R_2}(-R_4) + \frac{(V_3 - V_4)}{R_3}(-R_4)$$

$$= 1\text{V} \cdot (-1) + 0 = -1\text{V}$$

(c) (4 points) Suppose that V_1 then it changes abruptly from -1V to 2V (step function). Draw V_o as a function of time. (*Hint:* What's the circuit time constant?)

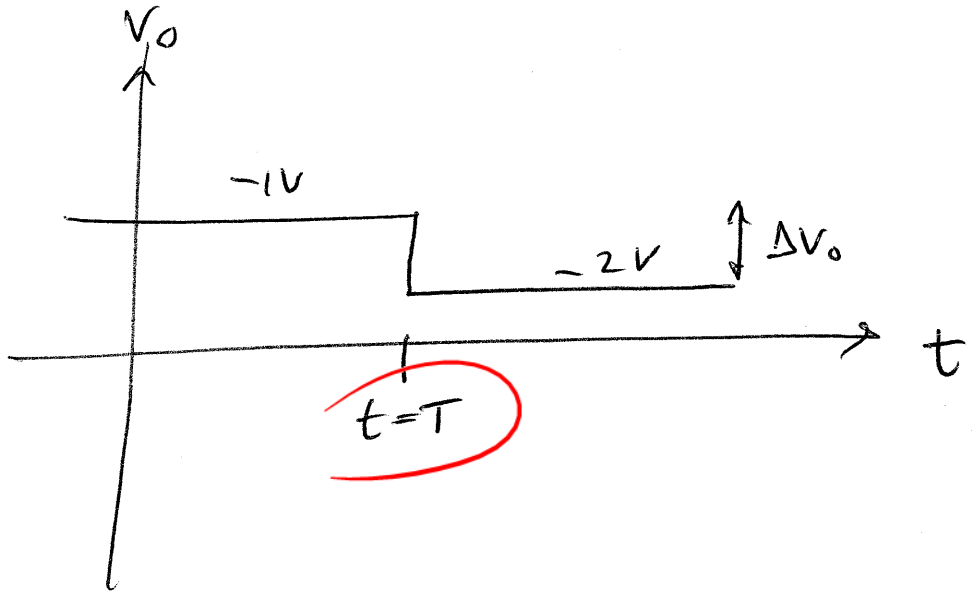
GAIN

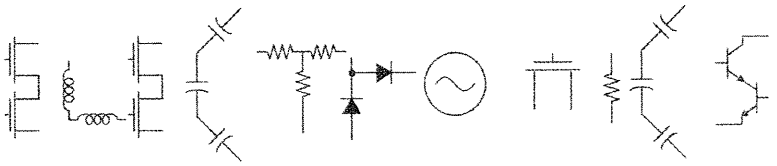
$$\Delta V_o = \frac{(V_1 - V_4)}{R_1}(-R_4) = -1V$$

C_1 CHARGES INSTANTLY DUE TO OP-AMP

VOLTAGE ACROSS

C_x DOES NOT CHANGE





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(d) (4 points) Suppose that the voltages are again $V_1 = -1\text{V}$, $V_2 = 2\text{V}$, $V_3 = 1\text{V}$, and $V_4 = 1\text{V}$ and then suppose that V_4 changes abruptly from 1V to 0V (step function). Draw V_o as a function of time. (*Hint:* What's the circuit time constant?)

D_1 STILL OFF BUT MORE CURRENT FLOWS IN THROUGH V_2 & V_3

$$V_o(t \to \infty) = -V_2 \frac{R_4}{R_2} - V_3 \frac{R_4}{R_2}$$

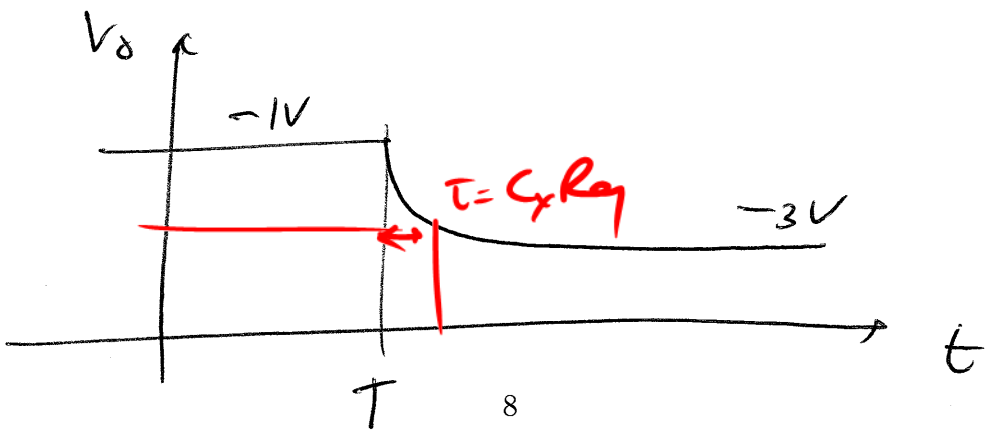
$$= -2 - 1 = -3\text{V}$$

C_x MUST DISCHARGE THROUGH RESISTANCES IN CIRCUIT.

$$R_{eq} = R_2 \| R_3 \| R_4 = \frac{1}{3}\ \text{k}\Omega$$

$$\tau = C_x R_{eq}$$

$R_{eq} = R_4 = 1\text{k}\Omega$



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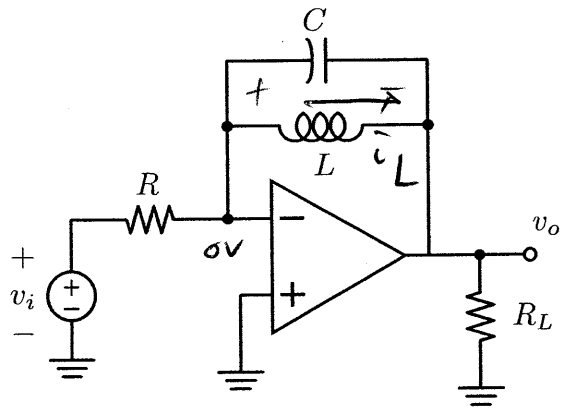
3. (15 points) The circuit shown below has a capacitor C which is initially discharged and an inductor with zero initial current.



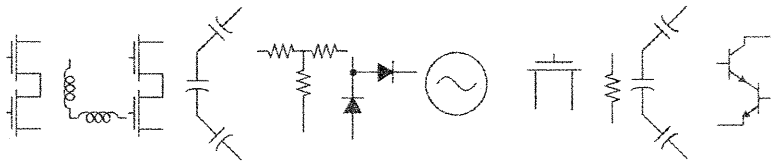
(a) (5 points) Write a differential equation describing the circuit behavior. Use i_L as the unknown quantity.

$$\frac{V_i}{R} = -C\frac{dV_o}{dt} + i_L$$

$$V_o = -L\frac{di_L}{dt}$$

$$\frac{V_i}{R} = LC\frac{d^2 i_L}{dt^2} + i_L$$

NOTE: DIRECTION OF i_L NOT SPECIFIED SO DOUBLE CHECK STUDENT'S ANSWER & DEF.



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(b) (2 points) What is the circuit Q factor?

$Q = \infty$

(c) (3 points) Express the output voltage v_o in terms of the inductor current i_L.

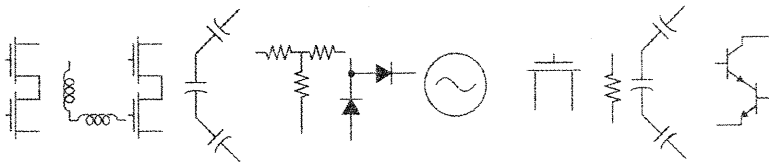
$$v_o = -L \frac{di_L}{dt}$$

(d) (2 points) If $L = 1\mu$H, specify C so that the undamped resonant frequency ω_0 is equal to 1000 rad/sec.

$$\sqrt{\frac{1}{LC}} = \omega_o = 10^3$$

$$\frac{1}{LC} = 10^6$$

$$C = \frac{1}{L\,10^6} = \frac{1}{10^{-6} \cdot 10^6} = 1\,\text{F}$$



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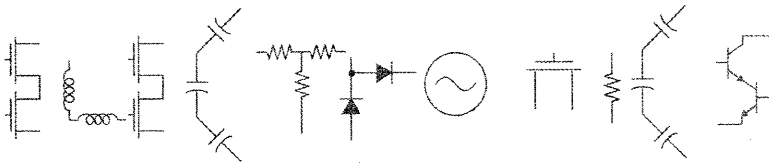
(e) (3 points) Derive V_o in terms of V_i directly for a sinusoidal steady-state source. Do this without using the original differential equations with phasor analysis.

$$\frac{V_i}{R} = -V_o\, j\omega C + \frac{V_o}{j\omega L}$$

$$= V_o\left(\frac{1}{j\omega L} - j\omega C\right)$$

$$\frac{V_o}{V_i} = \frac{1}{R\left(\frac{1}{j\omega L} - j\omega C\right)}$$

$$= \frac{j\omega L}{R(1+\omega^2 LC)}$$



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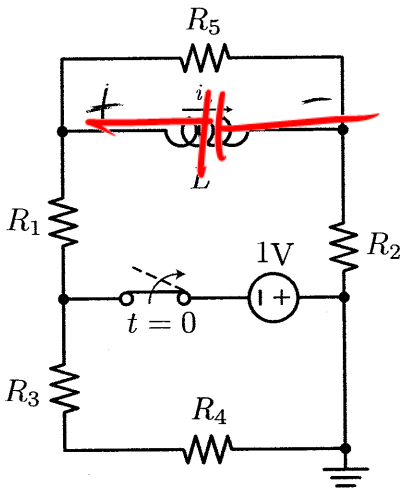
4. (15 points) In the following circuit, the switch has been closed for a long time. It opens at time $t = 0$s.



(a) (5 points) At time $t = 0^-$s, right before the switch opens, what's the inductor current i_L?

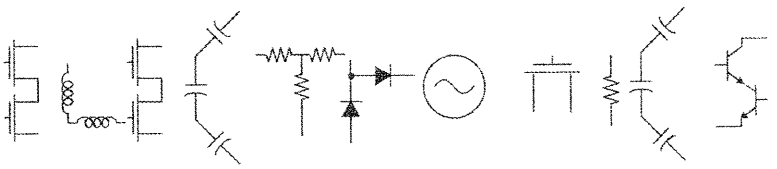
$$i_L(t=0^-) = \frac{-1V}{R_1+R_2}$$

(b) (5 points) Derive the equivalent Thevenin circuit for time $t \geq 0$s as seen by the inductor. In other words, what's the equivalent circuit seen by the inductor?

$$V_{th} = V_{oc} = \frac{R_5}{R_1+R_2+R_5}(-1V)$$

$$R_{th} = R_5 \,||\, (R_1+R_2)$$

CHECK STUDENT'S SIGN CONVENTION



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(c) (2 points) What is the circuit time constant (by inspection of the equivalent circuit)?

$$\tau = L/R_{th}$$

(d) (3 points) Find the complete solution $i_L(t)$ for $t \geq 0$.

$$i_L(0) = \frac{-1V}{R_1 + R_2}$$

$$i_L(\infty) = 0$$

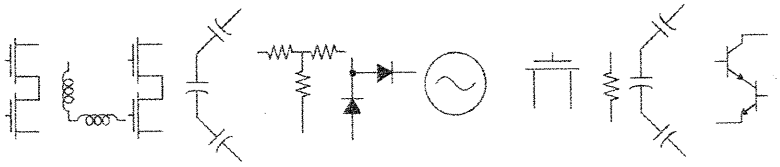
$$i_L(t) = A + Be^{-t/\tau}$$

$$i_L(0) = A + B = \frac{-1V}{R_1 + R_2}$$

$$i_L(\infty) = A = 0$$

$$B = \frac{-1V}{R_1 + R_2}$$

$$i_L(t) = \frac{-1V}{R_1 + R_2} e^{-t/\tau}$$



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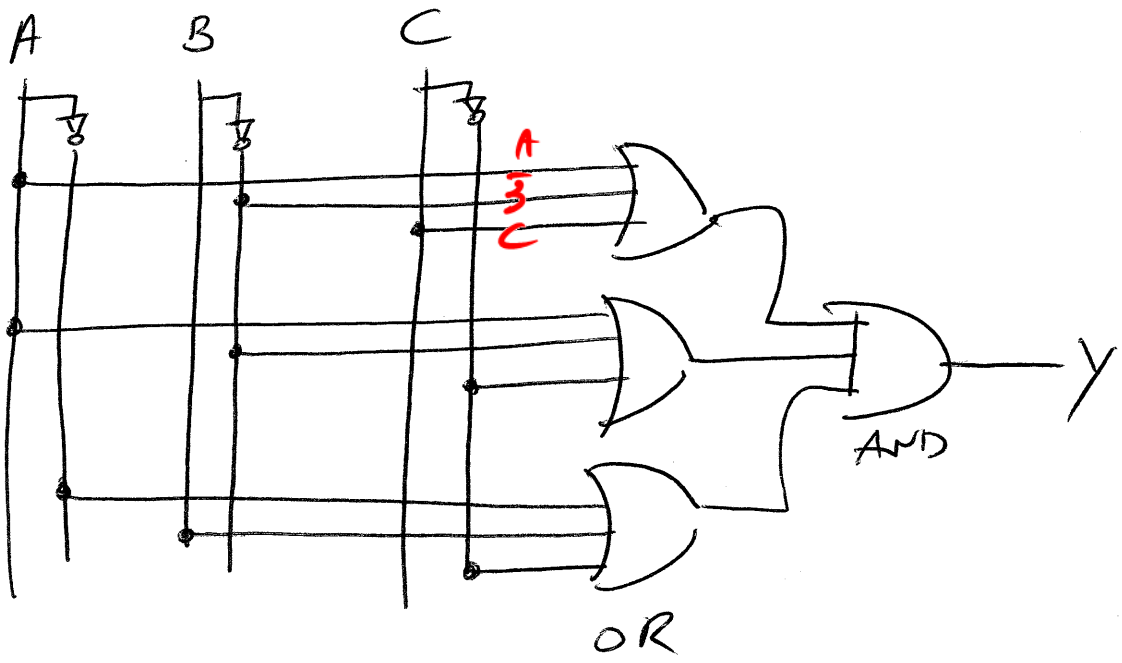
5. (15 points) Consider the following truth table for a three-input function, with inputs A, B, and C and one output Y.

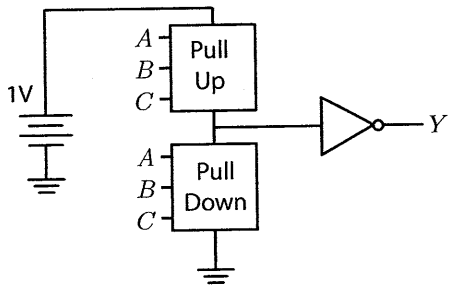
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0 ←
0	1	1	0 ←
1	0	0	1
1	0	1	0 ←
1	1	0	1
1	1	1	1

(a) (4 points) Write a Boolean epxpression for Y in maxterm form. In other words, write Y as a product of sums.

$$Y = (A + \bar{B} + C) \cdot (A + \bar{B} + \bar{C}) \cdot (\bar{A} + B + \bar{C})$$

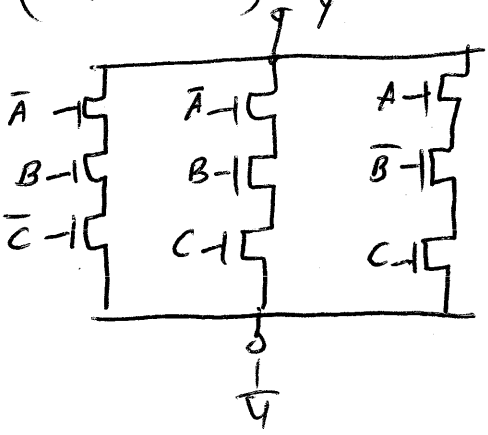
(b) (3 points) Implement the logic expression using AND, OR and NOT.



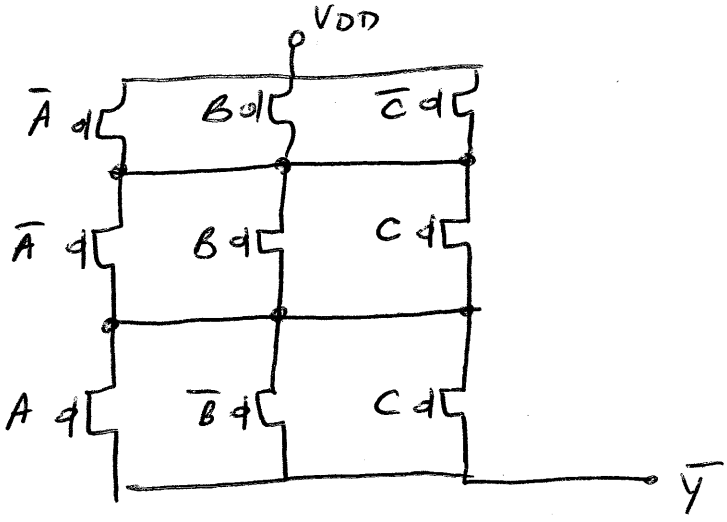


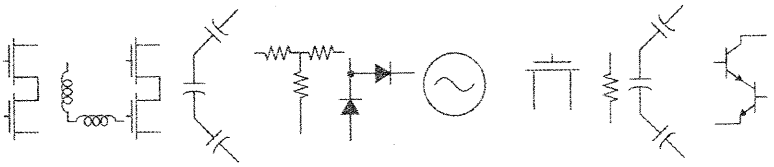
(c) (4 points) Now realize this function using CMOS logic transistors directly as shown above. Draw only the pull down network for $\overline{Y}$.

$$\overline{Y} = \overline{(A+\overline{B}+C)} + \overline{(A+\overline{B}+\overline{C})} + \overline{(\overline{A}+B+\overline{C})}$$
$$= \overline{A}B\overline{C} + \overline{A}BC + A\overline{B}C$$



(d) (4 points) Draw the pull up network for $\overline{Y}$.





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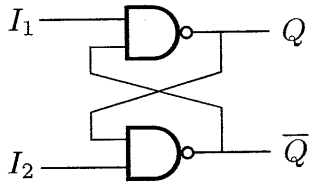
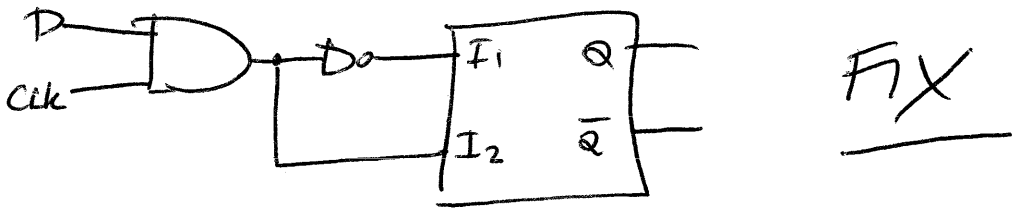
6. (10 points) The following sequential circuit has two inputs I_1 and I_2 and two outputs Q and $\overline{Q}$.



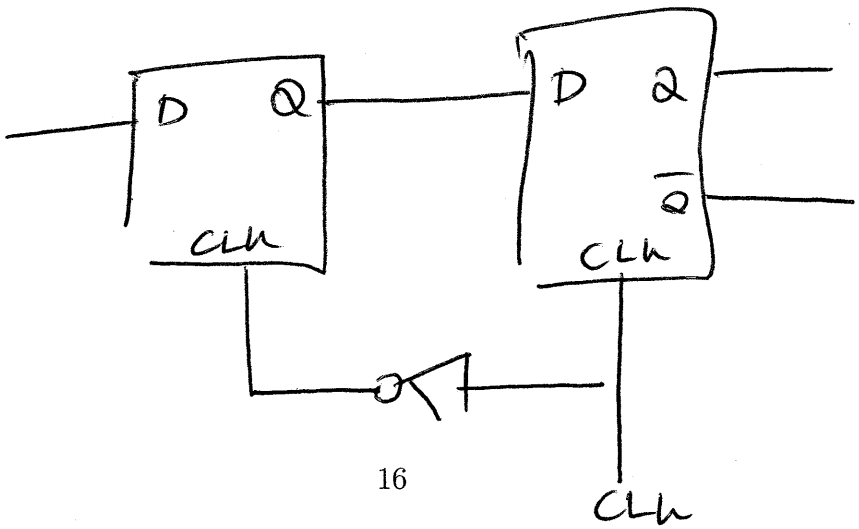
(a) (3 points) Complete the truth table where Q_n is the current output and Q_{n-1} is the previous output.

I_1	I_2	Q_n	$\overline{Q}_n$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	Q_{n-1}	$\overline{Q}_{n-1}$

(b) (3 points) Design a D latch using this building block with a clock enable input.



(c) (4 points) Design a positive edge triggered flip-flop using the D latch as a building block.



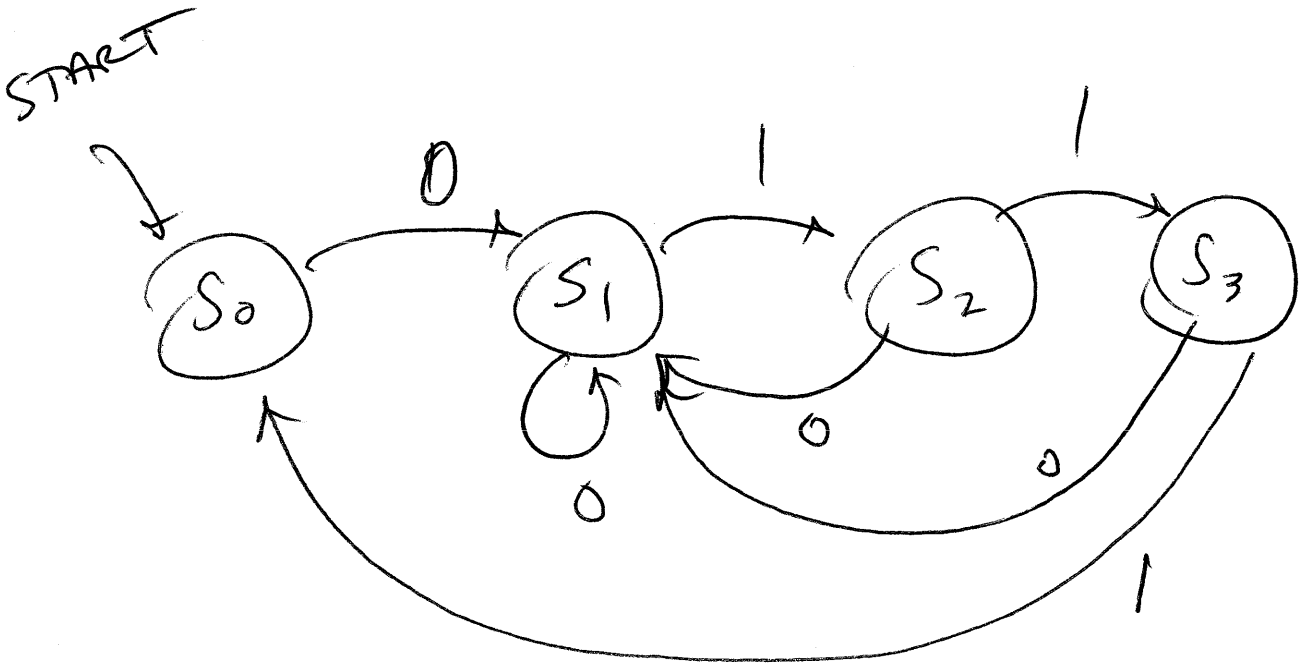
7. (5 points) Draw the state transition diagram for an FSM that detects the patter 011.

S_0 : NO PATTERN

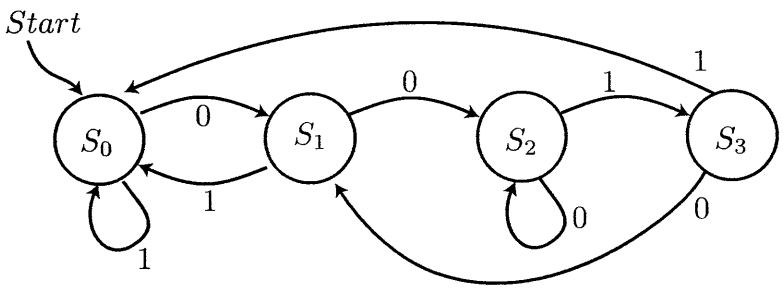
S_1 : 0

S_2 : 01

S_3 : 011



8. (10 points) Consider the following state diagram. There is only one binary input.



(a) (2 points) What pattern does it detect?

0 0 1

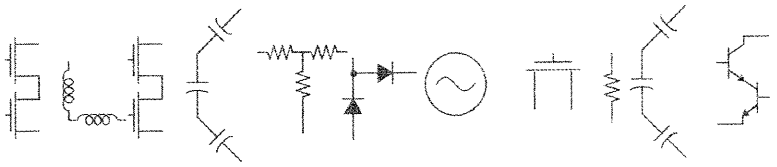
(b) (2 points) For the pattern "0111100010" write the sequence of states for the system.

S_1 S_0 S_0 S_0 S_0 S_1 S_2 S_2 S_3 S_1

↑ DETECT!

(c) (2 points) Draw the state transition table.

S_1	S_0	I	S_1'	S_0'
0	0	0	0	1
0	0	1	0	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	0
1	0	1	1	1
1	1	0	0	1
1	1	1	0	0



SID:

(d) (2 points) Implement the state transition logic.

$$S_0' = \bar{S}_1 \bar{S}_0 \bar{I} + S_1 \bar{S}_0 I + S_1 S_0 \bar{I}$$

$$S_1' = \bar{S}_1 S_0 \bar{I} + S_1 \bar{S}_0 \bar{I} + S_1 \bar{S}_0 I$$

(e) (2 points) Draw a complete FSM using registers and the logic at the block diagram level.