

# **EECS 242: Linearization Efficiency Enhancement and Power Combiners**

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**University of California, Berkeley**

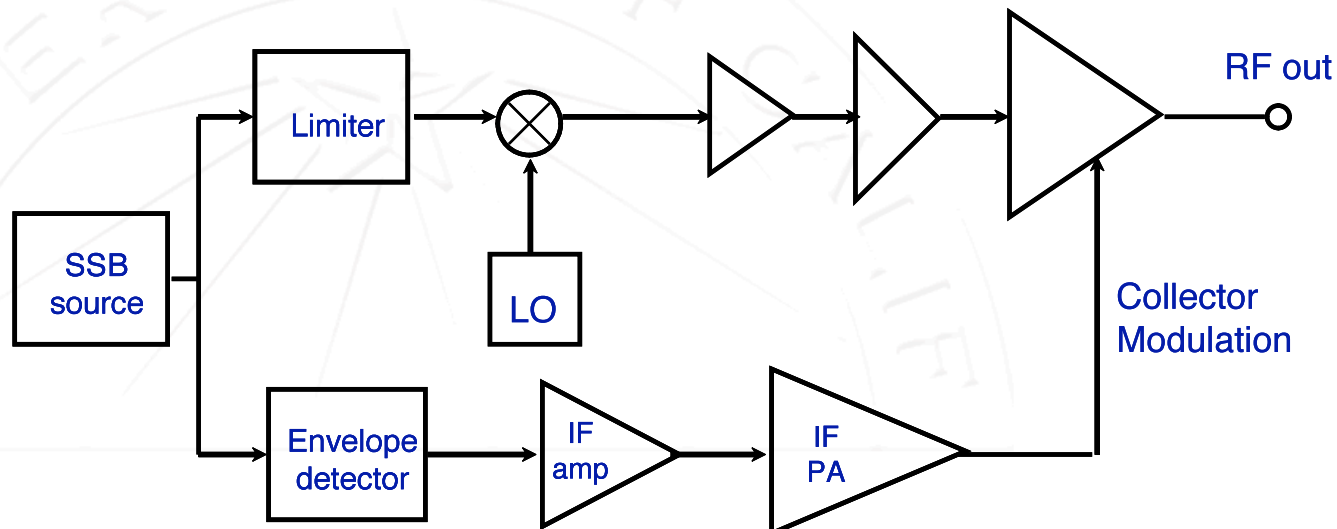




# Linearization

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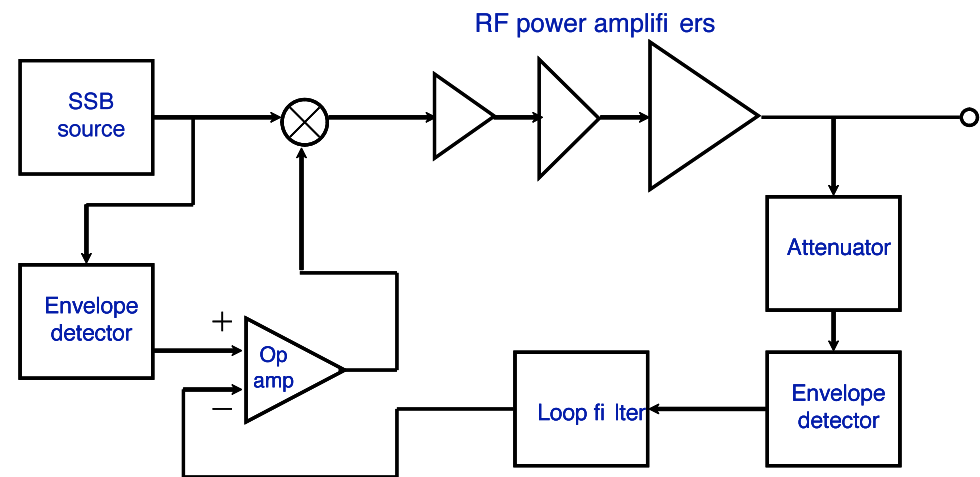
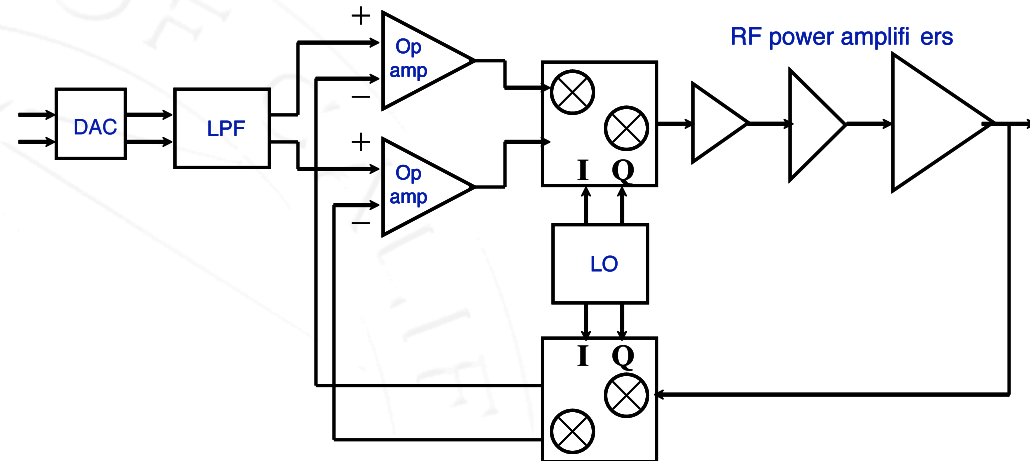
# Polar Modulators



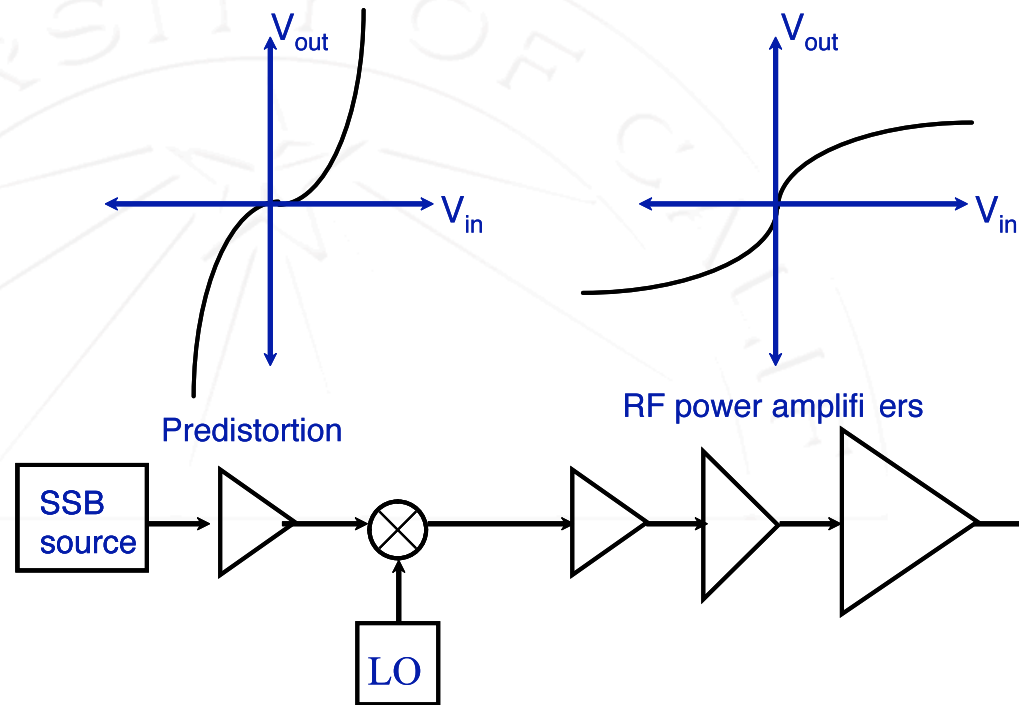
- Polar modulators are gaining popularity by require complex feedback and/or chip to external PA interaction
- Modulation bandwidth is a limiting factor
- In a digital system, the magnitude/phase signal are generated directly and fed into an offset PLL and PA supply voltage

# Feedback Loops with PA

- Need loop gain, stability a big concern, modulation bandwidth
- Envelope feedback only works for AM-AM non-linearity
- Cartesian requires linear mixers and good amplitude/phase matching
- Complexity...

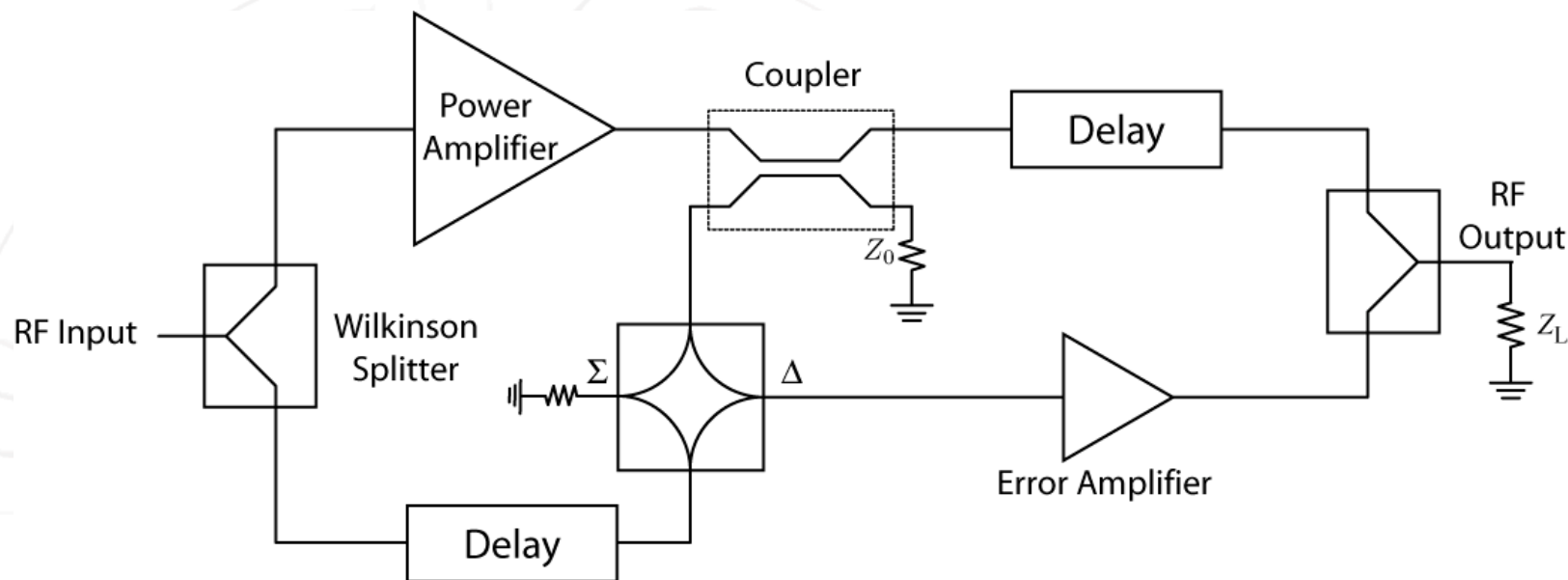


# Digital Predistortion



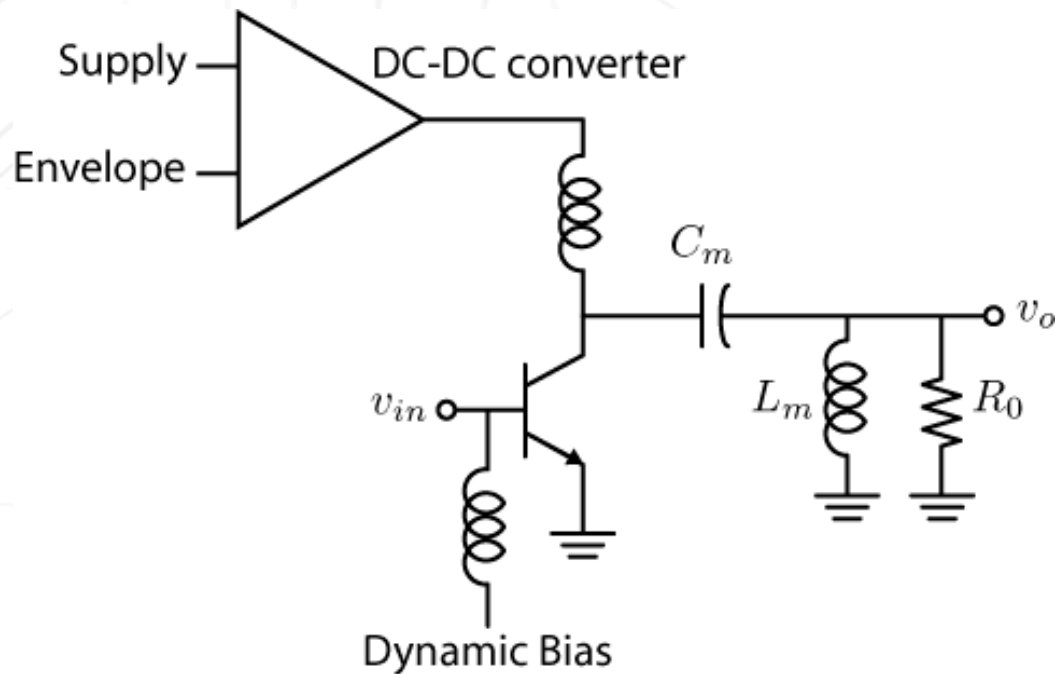
- In a modern system a dynamic predistortion circuit can compensate for process/temp variations
- Can implement predistortion at baseband
- 100k gates = 1 pad

# Microwave Feedforward



- Basestations use feedforward linearization since calibration is a possibility.
- Use couplers

# Dynamic PA



- Envelope tracking supply and dynamic class-A
- Efficiency always close to peak efficiency of amplifier (say 30%) regardless of PAR
- Need a very fast DC-DC converter



# Power Combining

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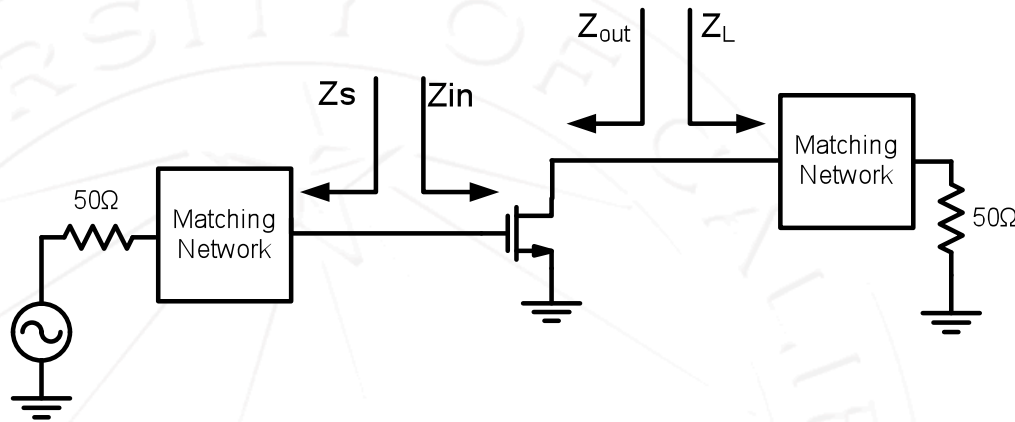


# How Big?

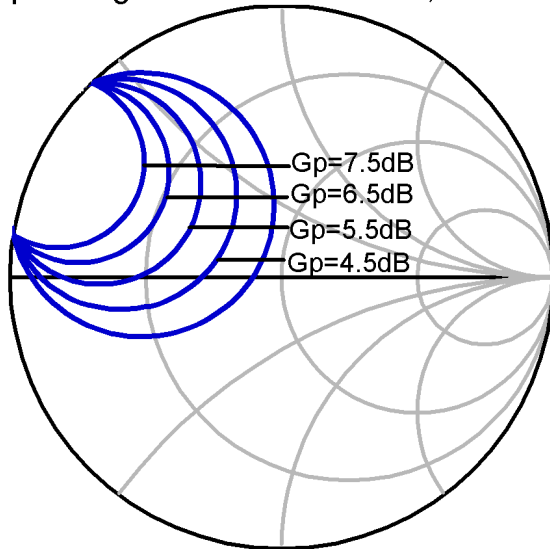
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- The amount of power that we can extract from a PA device is limited by the output impedance of the device. As the device is made larger to handle a higher DC current (without compromising the  $f_T$ ), the lower the output impedance.
- For a “current source” style of PA, eventually the device is so large that power is lost in the device rather than the load. This is the attraction of a switching PA.

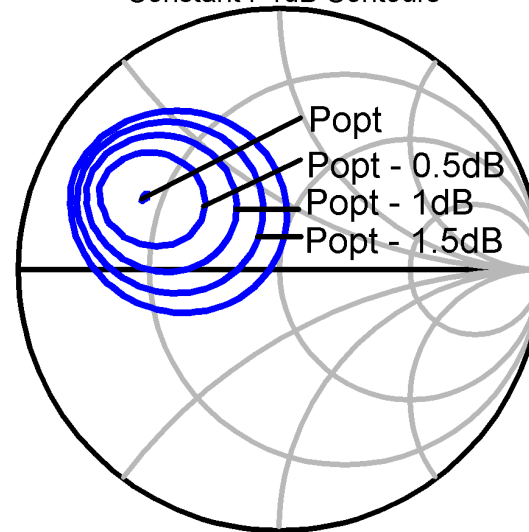
# Gain vs. Output Power Tradeoff



Operating Power Gain Circles,  $F=60\text{GHz}$



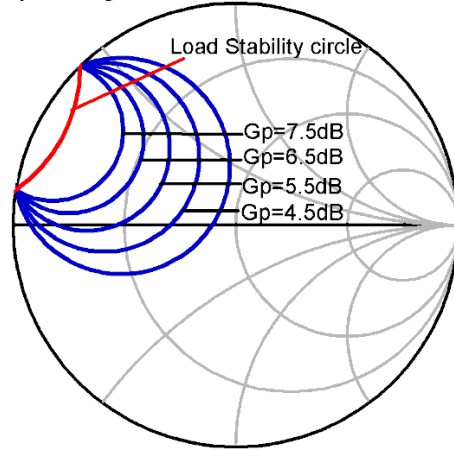
Constant  $P_{1\text{dB}}$  Contours



# Power Devices (cont)

100 fingers  
1  $\mu\text{m}$ /finger

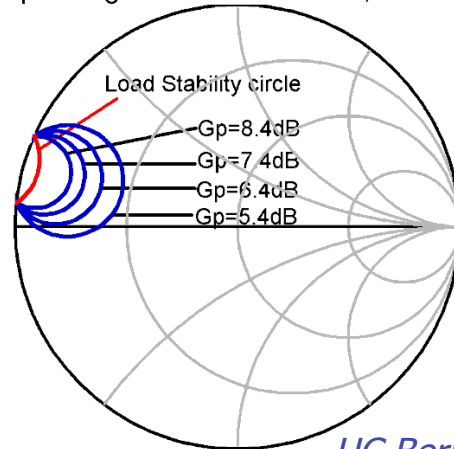
Operating Power Gain Circles,  $F=60\text{GHz}$



Finger width	MSG	Idc
1 $\mu\text{m}$	7.6dB	25mA
2 $\mu\text{m}$	8.4dB	47mA
4 $\mu\text{m}$	6.8dB	94mA

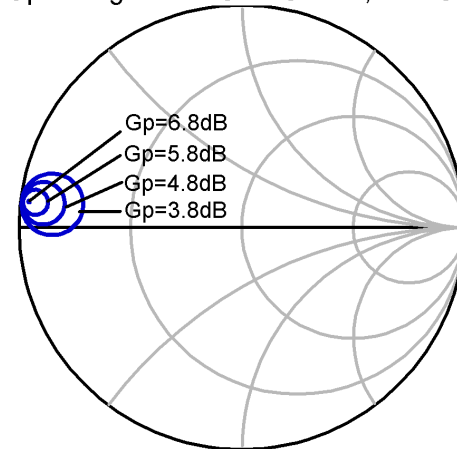
100 fingers  
2  $\mu\text{m}$ /finger

Operating Power Gain Circles,  $F=60\text{GHz}$

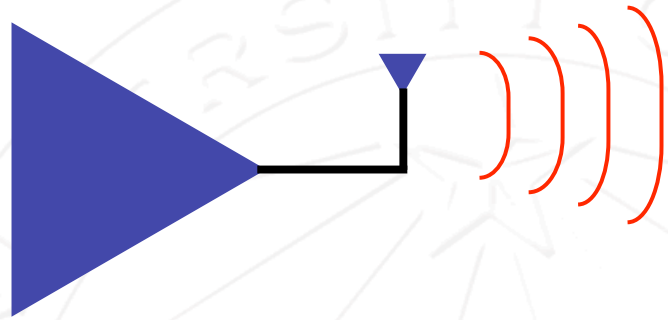


100 fingers  
4  $\mu\text{m}$ /finger

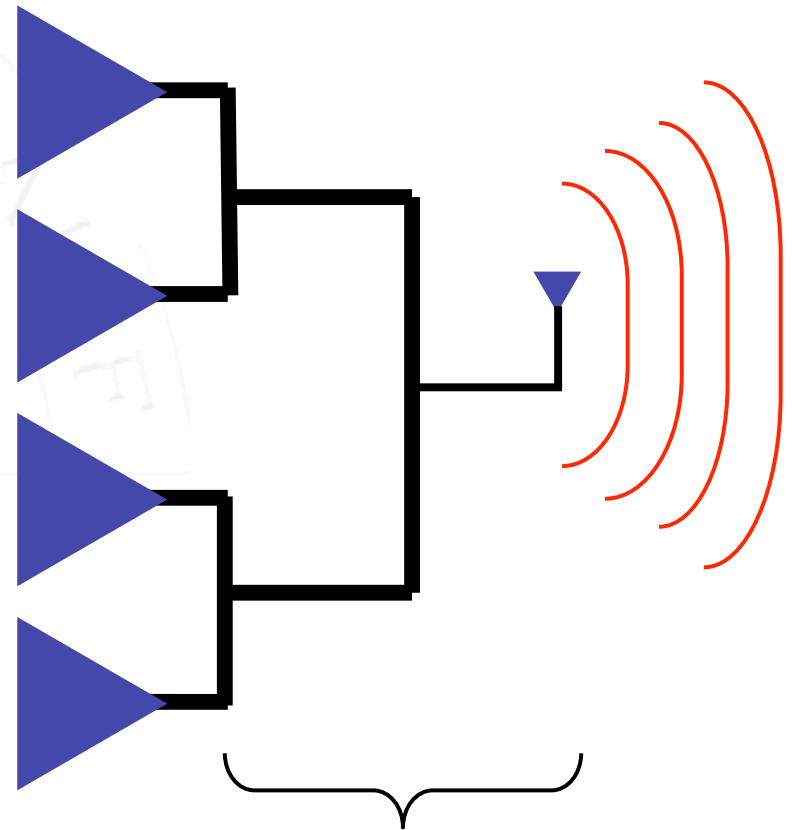
Operating Power Gain Circles,  $F=60\text{GHz}$



# Power Combining (cont)



- But for a non-switching PA we must perform some power combining to use more than one device. This way we can transform the load into a higher impedance seen by each PA.
- The power combining networks are lossy and large. We'll come back to them later.



**Lossy Power Combiner**

# Can we “wire” PAs together?

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- Note that we cannot simply “wire” PAs together since the impedance seen by each PA increases by  $N$  if we connect  $N$  in parallel:

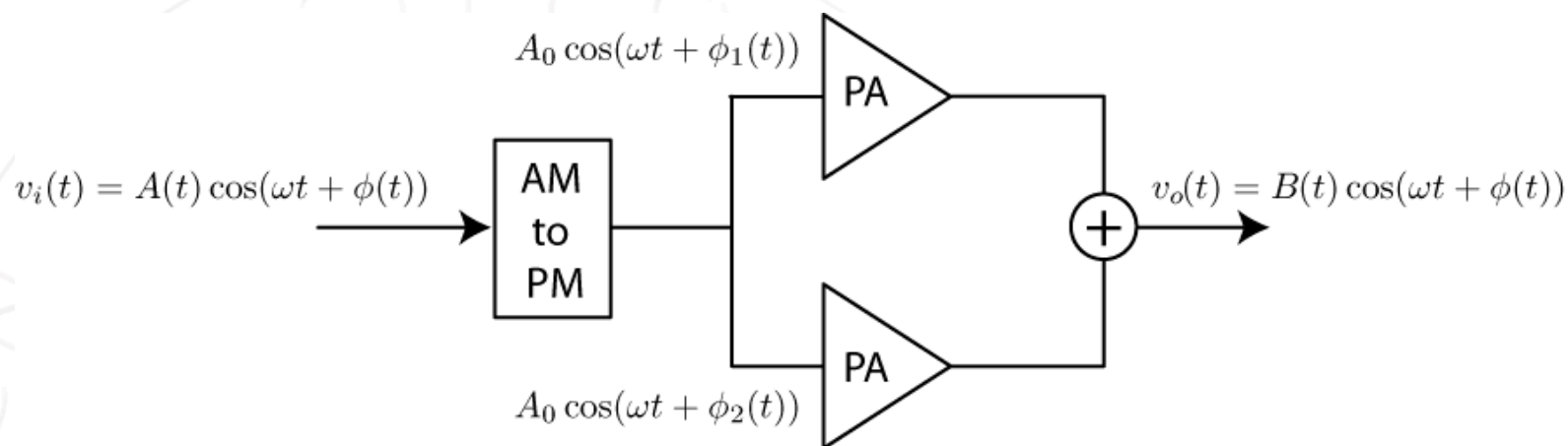
$$R_{PA} = \frac{V_L}{I_L/N} = NR_L$$

- This means that each PA delivers less power for a fixed swing

$$P_{PA} = \frac{V_{swing}^2}{2R_{PA}}$$

- There is also “load pulling” effects if the sub-PAs are not perfectly in phase

# Outphasing LINC Amplifier



- Decompose the AM/PM signal into two PM signals
- The two PM signals can get amplified by two non-linear PA's. These can be saturated and efficient amplifiers.
- By combining the two signals, the amplitude modulation is restored at the antenna.
- How to combine signals? Simple current mode will present a time-varying load to each PA. Coupler or isolator will waste power.

# Outphasing Math

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$$\cos(A) + \cos(B) = 2 \cos\left(\frac{A+B}{2}\right) \cos\left(\frac{A-B}{2}\right)$$

$$\cos(\omega t + \phi) + \cos(\omega t - \phi) = 2 \cos(\phi) \cos(\omega t)$$

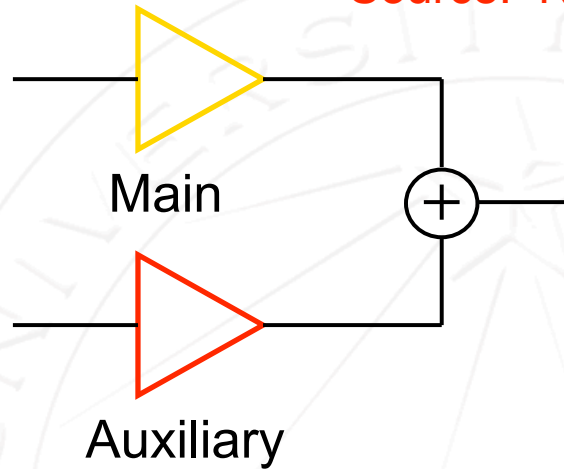
$$\cos(\omega t + \cos^{-1} A(t)) + \cos(\omega t - \cos^{-1} A(t)) = 2 \cos(\cos^{-1} A(t)) \cos(\omega t)$$

$$\cos(\omega t + \cos^{-1} A(t)) + \cos(\omega t - \cos^{-1} A(t)) = 2 A(t) \cos(\omega t)$$

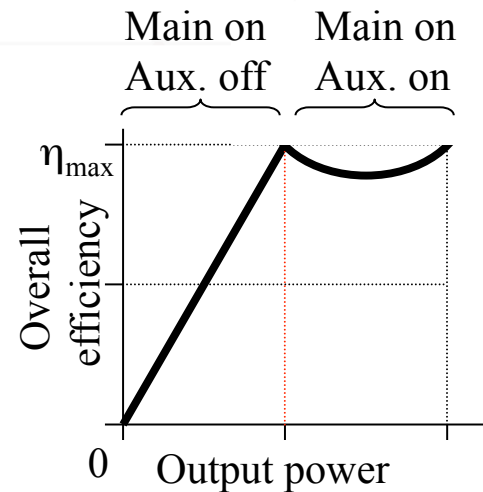
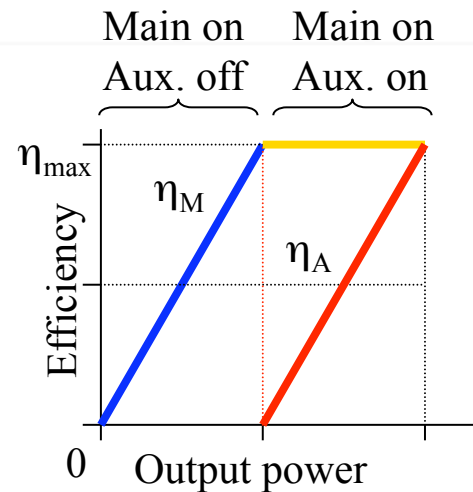
- In theory all we need to do is to compute the inverse cosine of the AM waveform to generate our outphasing signals
- In practice, we can use a DSP to calculate these signals since the envelope rate is at the modulation rate and digital techniques work well
- Power combining is the main difficulty.

# Doherty Amplifier Concept

Source: Naratip Wongkomet and P. Gray (UCB)



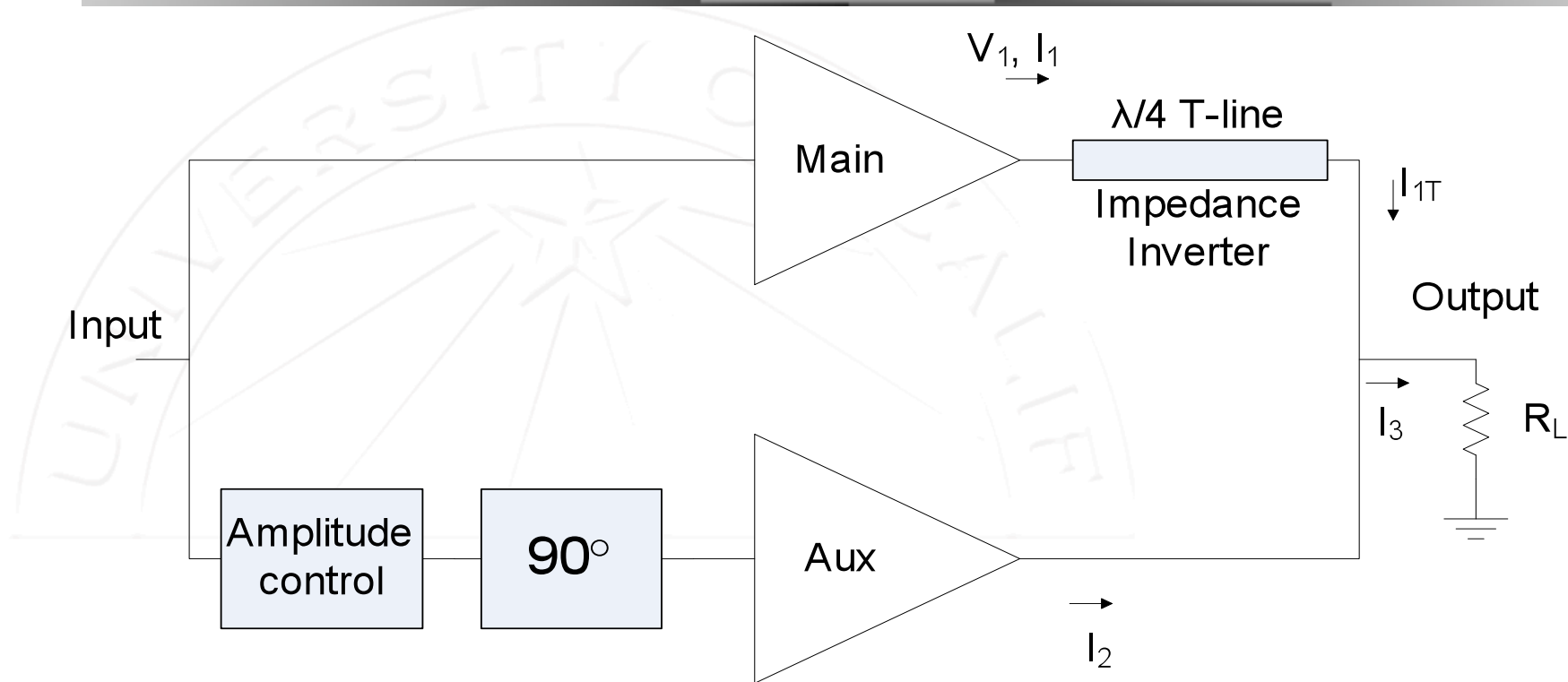
- Invented by W.H. Doherty in 1936
- Good power efficiency over a wide range of output power



Must efficiently combine power without increasing  $V_{\text{swing}}$

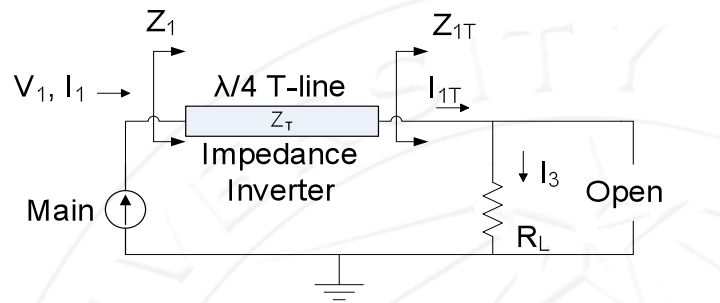


# Doherty Amplifier Block Diagram



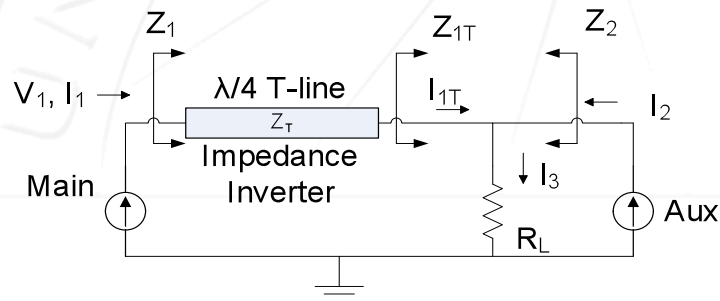
Quarter wave line used as an impedance inverter. Can be realized with LC equivalent.

# Doherty Details



(a)

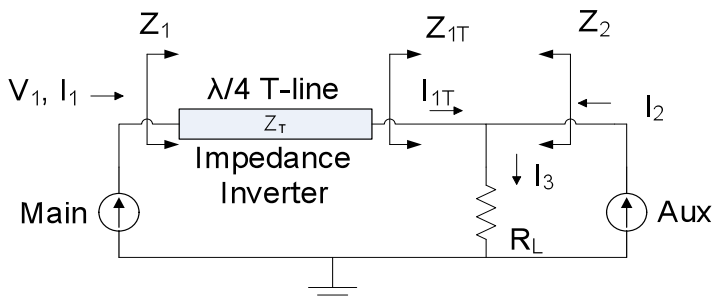
$$Z_1 = \frac{Z_T^2}{R_L}$$



(b)

$$Z_1 = \frac{Z_T^2}{R_L \left(1 + \frac{I_2}{I_{1T}}\right)}$$

$$Z_2 = R_L \left(1 + \frac{I_{1T}}{I_2}\right)$$



(c)

$$I_{1T} = I_2$$

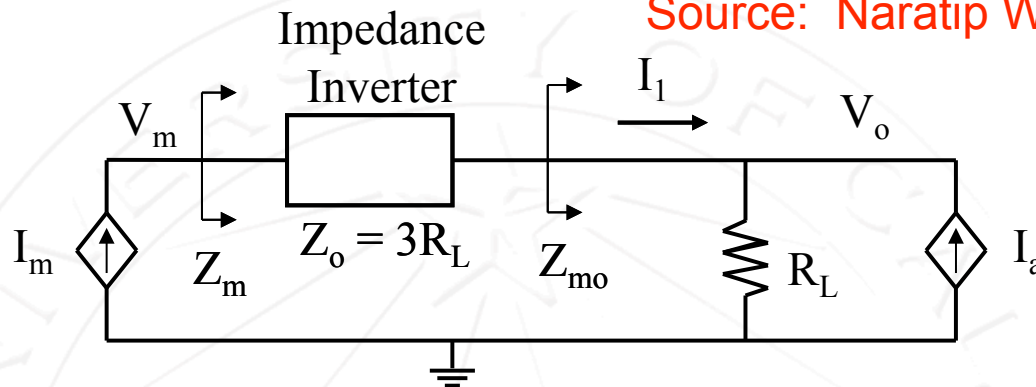
$$Z_1 = \frac{Z_T^2}{2R_L}$$

$$Z_2 = 2R_L$$

- Small signal region: auxiliary amplifier is off
- When the input crosses the threshold, the action of the auxiliary amplifier is to dynamically lower the load seen by the main PA
- Finally, both amplifiers operate at the peak power point

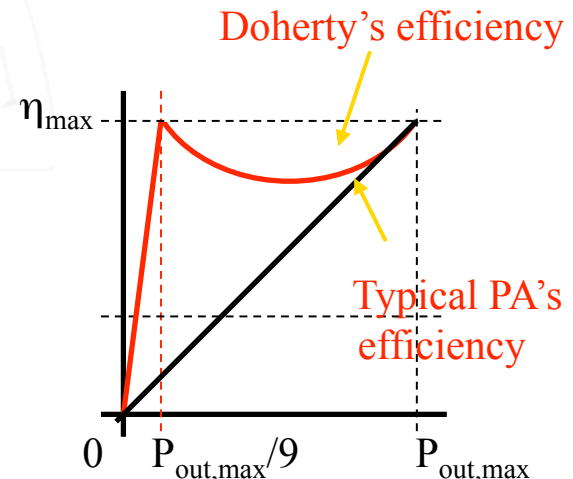
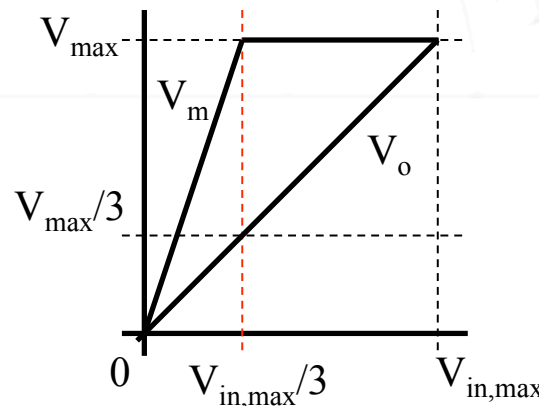
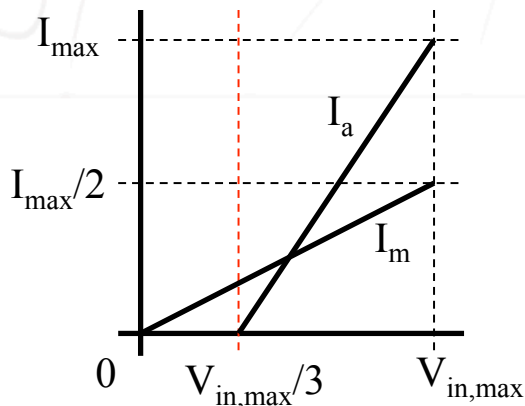
# Doherty Amplifier Operation

Source: Naratip Wongkomet and P. Gray (UCB)



$$Z_m = Z_o^2 / Z_{mo}$$

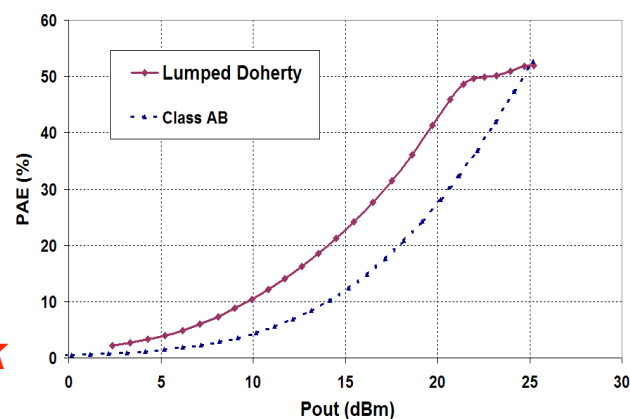
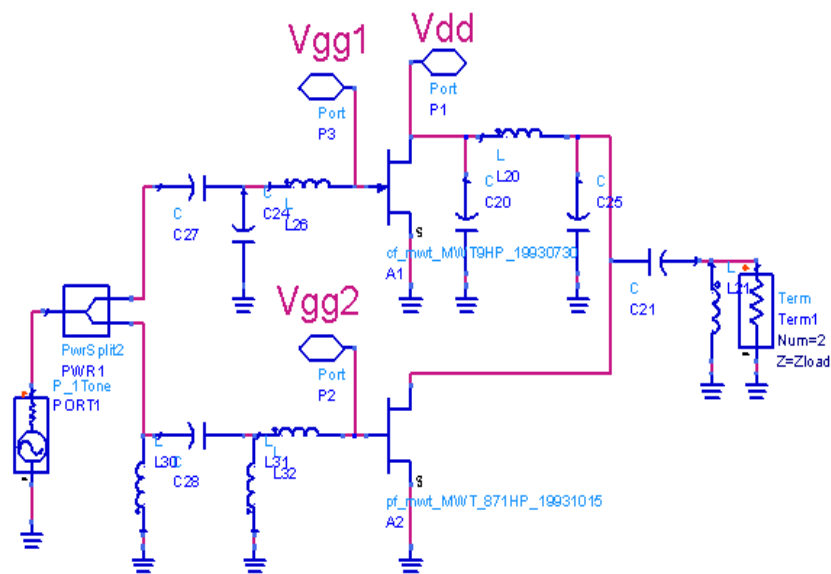
$$Z_{mo} = R_L (1 + I_a / I_1)$$



Auxiliary amplifier actively changes load impedance of the main amplifier

# Lumped Doherty Implementation

- Can use lumped elements to realize  $90^\circ$  phase shift
- The CLC line is an impedance inverter that also provides VDD for the aux amp
- The LCL line is embedded into the matching network and provides  $90^\circ$  phase shift
- Simulations show an improved efficiency



**Zhao, M. Iwamoto, D. Kimball, L. Larson, P. Asbeck**

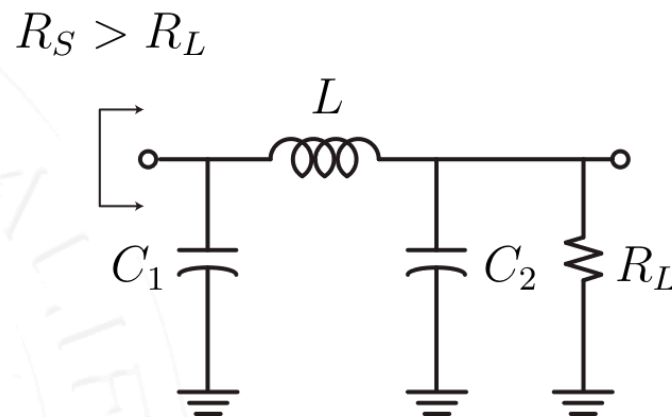
**University of California, San Diego**

UC Berkeley, EECS 242

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# LC Matching Networks

- Matching networks are needed to drive output power to the load, which has a fixed impedance.
- Large output powers require a large transformation ratio, and low voltage operation means high currents in the CMOS stage (sensitive to series resistance).
- 30 dBm of output power requires a matching ratio of 100 !



$$P_L = m \frac{V_{SW}^2}{2R_L} < m \frac{V_{DD}^2}{2R_L}$$

$$P_L < m \cdot \frac{1V^2}{2 \cdot 50\Omega} = m \times 10\text{mW}$$

# LC Matching Network Loss

- The power loss of integrated matching networks is important.
- The insertion loss can be derived by making some simple approximations
- The final result implies that we should minimize our circuit  $Q$  factor and maximize the component  $Q_c$

$$P_{in} = P_L + P_{diss}$$

$$IL = \frac{P_L}{P_{in}} = \frac{P_L}{P_L + P_{diss}} = \frac{1}{1 + \frac{P_{diss}}{P_L}}$$

$$W_m = \frac{1}{4}Li_s^2 = \frac{1}{44R_S^2}v_s^2L$$

$$\omega_0 \times W_m = \frac{1}{44R_S} \frac{v_s^2}{R_S} \omega_0 L = \frac{1}{28R_S} v_s^2 Q = \frac{1}{2} P_L \times Q$$

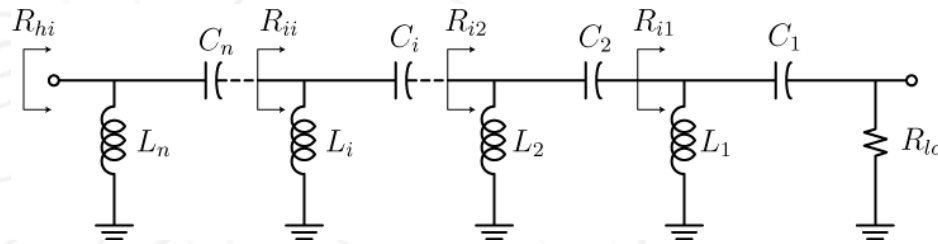
$$P_L = \frac{v_L^2}{2R_S} = \frac{v_s^2}{4 \cdot 2 \cdot R_S} = \frac{v_s^2}{8R_S}$$

$$\omega_0(W_m + W_e) = Q \times P_L$$

$$P_{diss} = \frac{P_L \cdot Q}{Q_c}$$

$$IL = \frac{1}{1 + \frac{Q}{Q_c}}$$

# Multistage Matching



$$Q = \frac{\omega(W_{s1} + W_{s2})}{P_{d1} + P_{d2}} = \frac{\omega W_{s1}}{2P_d} + \frac{\omega W_{s2}}{2P_d} = \frac{Q_1 + Q_2}{2}$$

$$R_{i,opt} = \sqrt{R_L R_S}$$

$$Q = \frac{1}{2} \left( \sqrt{\frac{R_i}{R_L}} - 1 + \sqrt{\frac{R_S}{R_i}} - 1 \right)$$

$$Q_{opt} = \sqrt{\sqrt{\frac{R_S}{R_L}} - 1} \approx m^{1/4}$$

$$\frac{R_{i1}}{R_{lo}} = \frac{R_{i2}}{R_{i1}} = \frac{R_{i3}}{R_{i2}} = \dots = \frac{R_{hi}}{R_{in}} = 1 + Q^2$$

$$\frac{R_{i1}}{R_{lo}} \cdot \frac{R_{i2}}{R_{i1}} \cdot \frac{R_{i3}}{R_{i2}} \dots \frac{R_{hi}}{R_{in}} = \frac{R_{hi}}{R_{lo}} = (1 + Q^2)^N$$

$$Q = \sqrt{\left(\frac{R_{hi}}{R_{lo}}\right)^{1/N} - 1}$$

- Since the  $Q$  of each stage is lowered, the insertion can improve

# Approximate Insertion Loss

$$P_{diss} = \frac{NQ P_L}{Q_u}$$

$$IL = \frac{1}{1 + N \frac{Q}{Q_u}}$$

$$IL = \frac{1}{1 + \frac{N}{Q_u} \sqrt{\left(\frac{R_{hi}}{R_{lo}}\right)^{1/N} - 1}}$$

$N$	$Q$ (Eq. 7.125)	$IL$ (dB) (Eq. 7.128)
1	9.95	-1.24
2	3	-0.79
3	1.91	-0.76
4	1.47	-0.78
5	1.23	-0.81
6	1.07	-0.85

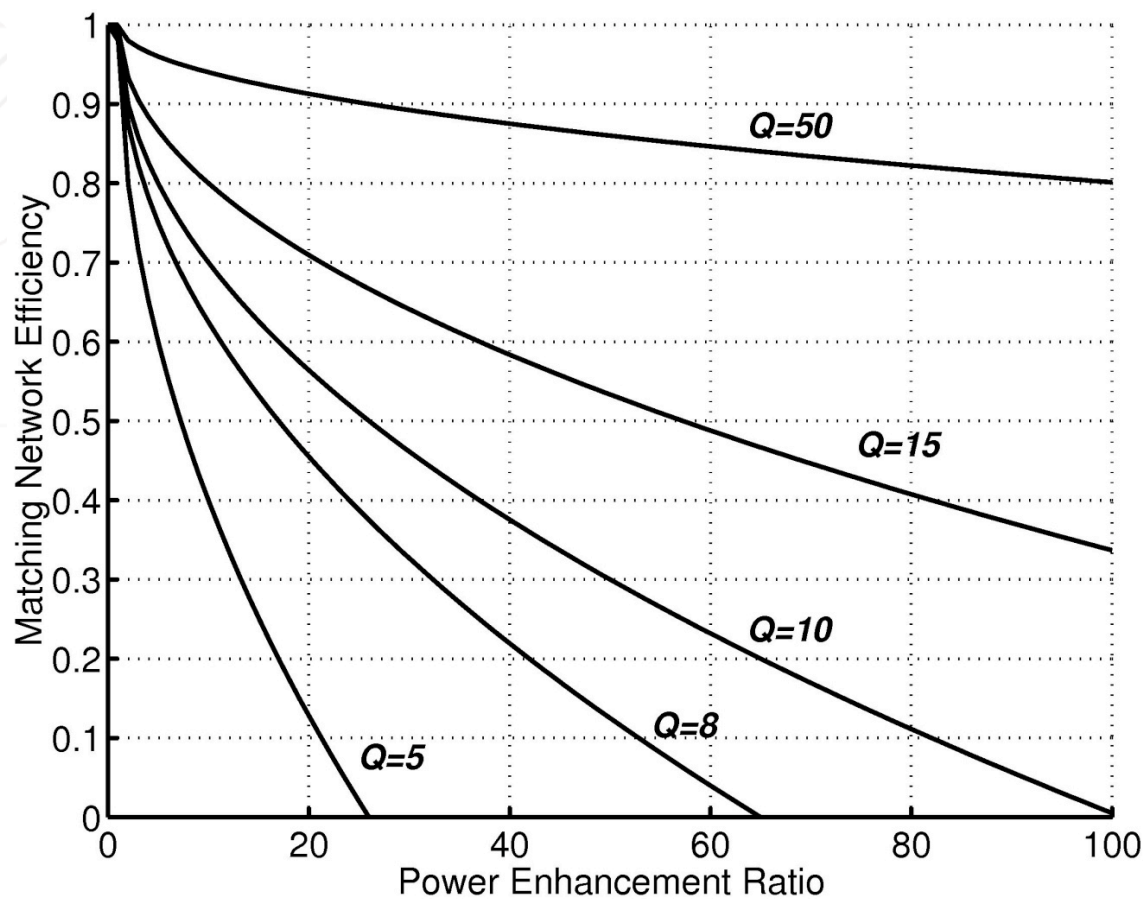
- Suppose a power amplifier delivering 100 W of power has an optimal load resistance of .5, but needs to drive a 50 IΩ antenna.
- Design a matching network assuming that the component Q's of 30 are available.
- First note that a matching factor of  $m = 50/.5 = 100$  is needed.
- Table above shows that 3 stages is optimum



# Technology Scaling

- Power Enhancement Ratio

$$PER = r \cdot \eta$$



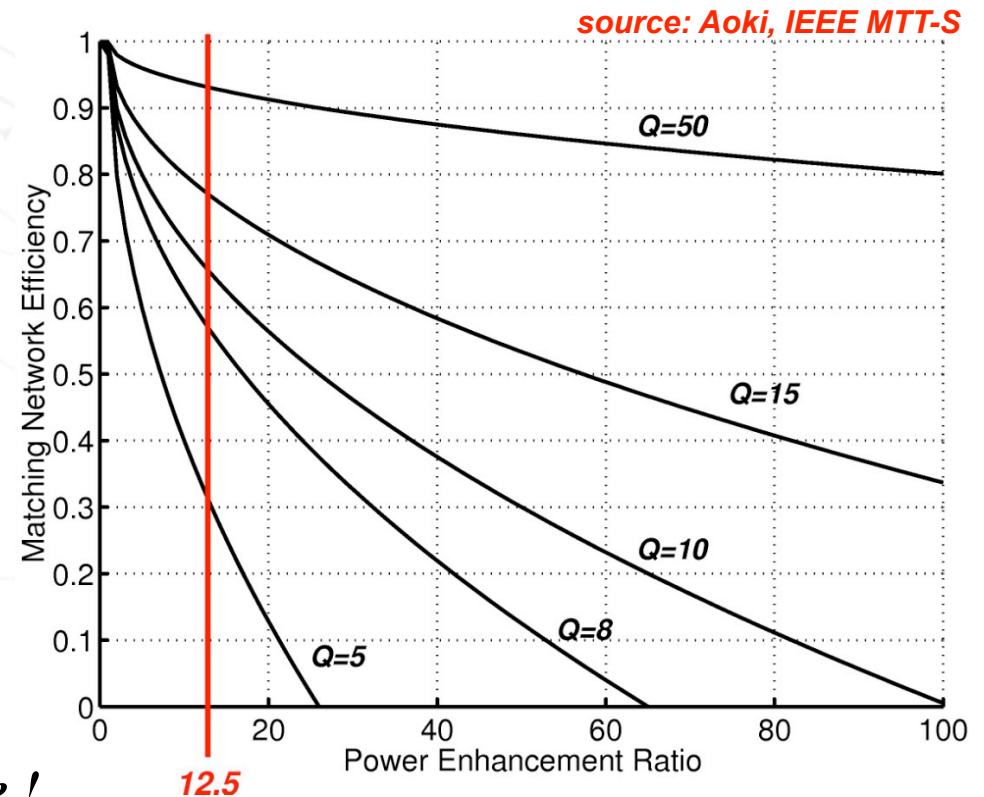
source: Aoki, IEEE MTT-S

# Technology Scaling

## ■ Example Class E

- $0.13 \text{ } \mu\text{m} \rightarrow V_{\text{PEAK}} = 3 \text{ V}$
- $P_{\text{OUT},50} = 8 \text{ mW}$
- Required  $P_{\text{OUT}} = 100 \text{ mW}$
- $R_{\text{IN}} = 4 \text{ } \Omega$
- $\text{PER} = 50/4 = 12.5$
- Q of 5  $\rightarrow \eta = 32\%$
- Q of 10  $\rightarrow \eta = 65\%$

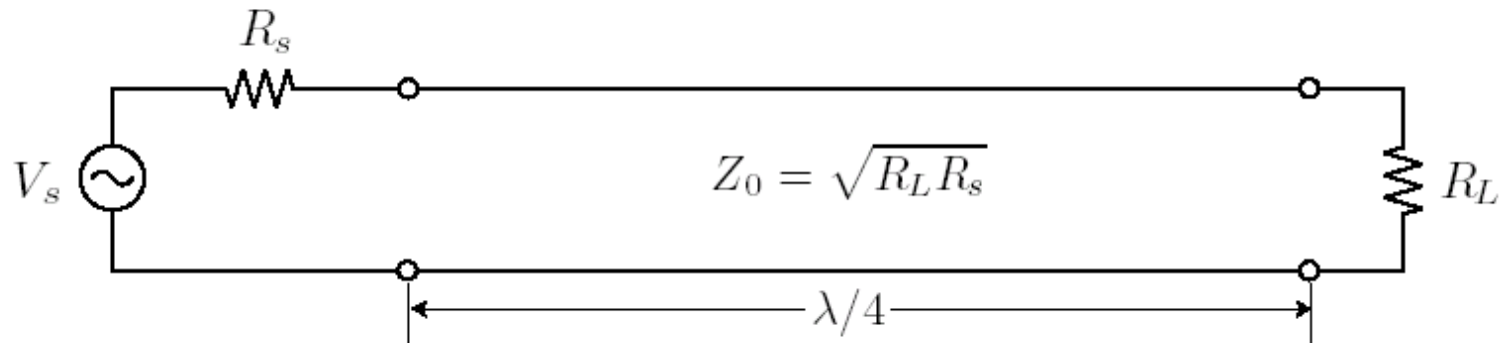
- *...For the matching network alone !*  
 $\rightarrow$  impedance matching is limited  
 $\rightarrow$  problem for low-voltage operation



$$\text{PER} = r \cdot \eta$$

source: Reynaert

# Quarter Wave Transformer



$$P_{in} = \frac{|V^+|^2}{2Z_0} (e^{2\alpha\ell} - |\rho(\lambda/4)|^2 e^{-2\alpha\ell}) \quad |\rho(\lambda/4)| = |\rho_L| e^{-2\alpha\lambda/4}$$

$$P_L = \frac{|V^+|^2}{2Z_0} (1 - |\rho_L|^2) \quad IL = \frac{P_L}{P_{in}} = \frac{1 - |\rho_L|^2}{e^{2\alpha\lambda/4} - |\rho(\lambda/4)|^2 e^{-2\alpha\lambda/4}}$$

- Quarter wave line is a nice way to impedance match source and load. T-line comes for free since we can use the board trace at high frequency.
- How does this vary with matching ratio?

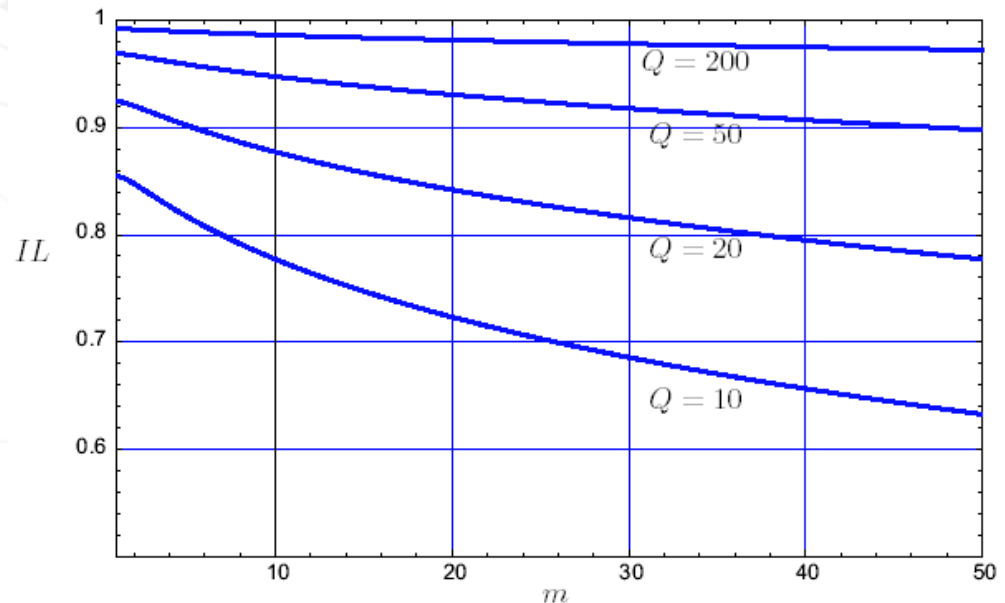
# T-Line Loss

$$m = \frac{R_{hi}}{R_{lo}} \geq 1$$

$$IL = \frac{1}{\cosh(2\alpha\lambda/4) + \frac{1+m}{2\sqrt{m}} \sinh(2\alpha\lambda/4)}$$

$$2\alpha\lambda/4 = \frac{\alpha\lambda}{2} = \frac{\beta}{2Q} \lambda 2 = \frac{\pi}{2Q}$$

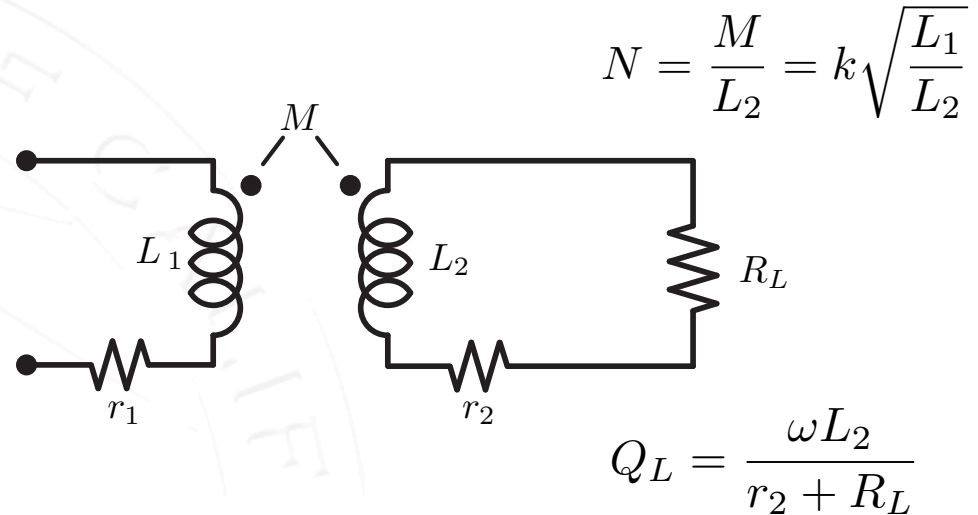
$$IL(Q, m) = \frac{1}{\cosh(\frac{\pi}{2Q}) + \frac{1+m}{2\sqrt{m}} \sinh(\frac{\pi}{2Q})}$$



- For FR4 and other lossy dielectrics, the IL can be quite high. Multi-section T-line helps (lower Q) but area is a big constraint.

# Transformer Matching

- Simple model of transformer as coupled inductors with series loss.



$$IL = \frac{P_L}{P_L + P_{diss}}$$

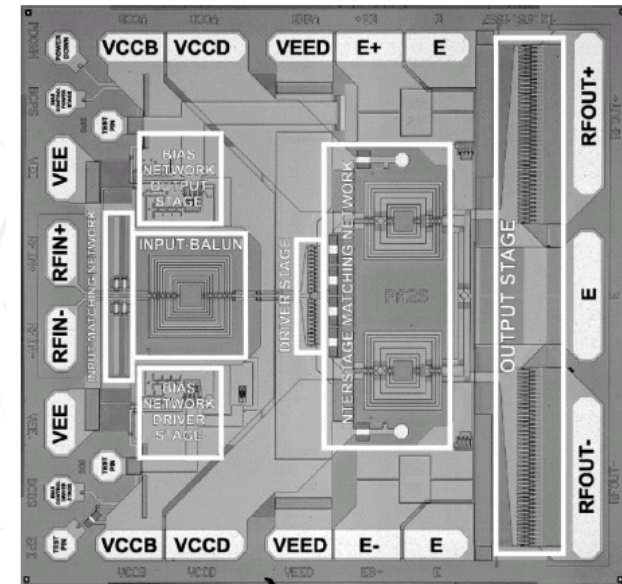
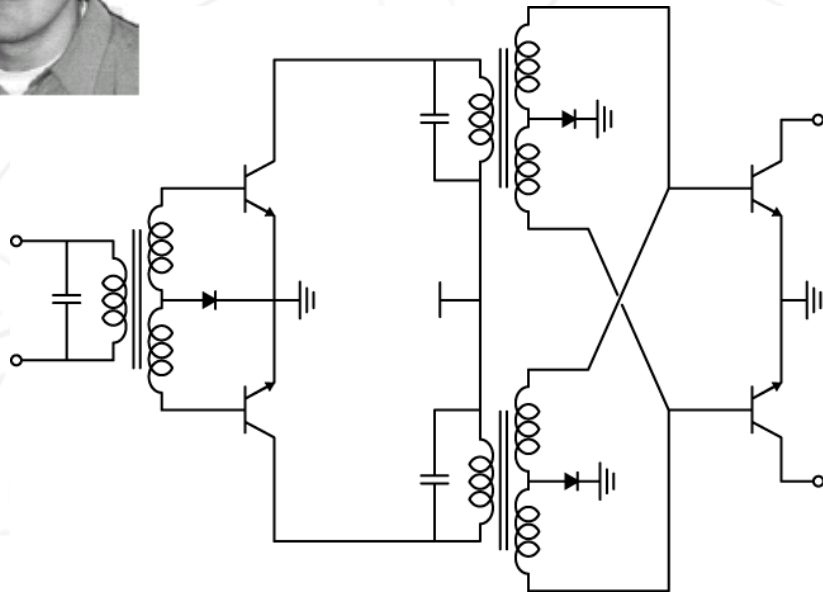
$$IL = \frac{R_L}{r_1 + r_2 + R_L + \left(\frac{L_2}{M}\right)^2 r_1 + \frac{r_1(r_2 + R_L)^2}{\omega^2 M^2}}$$

- Key result: loss is nearly independent of the matching ratio!

$$IL \approx \frac{R_L}{r_1 + r_2 + R_L + \frac{r_1}{N^2 Q_L^2}}$$

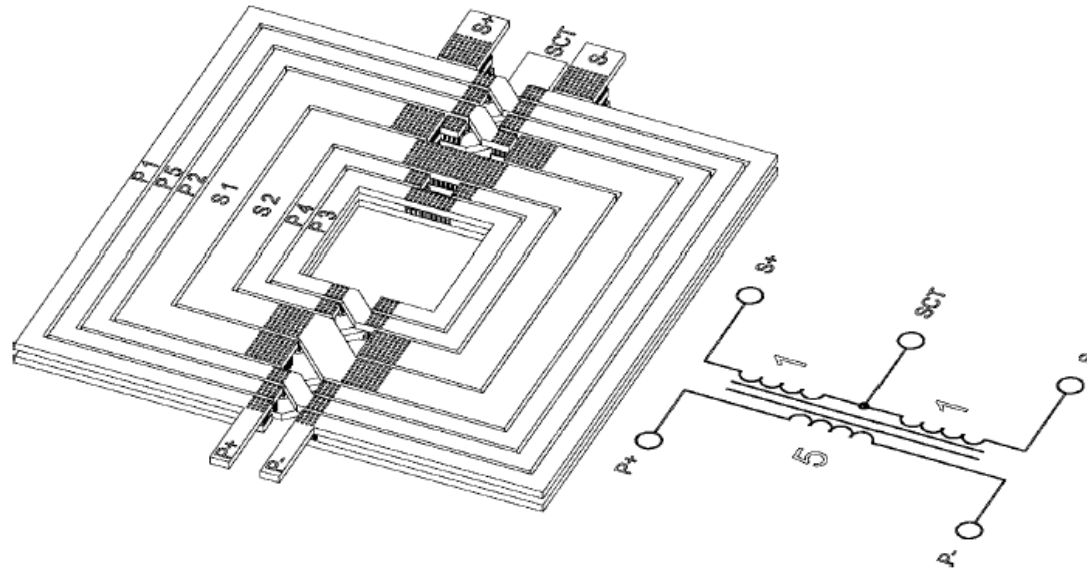


# Simbürger PA Interstage Drive



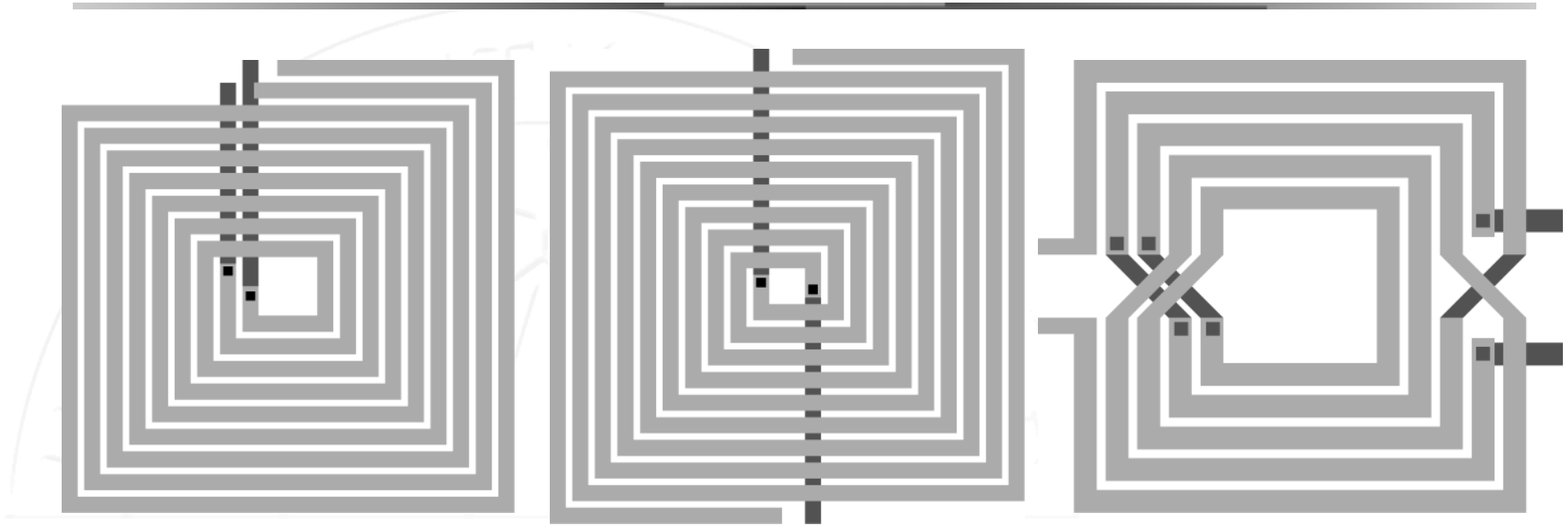
- Simbürger and co-authors demonstrated that on-chip transformer can be used to drive large bipolar PA devices
- Output power  $\sim 5\text{W}$ , 55% PAE

# Simbürger Transformer



- Siemens team showed that on-chip transformers were useful for PA interstage matching.
- Can they be used for the output stage as well? ... Caltech DAT

# Planar Transformer Layout

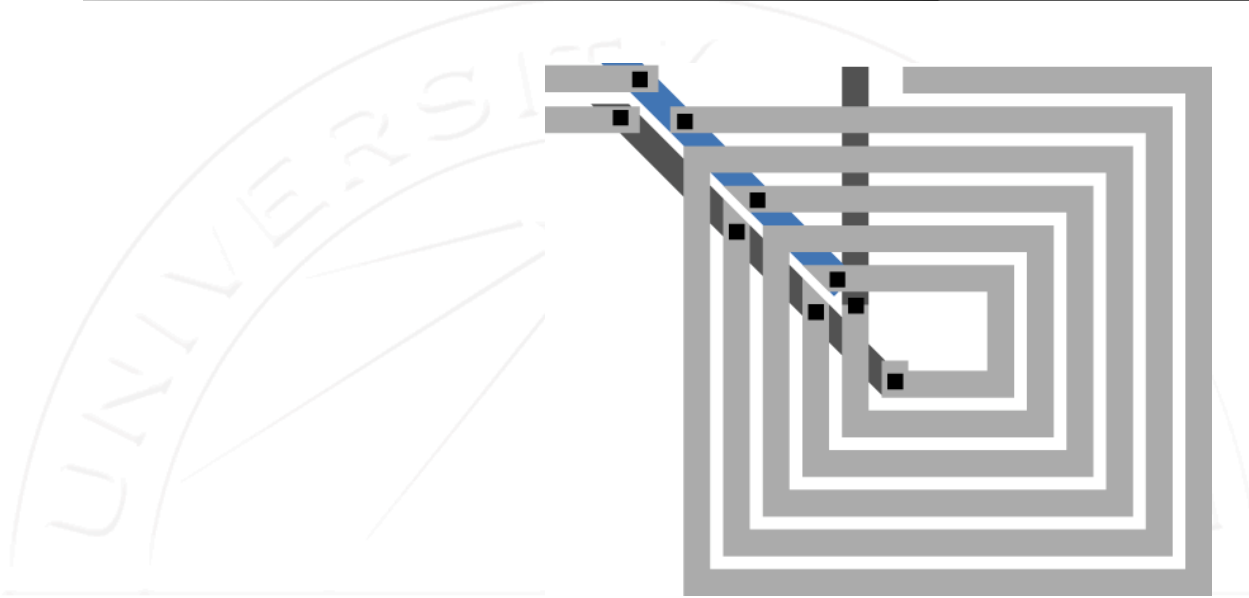


- Moderately high  $k$  factor transformers can be realized using two metal layers
- Different layout styles offer an asymmetric primary/secondary, a symmetric prim/sec, and a fully balanced and symmetric prim/sec



# Transformer Turns Ratio

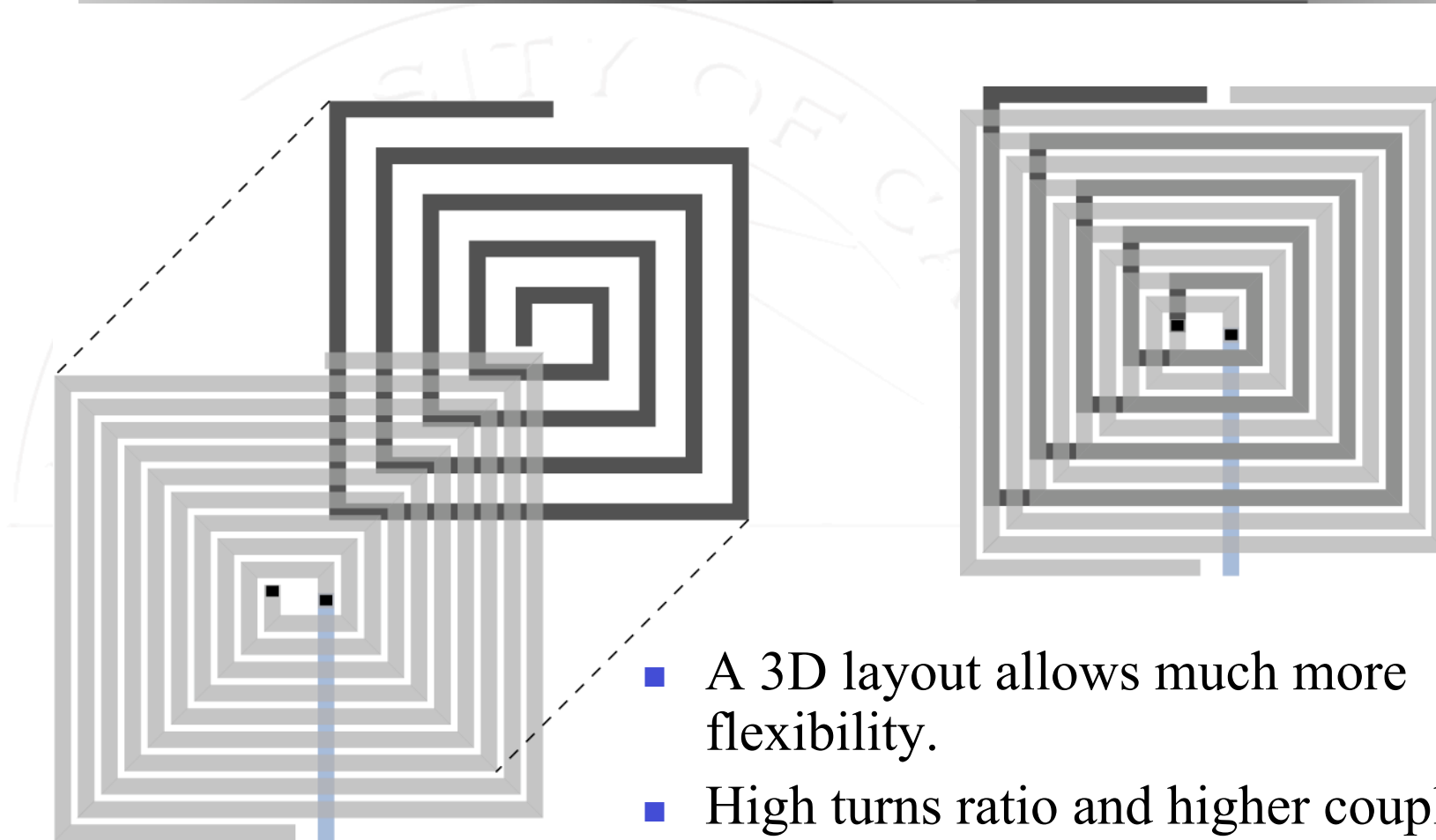
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- With a planar layout, turns ratio can be obtained from omitting turns on the secondary or by connecting secondary turns in parallel
- Parallel connection offers lower loss on secondary

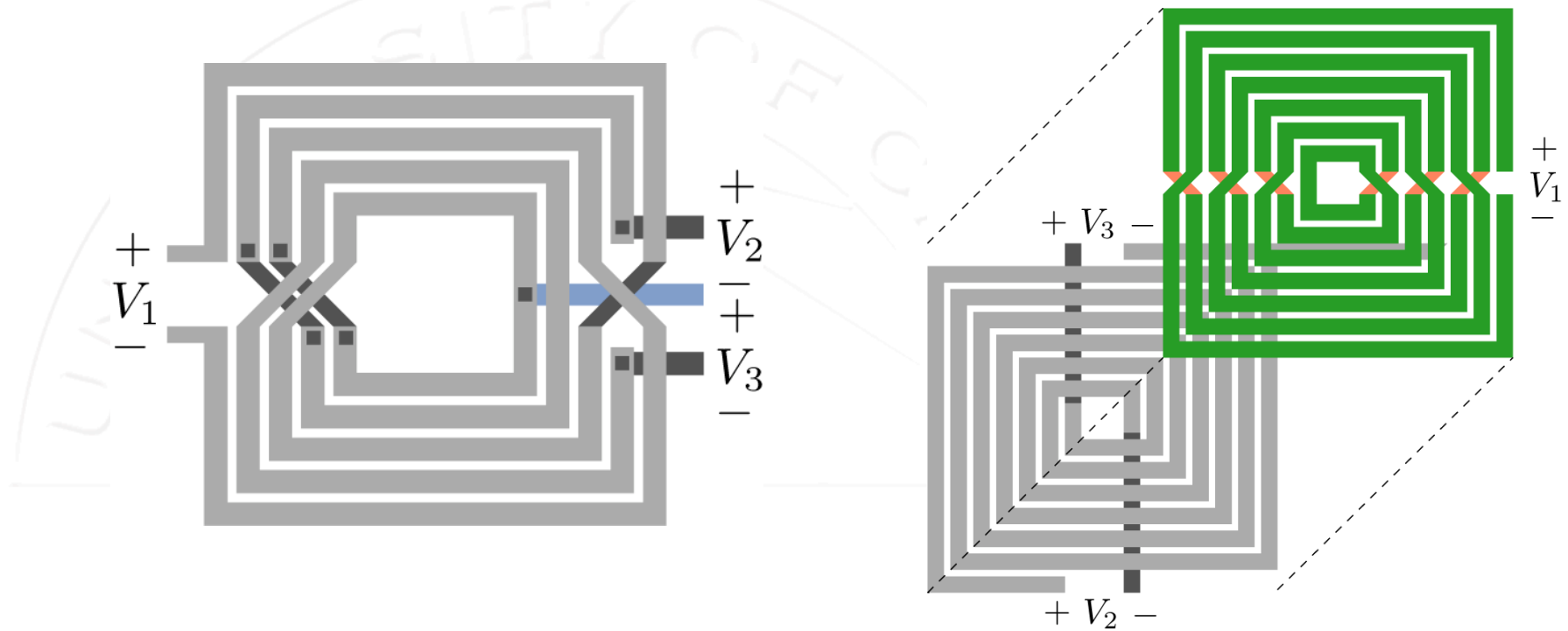
# High Turns 3D Ratio Transformers

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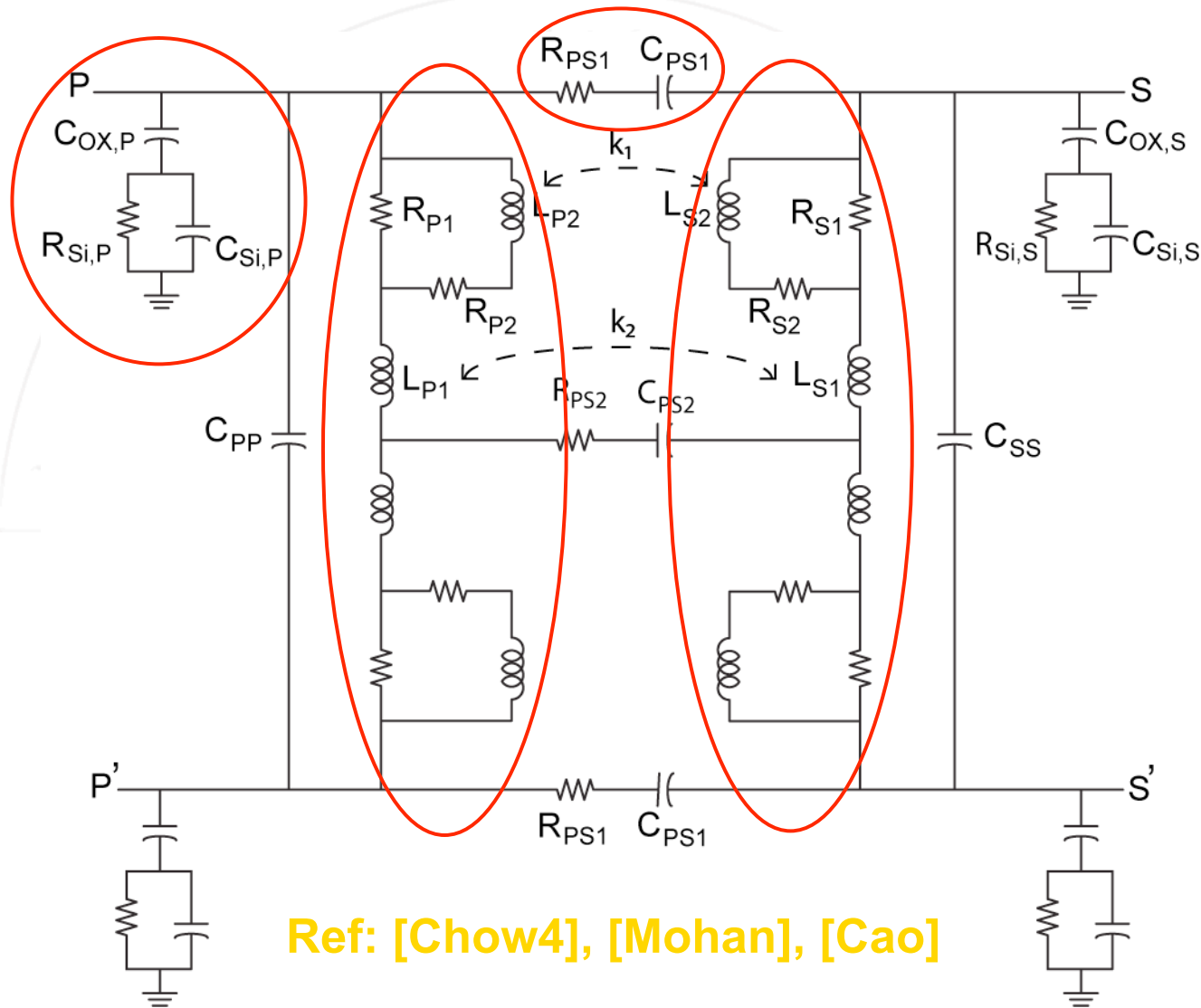
- A 3D layout allows much more flexibility.
- High turns ratio and higher coupling factor can be implemented in a simple way

# Balun Layout



- Symmetric structures can be used to build baluns.
- Baluns are a natural fit in fully differential circuits.

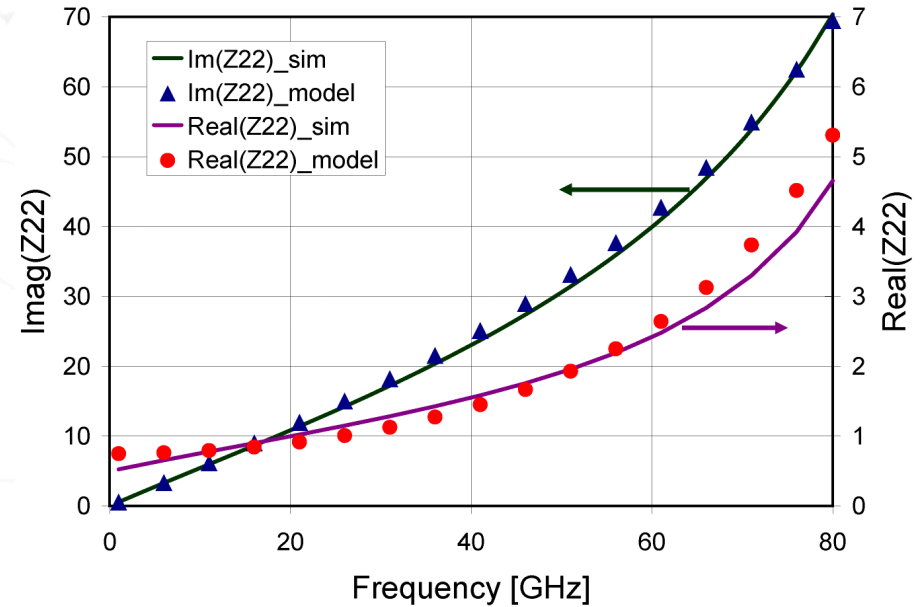
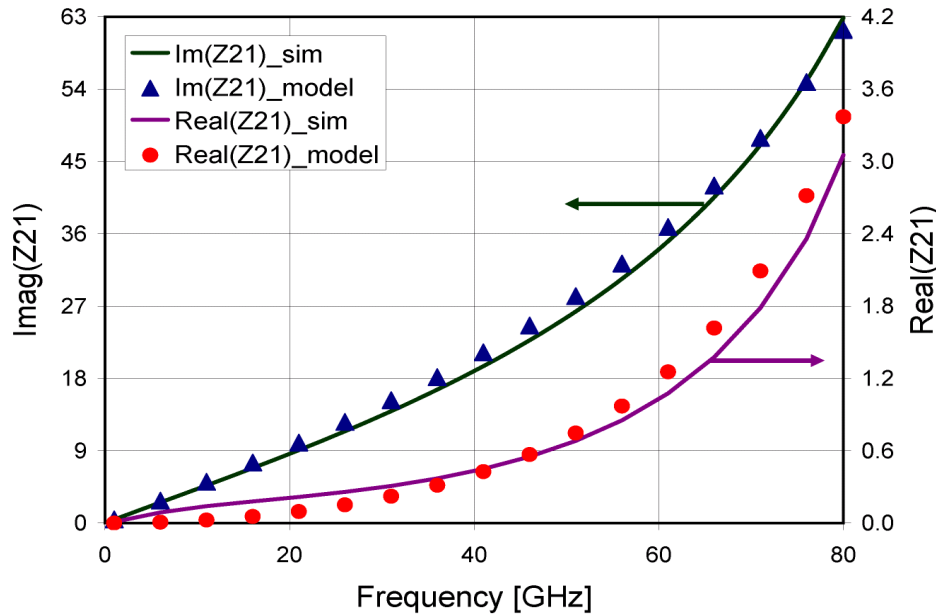
# Lumped Modeling of Transformer



Ref: [Chow4], [Mohan], [Cao]

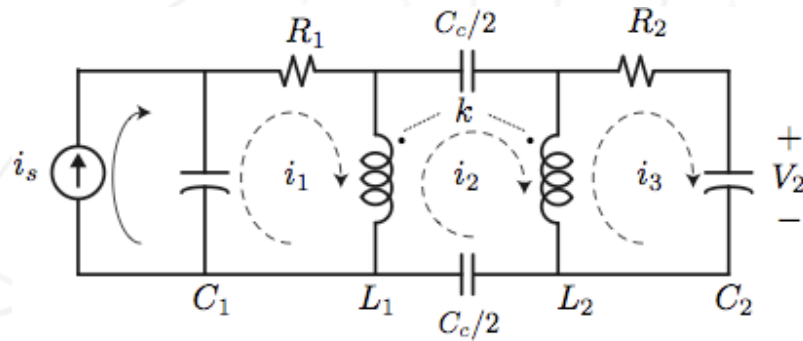
- Symmetric  $2\pi$  model
- RL network models frequency-dependent loss
- Winding capacitance for SRF
- Asymmetric substrate network

# Comparison of Results



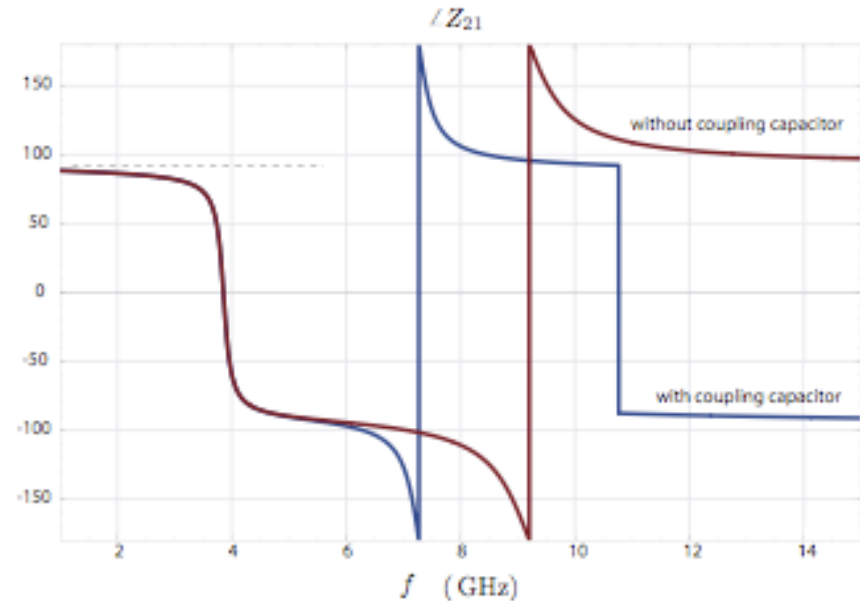
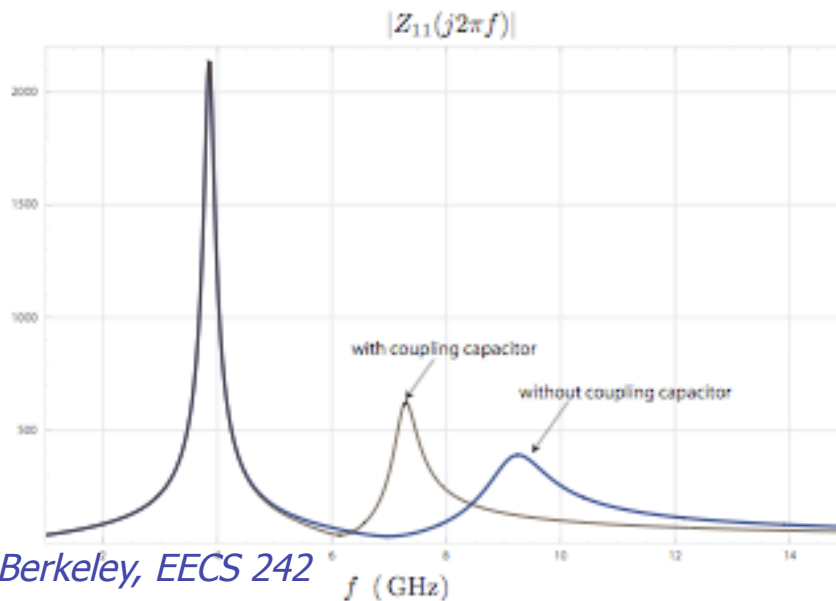
- Necessary to match both y, z parameters instead of s-parameters only
- Good match up to high frequencies

# Transformer Resonant Modes



$$\omega^+ = \sqrt{\frac{1}{C_0(L_1 + L_2 + 2M)}} \quad \omega^- = \sqrt{\frac{1}{(C + 2C_c)(L_1 + L_2 - 2M)}}$$

- Two modes due to odd and even excitation.
- In “even” mode the coupling capacitor  $C_c$  is not excited.

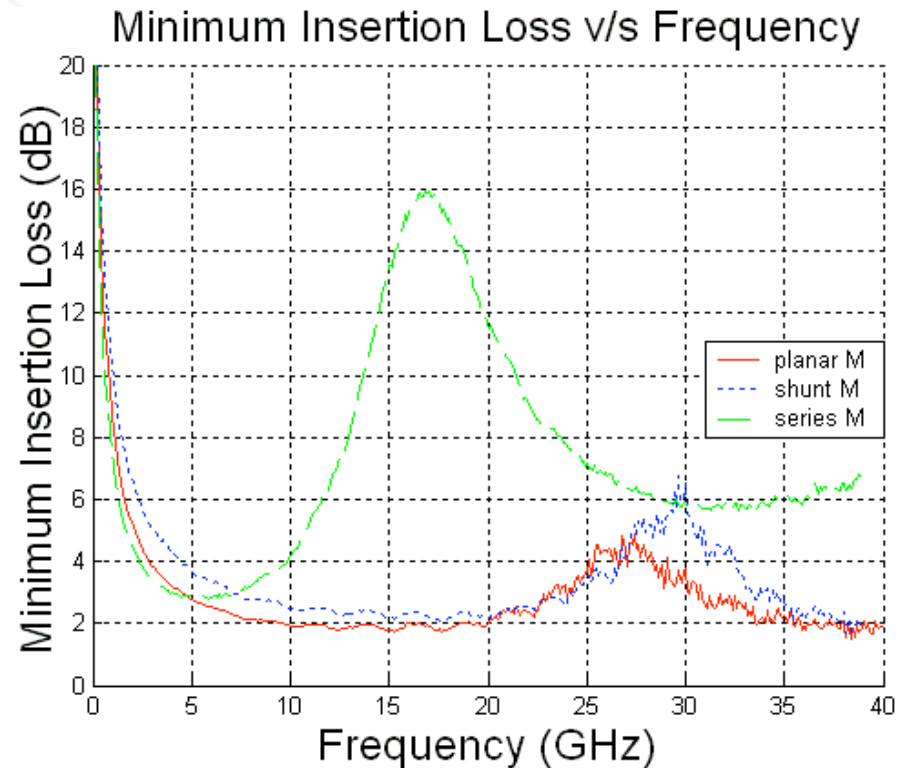
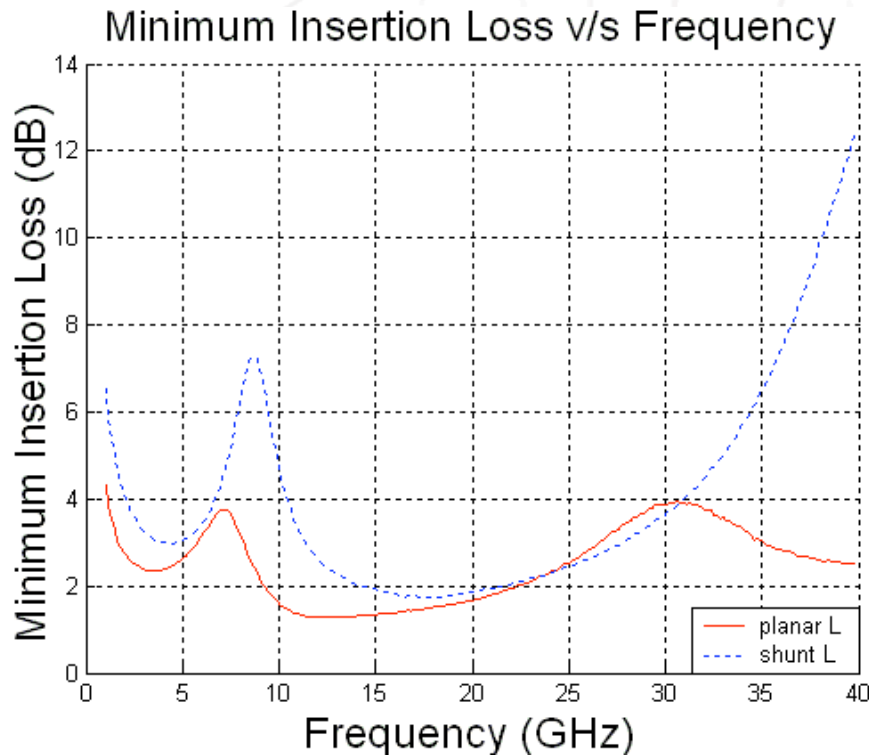


# Transformers Comparison

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- Paper published at RFIC 2004:
  - “Microwave Performance of Monolithic Silicon Passive Transformers”, Mounir. Y. Bohsali and Ali. M. Niknejad
- Compare various transformer layouts
- Define metric that takes into account bandwidth

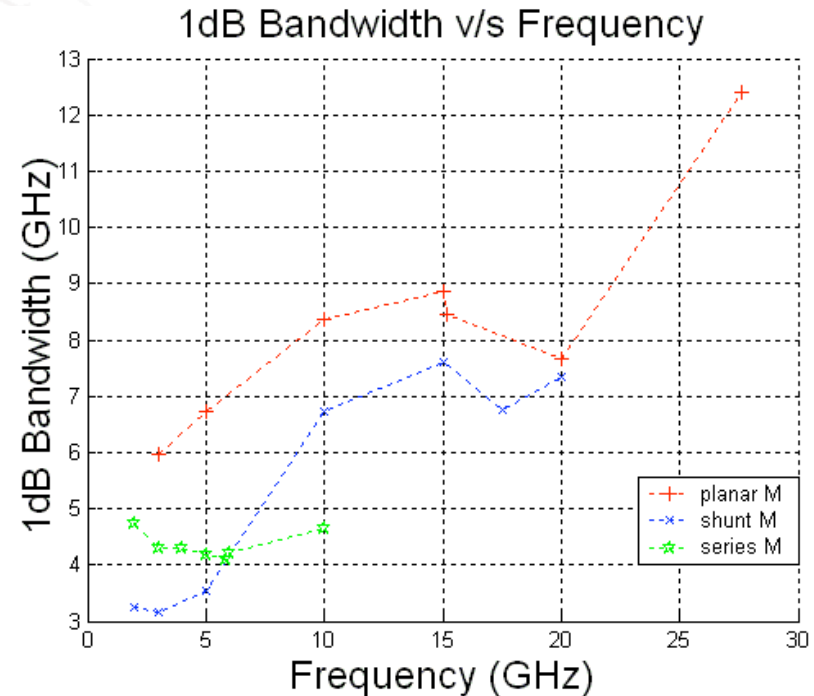
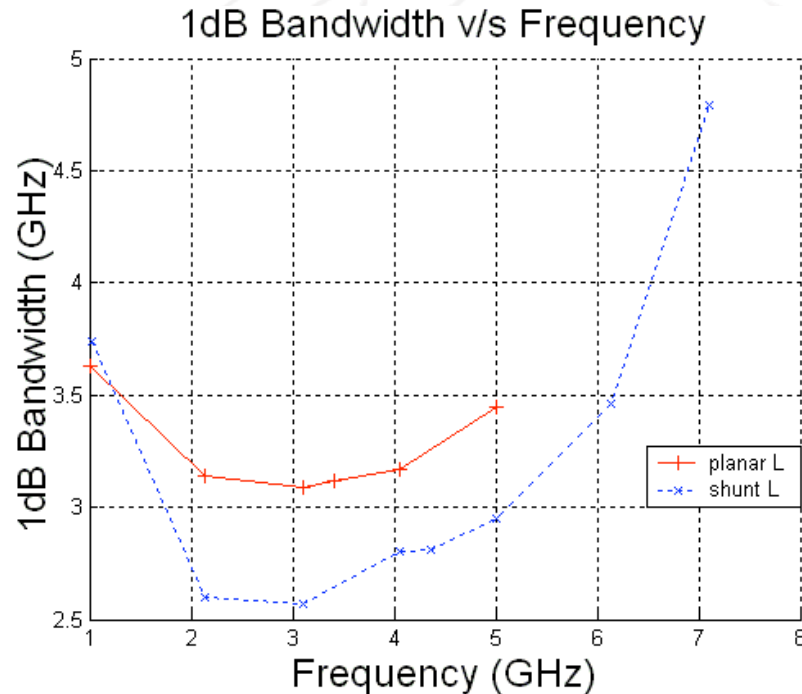
# Shunt versus Planar



- Planar versus shunt have similar behavior below “resonance” with 2-3 dB of loss.
- Series structure has much lower resonance frequency.

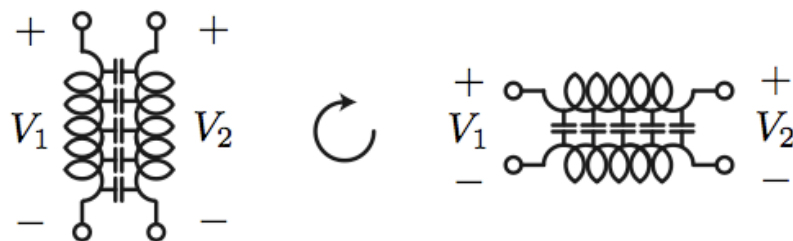


# Transformer Bandwidth

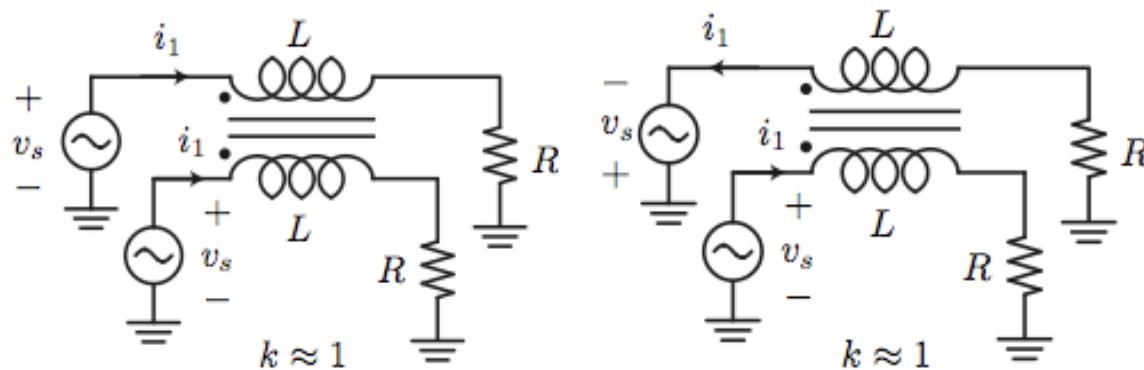


- Define a new metric: bandwidth over which gain is within 1 dB of “optimal” gain (for a bi-conj. match)
- Planar structure has very good bandwidth (50-150%), and other structures are worse, but series structure is significantly worse.

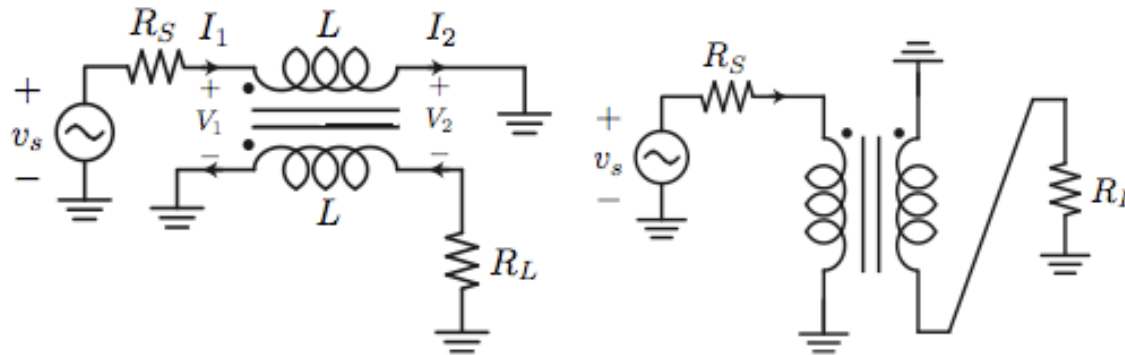
# Transmission Line Balun



- Turn parasitic coupling capacitance into a distributed broadband transmission line!
- Excite the differential mode rather than the odd mode.



# Broadband Inverter



$$V_1 = (\cosh \gamma \ell + \sinh \gamma \ell) V_2 = e^{\gamma \ell} V_2$$

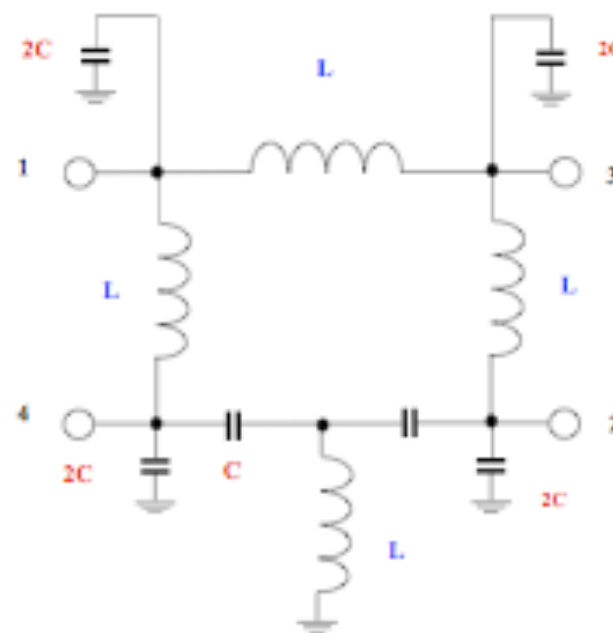
$$v_L = -V_2 = -e^{-\gamma \ell} V_1$$

- The voltage at the load is inverted if the length of the line is small ( $\sim 1/10$  wavelength)
- Note that line excited with both odd and even mode at source but higher  $Z_0$  and loss of line rejects even mode.

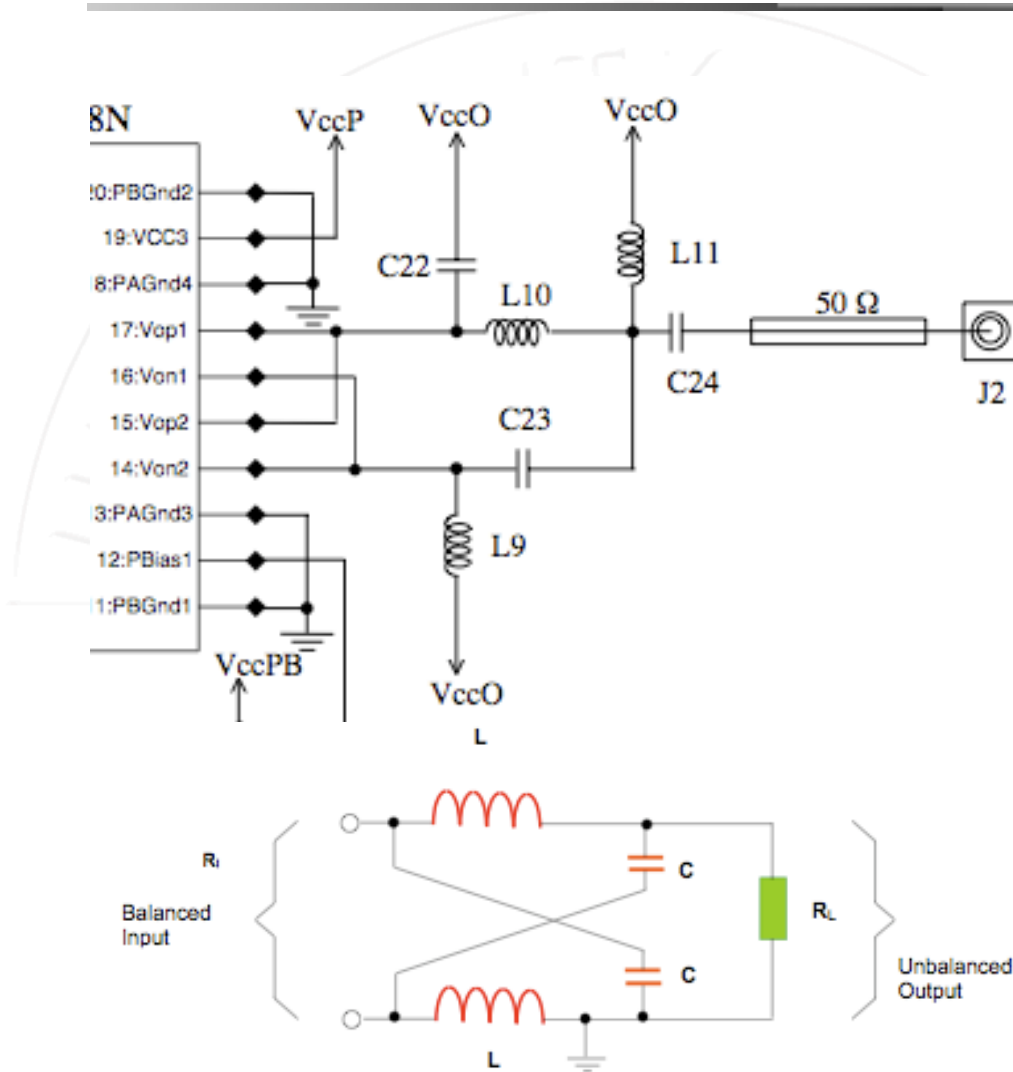
# LC Coupler

- Lumped 180° coupler
- Low bandwidth (20%)
- Element values

$$\frac{1}{\omega C} = \omega L = \sqrt{2}Z_0$$



# LC Balun



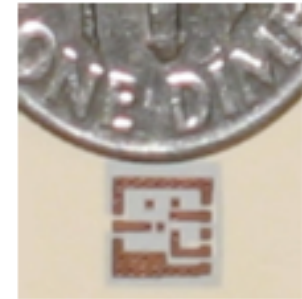
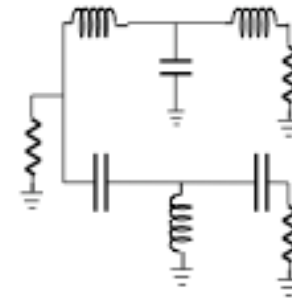
- Essentially a bridge with phase lead and lag networks.
- Bandwidth? Depends on Q of match since this is just a high-pass and low-pass matching network.

$$Z_c = \sqrt{R_i R_L}$$

$$L = \frac{Z_c}{\omega} \quad C = \frac{1}{\omega Z_c}$$

# Measured Lumped Balun

- 20% fractional bandwidth
- IL low due to substrate
- Phase/amplitude balance relatively poor.



Frequency	5.8-6.8 GHz
Return Loss	11 dB
Insertion Loss	0.7 dB
Amplitude Imbalance	0.5 dB
Phase Imbalance	3.6°

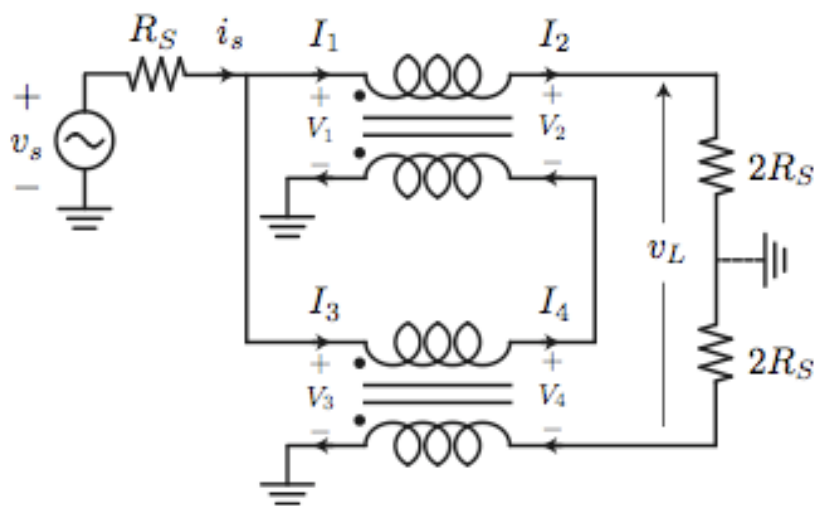
## An Integrated Double Balanced Mixer on Multilayer Liquid Crystalline Polymer (M-LCP) Based Substrate

Wansuk Yun<sup>1</sup>, Vinu Govind<sup>1</sup>, Sidharth Dalmia<sup>2</sup>, Venky Sundaram<sup>1</sup>, Madhavan Swaminathan<sup>1</sup>, and George E. White<sup>2</sup>

<sup>1</sup>Georgia Institute of Technology, Electrical and Computer Engineering, Atlanta, GA 30332, U.S.A, 404-385-6417

<sup>2</sup>Jacket Micro Devices, Suite 213, 75 5<sup>th</sup> Street, Atlanta, GA 30308, USA, 404-526-6046

# Transmission Line Balun



- This works as a balun over a very broad band. If length is quarter wavelength, the even mode is rejected at center frequency.

$$G_v = \frac{v_L}{v_s} = \frac{2}{\cos kl + j \sin kl \frac{Z_0}{2R_S}} = \frac{2}{e^{jkl}} = 2e^{-jkl}$$

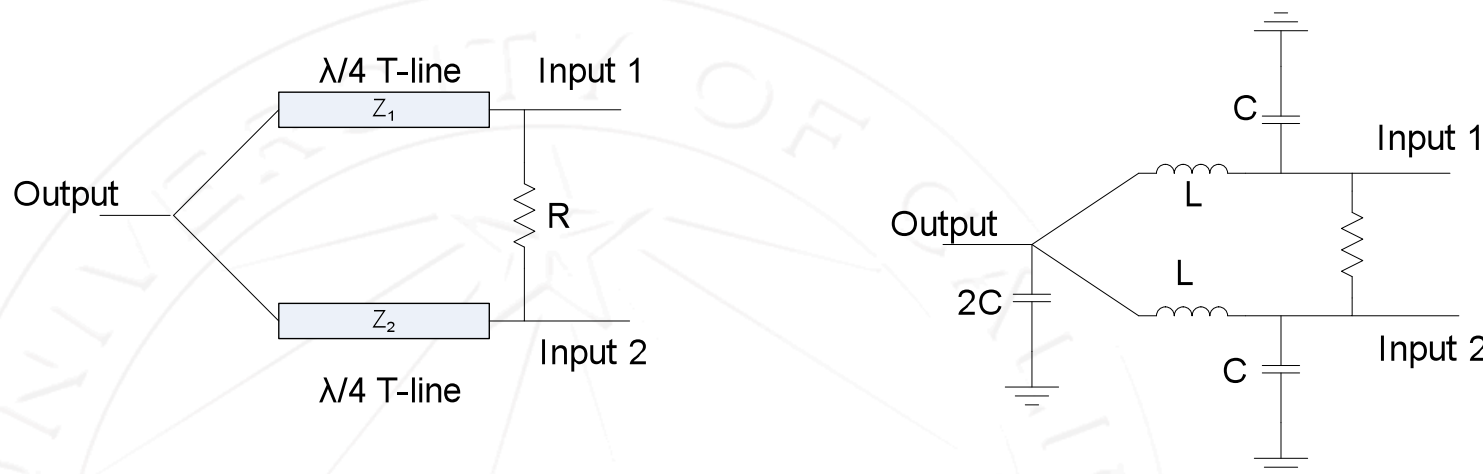
# Marchand Balun



- Improved bandwidth
- Less sensitivity to even-mode impedance
- Requires two quarter wave structures.

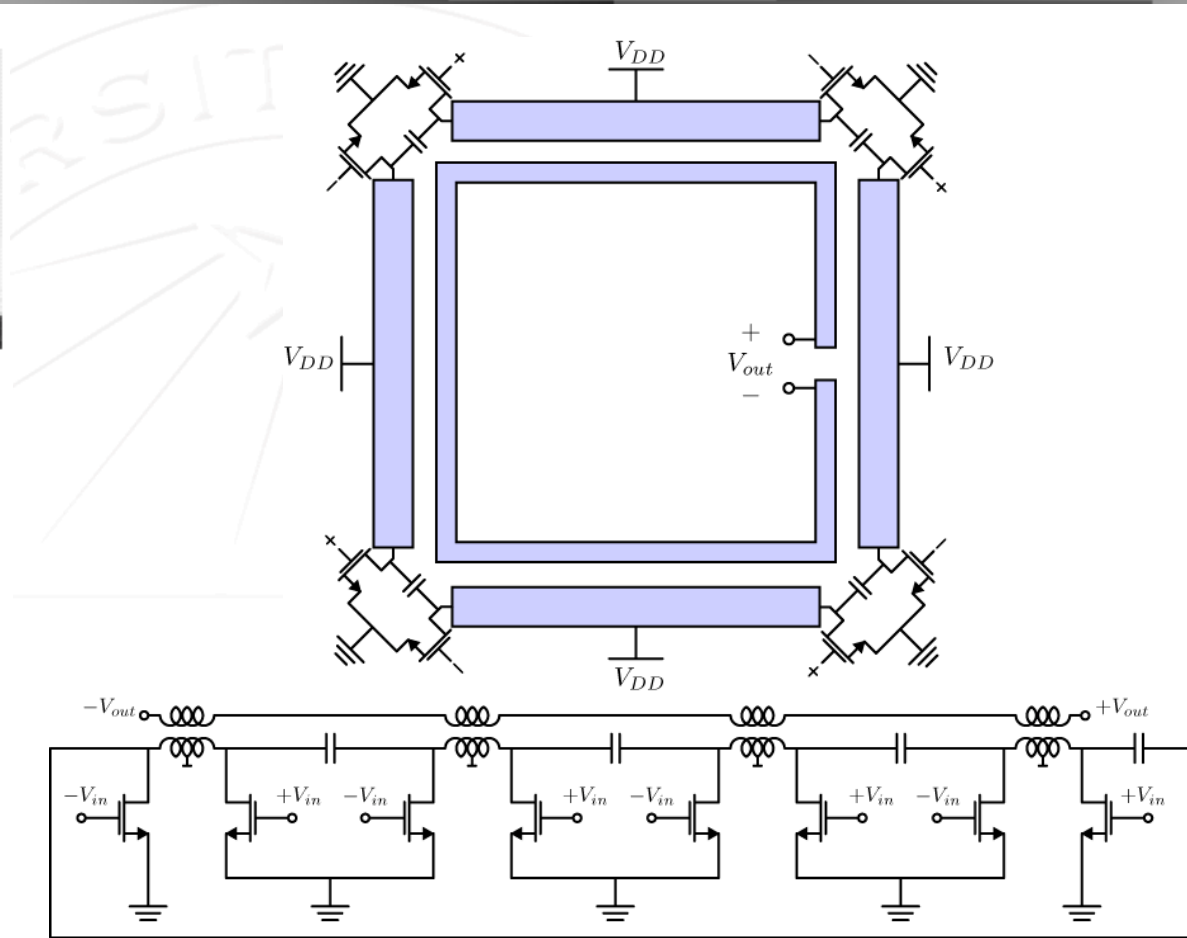


# Wilkinson Power Combiner



- Theoretically we cannot build a *lossless* 3 port device with isolation and power combining.
- The Wilkinson uses a resistor that is normally “open circuited” (even mode) and does not generate loss.
- Effective for high frequency designs or using LC circuit at low frequency.

# Cal Tech DAT



- Use virtual grounds wisely to turn 1:1 coupled lines into a transformer loop.

# Transformer FOM

- Unlike inductor Q factor, there is no obvious “silver bullet” FOM for transformers.
- For power combining applications, the maximum power gain (bi-conjugate match) has been used as a figure of merit
- For a simple 1:1 transformer, the maximum gain is a function of only the  $Q$  and  $K$  factors

$$G_{max} = \frac{y_{21}}{y_{12}}(k - \sqrt{k^2 - 1}) = k - \sqrt{k^2 - 1}$$

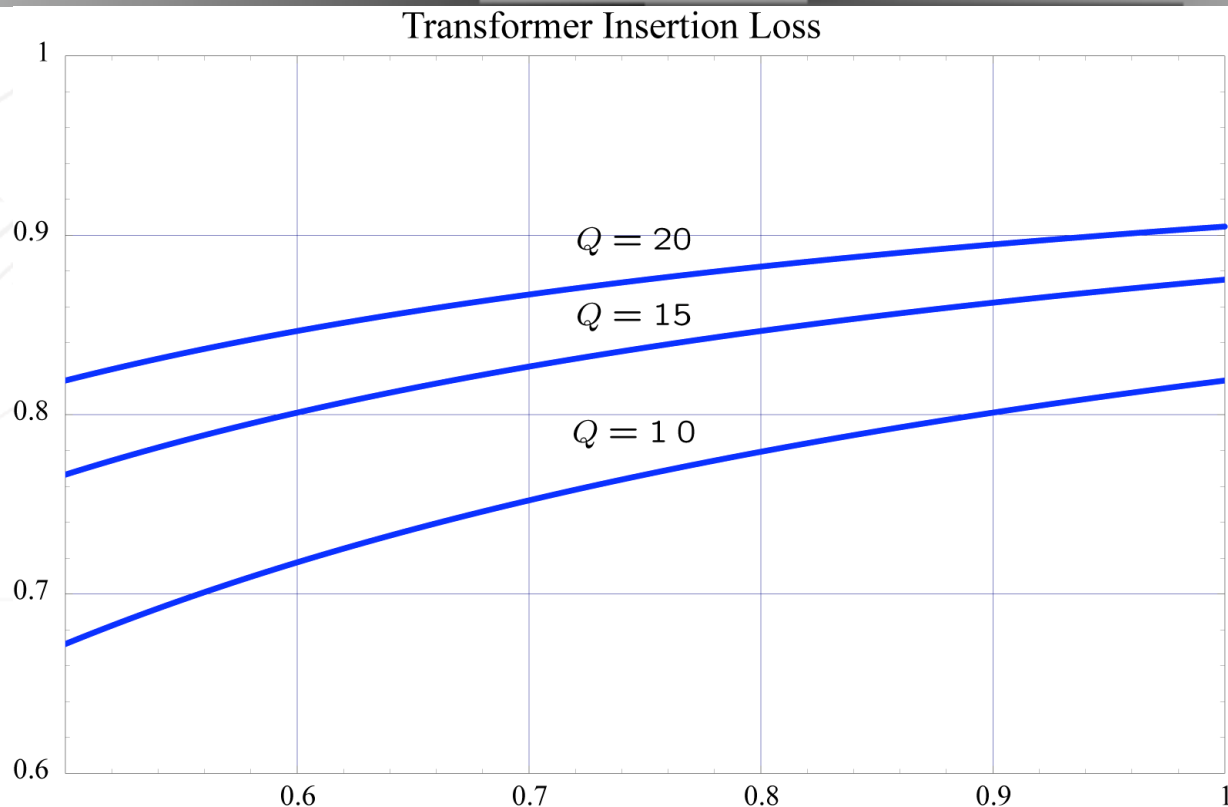
$$Z = \begin{pmatrix} R_p + j\omega L_p & j\omega M \\ j\omega M & R_s + j\omega L_s \end{pmatrix}$$

$$k = \frac{2\Re(z_{22})\Re(z_{11}) - \Re(z_{21}z_{12})}{|z_{21}z_{12}|}$$

$$k = \frac{2R_x^2 + \omega^2 M^2}{\omega^2 M^2} = \frac{2R_x^2 + \omega^2 K^2 L^2}{\omega^2 K^2 L^2}$$

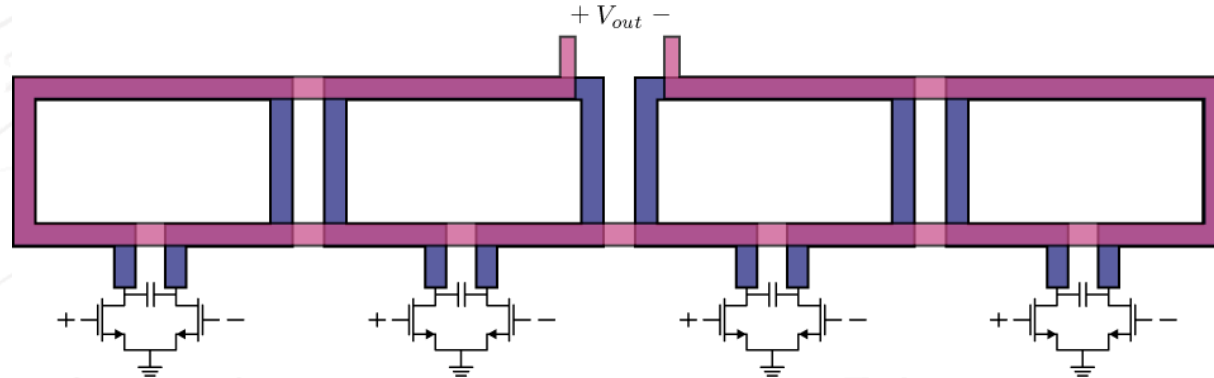
$$G_{max}(Q, K) = 1 + \frac{2}{Q^2 K^2} - 2\sqrt{\frac{1}{Q^4 K^4} + \frac{1}{Q^2 K^2}}$$

# Transformers for Power Combining



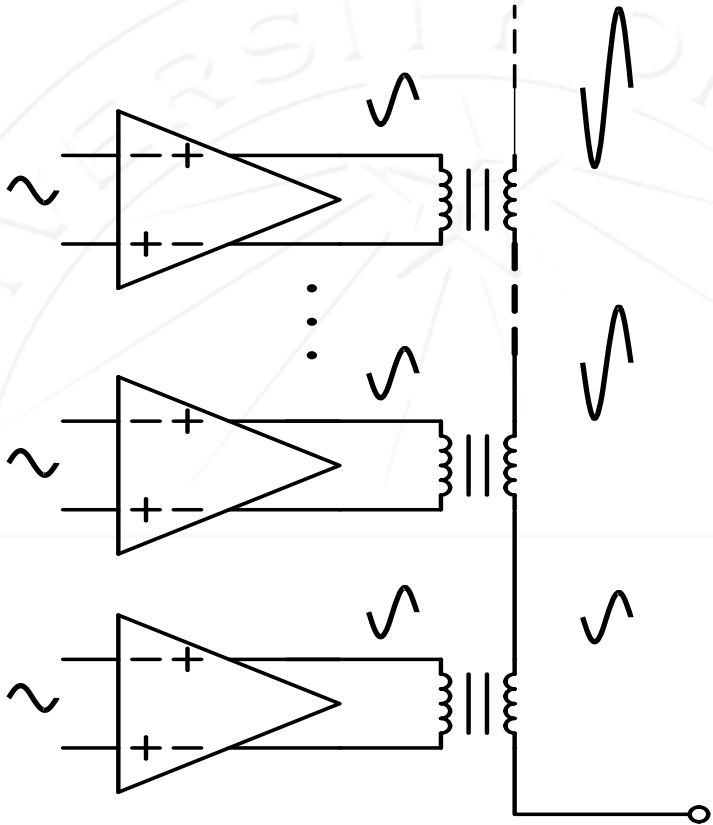
- Notice that relatively low insertion loss is possible with moderate on-chip  $Q$  and  $K$  factors, thus allowing fully-integrated transformers
- Connecting 1:1 transformers in series and shunt, we can perform efficient power combining *independent* of the number of sections [Caltech DAT architecture]

# Transformer Power Combining Layout

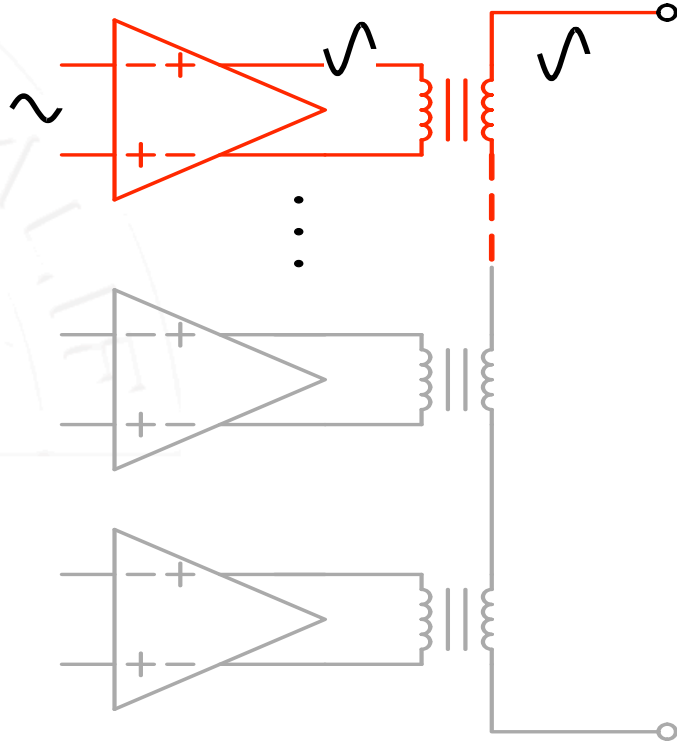


- Very simple layout
- Don't get DAT benefit → have extra “leads” that waste power
- But can turn off individual stages for power back-off
- Can easily scale power by adding more stages: design core driver stage

# Fully Integrated Dual Mode CMOS PA



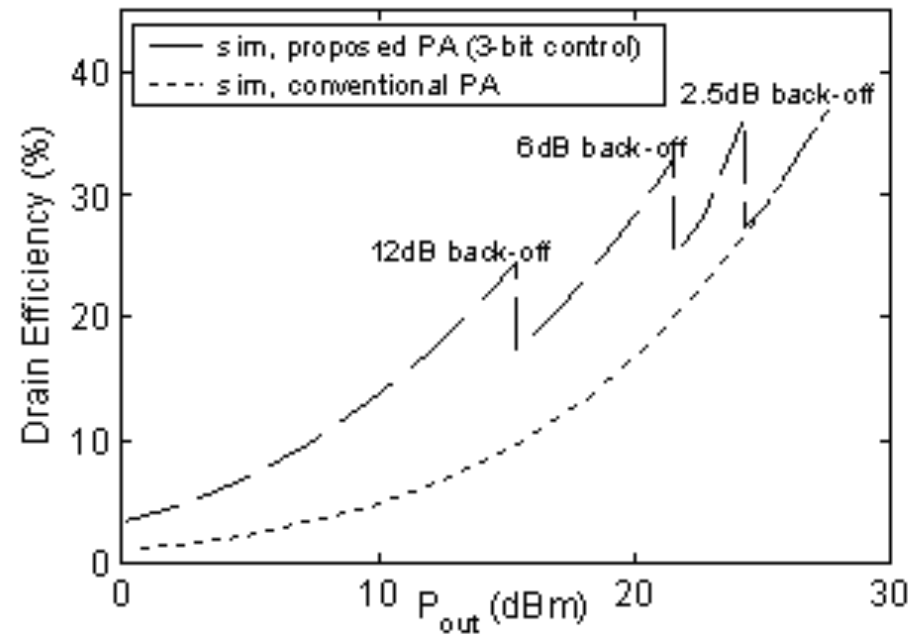
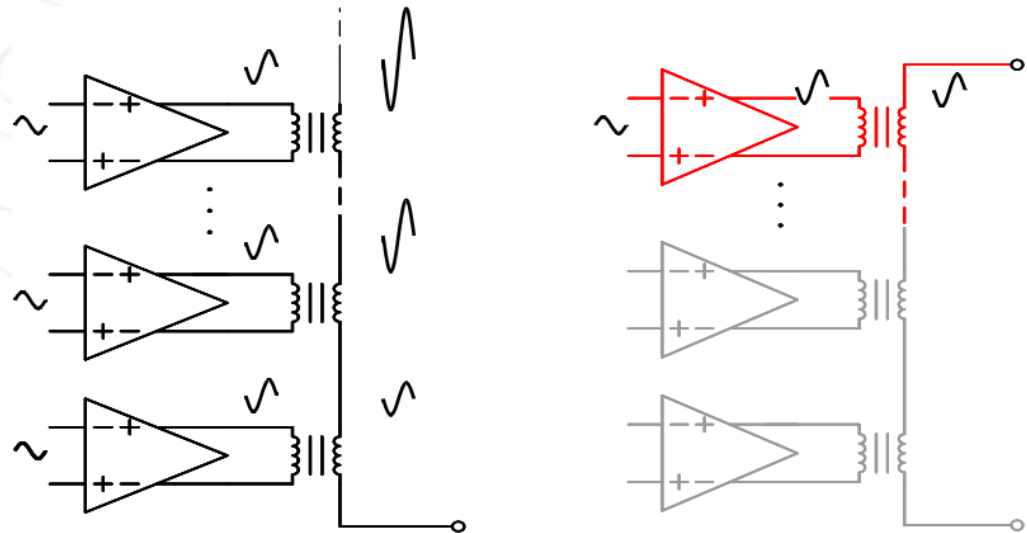
Peak Output Power Mode



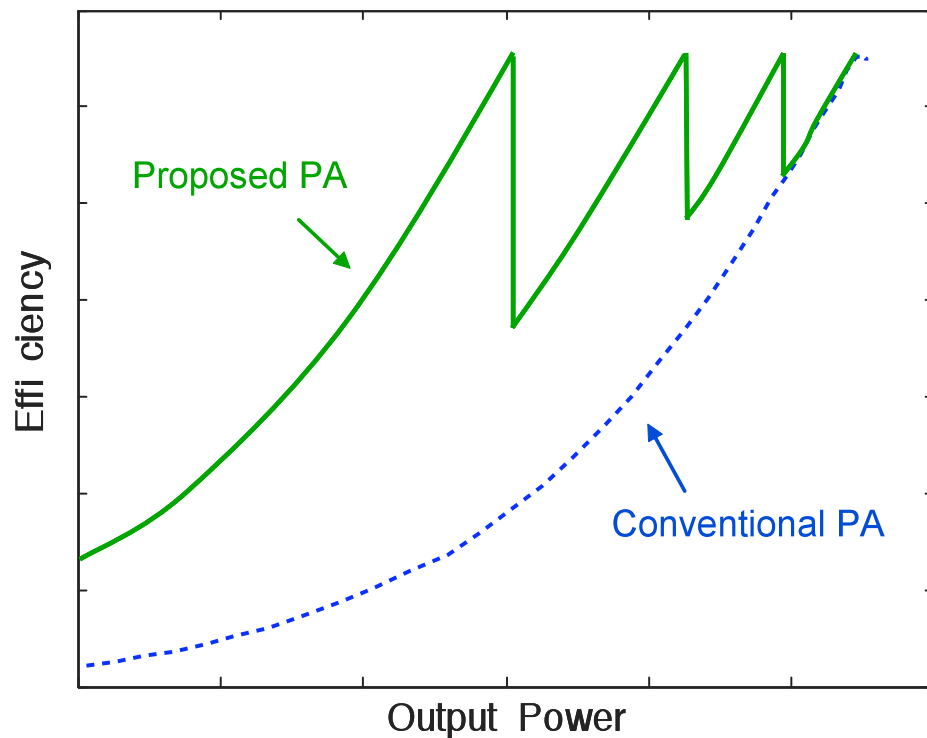
Power Back-off Mode

# Power Combining and Control

- Use transformer to perform efficient power combining
- Can also use structure for efficient power back-off to improve average power efficiency
- At moderate back-off (6 dB), efficiency close to peak level



# Power Control and Efficiency Enhancement



$$\eta_D = \frac{P_{OUTPUT}}{P_{SUPPLY}} = \frac{1}{2} \frac{V_{RF} I_{RF}}{V_{SUPPLY} \cdot I_{DC}}$$

At power back-off

Reduce DC current

Modulate load



# Load Modulation

$$Z_{m,j} = \frac{\left( R_L + \sum_{i=1}^N m_i^2 \cdot R_{PA,i} \right) \cdot V_{pa,j}}{m_j \cdot \sum_{i=1}^N m_i \cdot V_{pa,i}} - R_{PA,j} \longrightarrow R_m = \frac{R_L}{N \cdot m^2}$$

$$P_o = N^2 \cdot m^2 \cdot \frac{V_p^2}{2R_L}$$

- In general there is no isolation in the transformer so the load current of one primary will “pull” the impedance of another primary.
- It's only under the special circumstance that all windings are driven in phase that we obtain isolation.

# Efficiency at Back-Off

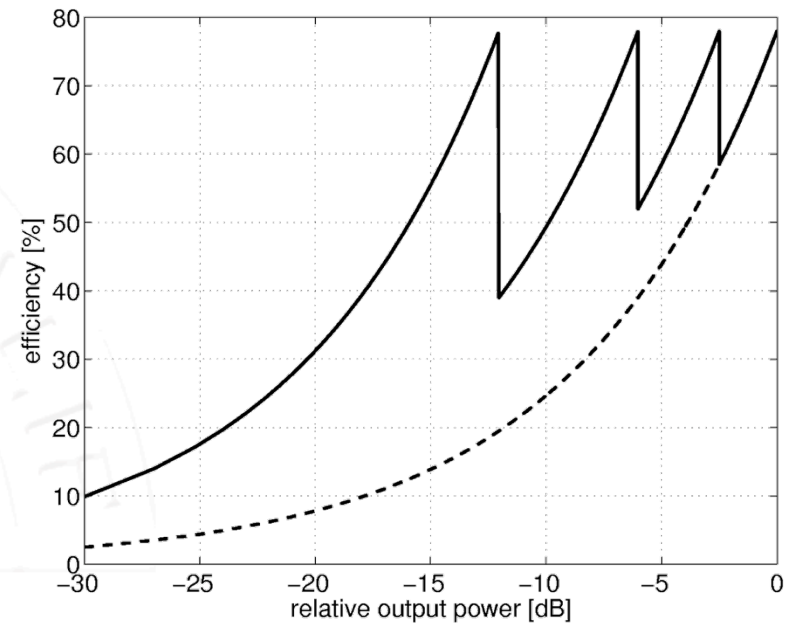
$$V_p = \frac{g_m R_L}{4} \cdot V_i = \frac{1}{4} g_m R_L \cdot V_i$$

$$\eta_B = \frac{\pi}{4} \frac{V_p}{V_{DD}}$$

$$V_{out} = 4V_p = g_m R_L \cdot V_i$$

$$V_p = \frac{g_m R_L}{2} \cdot V_i/2 = g_m R_L \cdot V_i/4$$

$$V_{out} = 2V_p = \frac{g_m R_L V_i}{2}$$



- When all four stages are on, each PA see's  $\frac{1}{4}$  of the load.
- Suppose 2 stages are turned off. Then the PA's see  $\frac{1}{2}$  the load. The voltage swing at the output drops, but the voltage on each primary remains the same!
- For Class B operation, we can theoretically achieve the same efficiency at back-off.

# Power Back-Off Mode

$$R = \frac{1}{3} R_L$$

$$A_{unit} = gm \cdot \frac{1}{3} R_L$$

$$V_o = A_{unit} \cdot V_i = gm \cdot \frac{1}{3} R_L \cdot \frac{3}{4} V_{i,max} = V_{o,max}$$

$$\eta_{overall} = \eta_{unit} = \eta_{max}$$

$$A_{overall} = N \cdot A_{unit} = gm \cdot R_L$$

$$P_{out} = N \cdot P_{unit} = 3 \cdot \frac{1}{2} \frac{V_o^2}{\frac{1}{3} R_L} = \frac{9}{2} \frac{V_o^2}{R_L} = \frac{9}{16} P_{peak}$$

- Say we back-off the input by 3/4 .
- If we turn off one amplifier, the load seen by each amplifier is now 1/3
- But the output voltage is still at the peak optimal value
- The overall efficiency is therefore at the peak value.

# **A 1.2V, 2.4GHz Fully Integrated Linear CMOS PA with Efficiency Enhancement**

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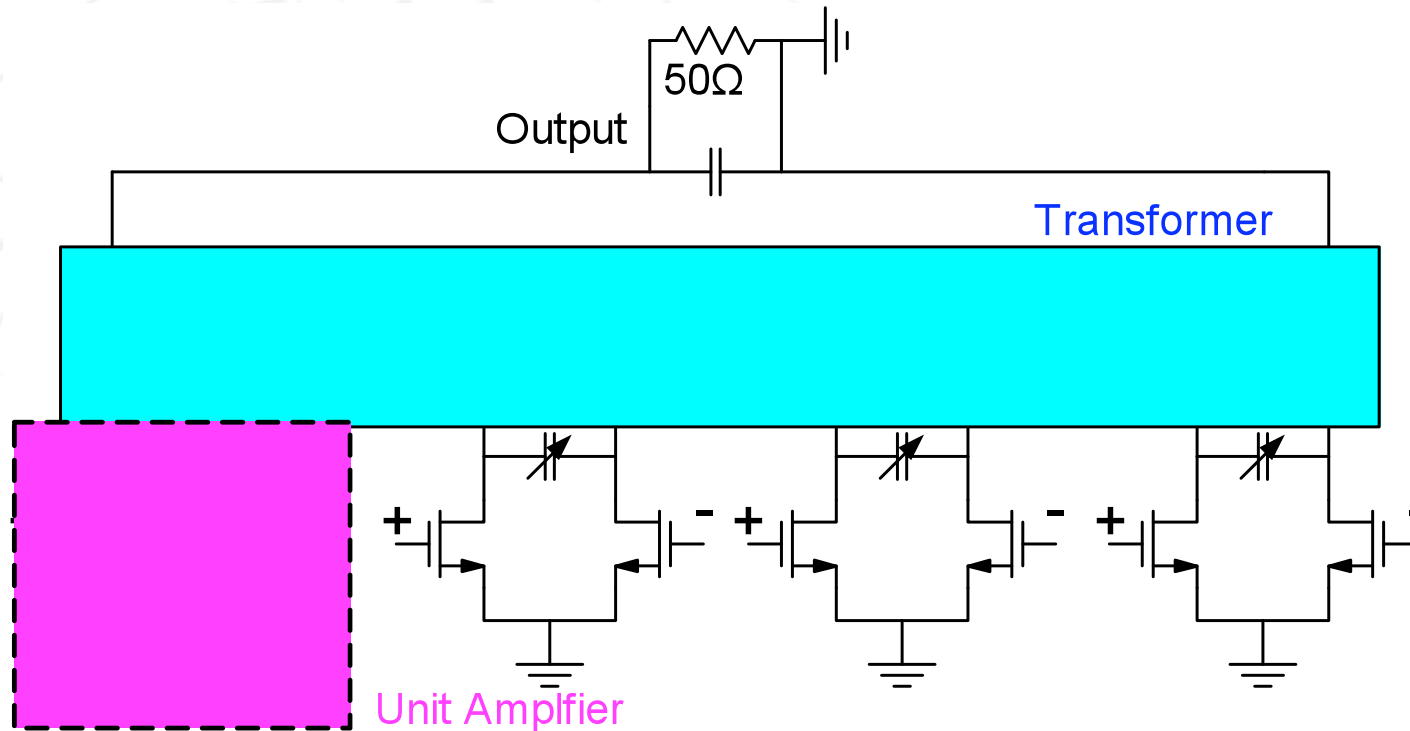
CICC 2006

Gang Liu<sup>1,2</sup>, Tsu-Jae King Liu<sup>2</sup>

Ali M. Niknejad<sup>1,2</sup>

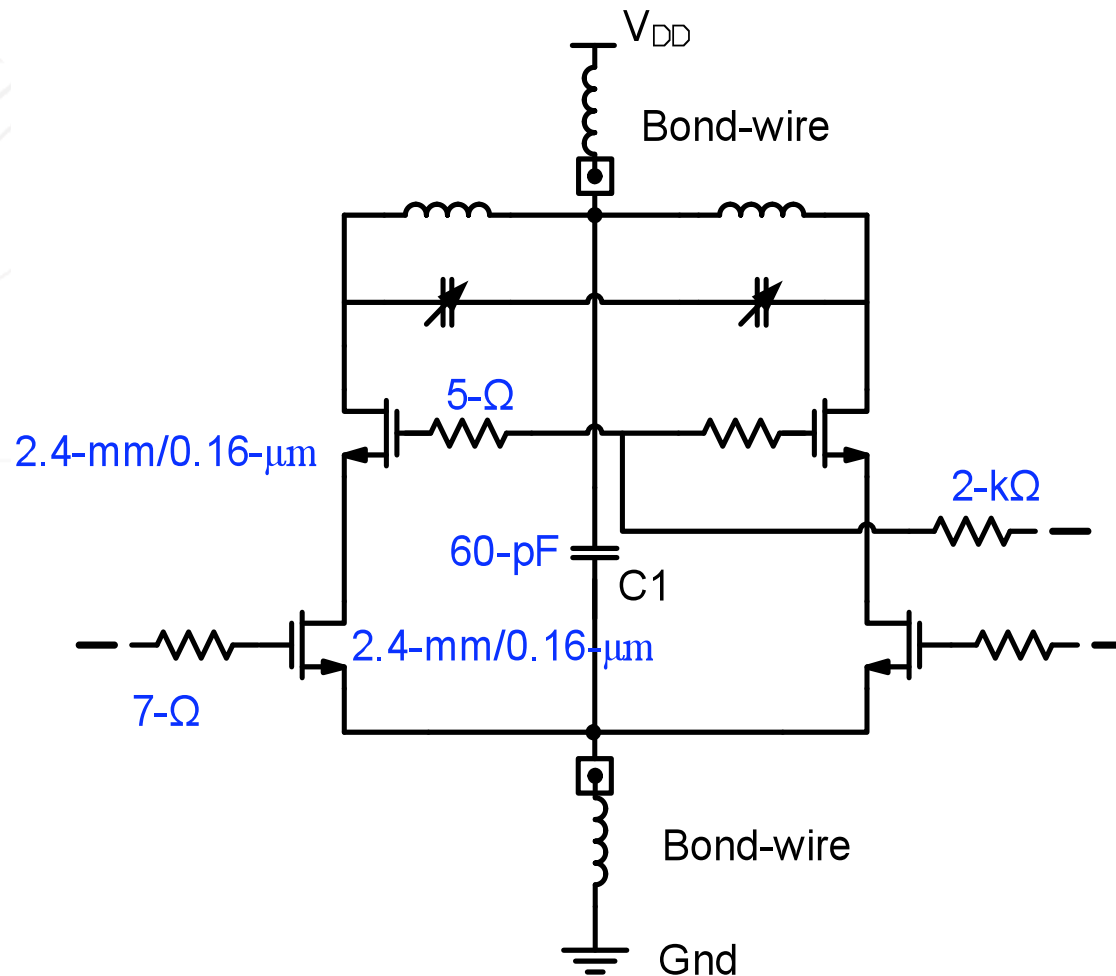
Berkeley Wireless Research Center<sup>1</sup>  
Electrical Engineering and Computer Sciences<sup>2</sup>  
University of California, Berkeley, CA, USA

# Simplified 4-Way Combiner Schematic

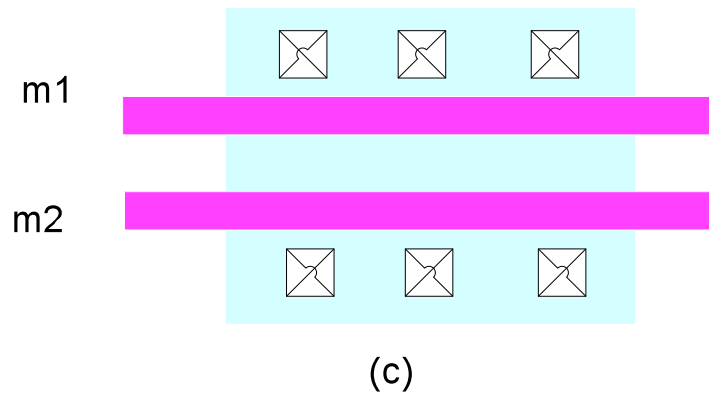
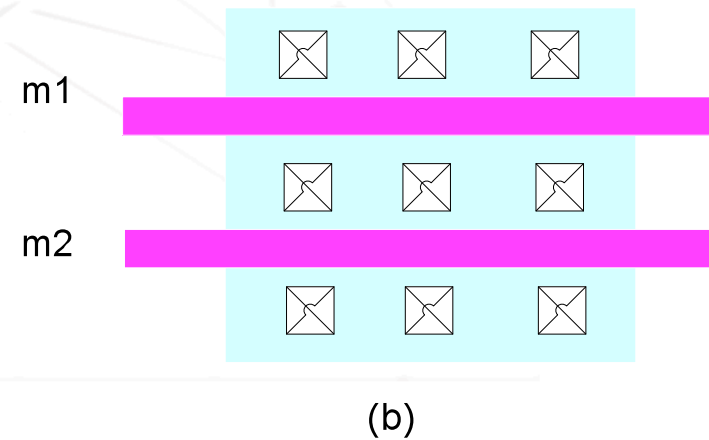
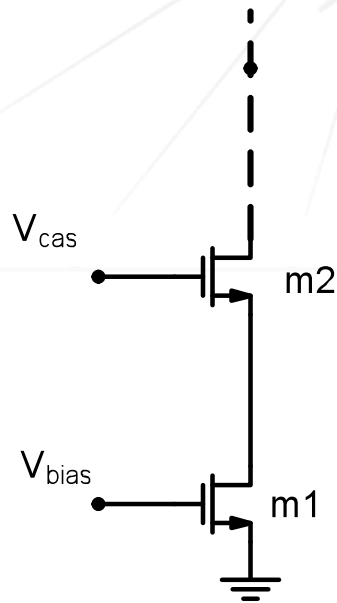


- Combing power from 4 unit amplifiers
- Centering at 2.4-GHz
- Output matching tuned by switched cap at back-off

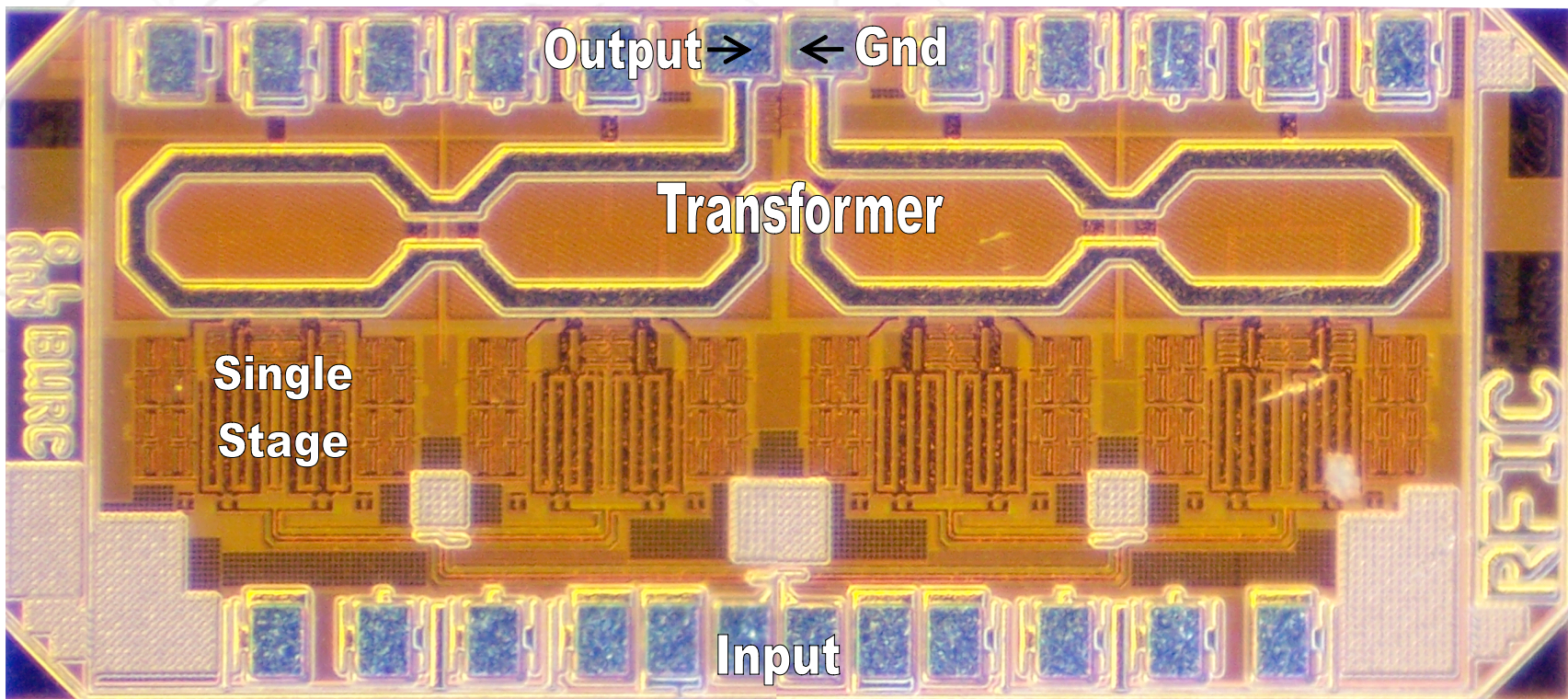
# Schematic of Each Unit Amplifier



# Cascode Layout

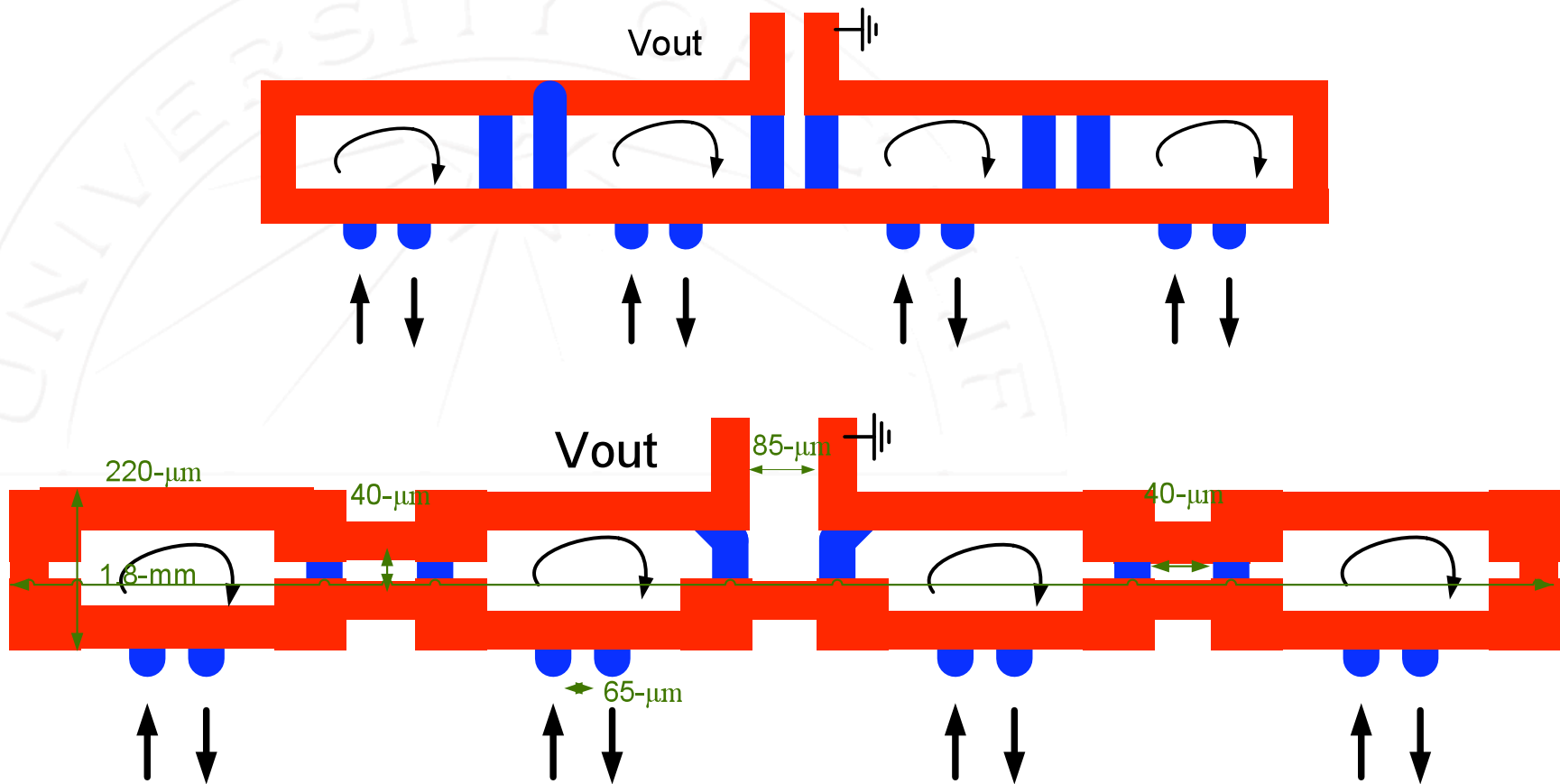


# Die Microphotograph

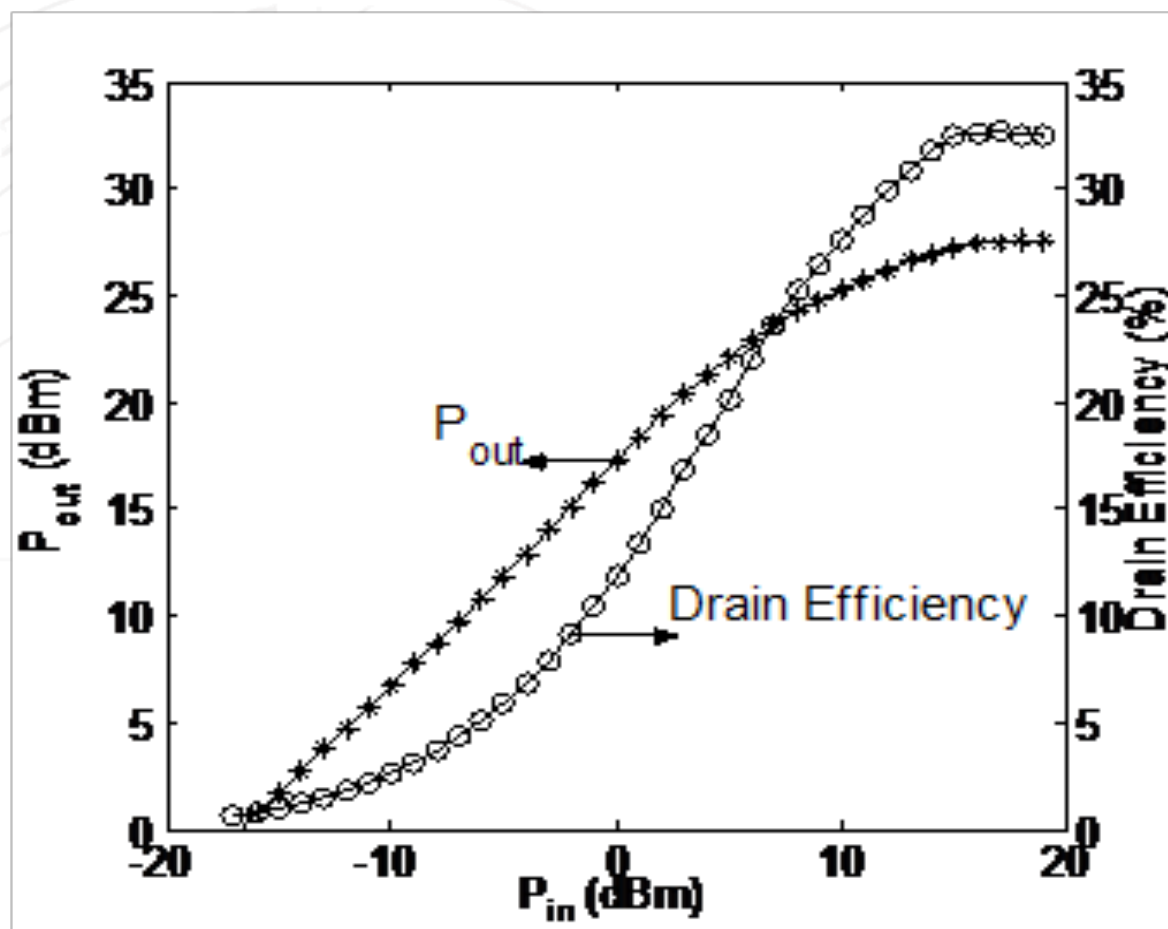




# Transformer & Cap Array

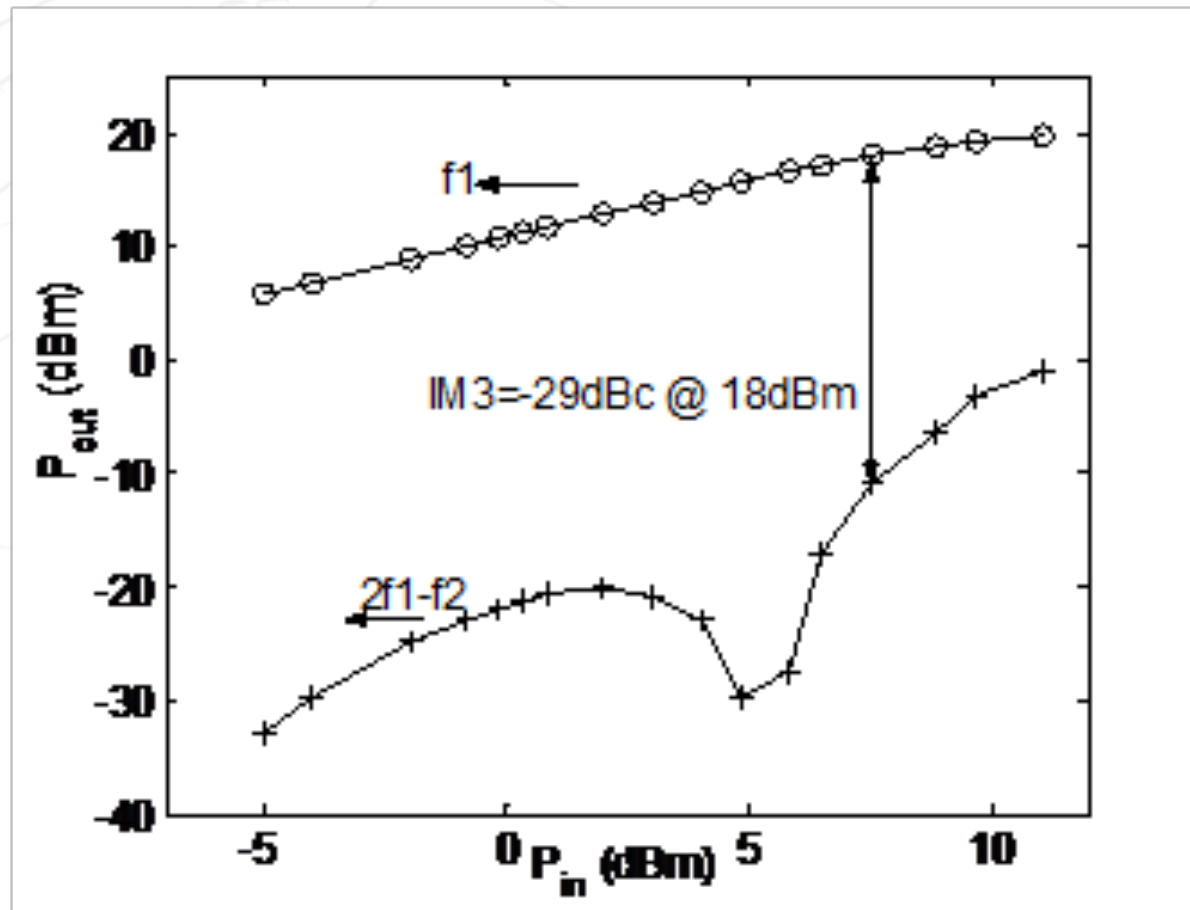


# Single-Tone Test



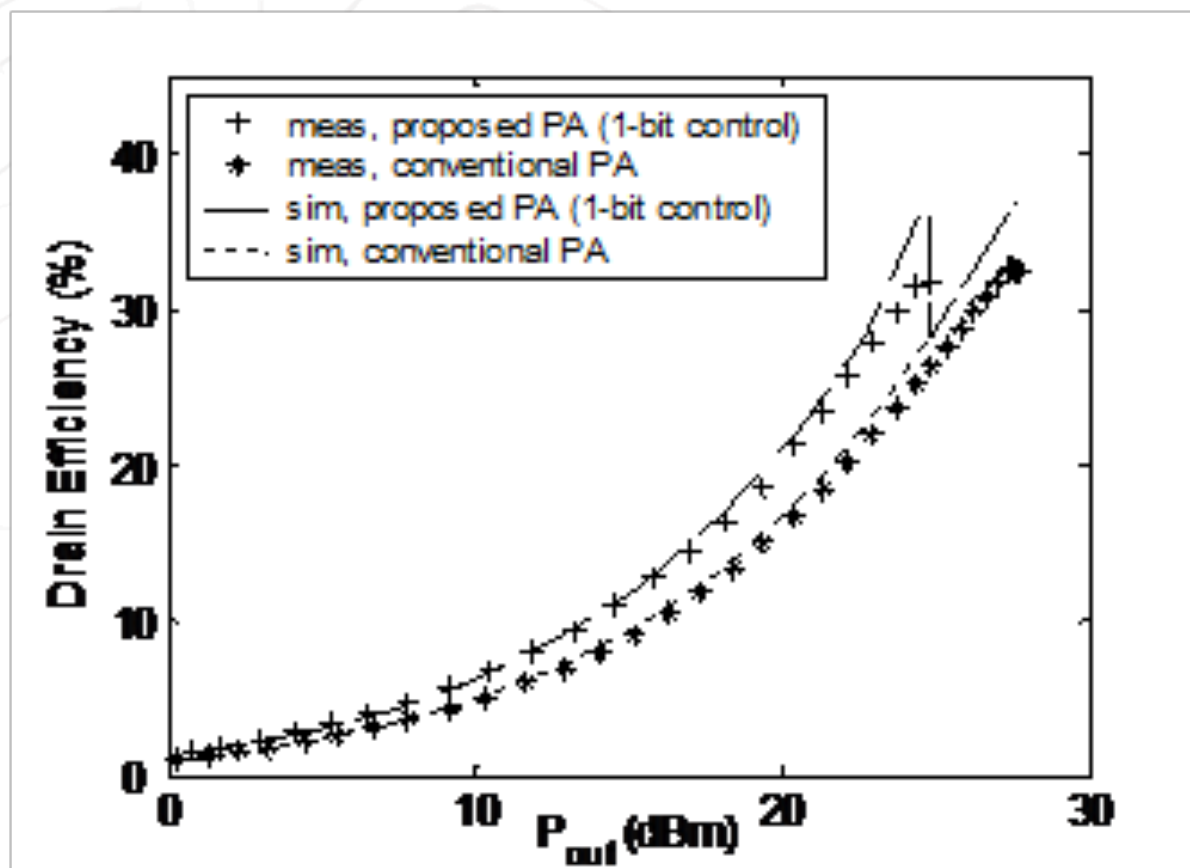
Freq = 2.4-GHz, Peak Power Mode

# Two-Tones Test



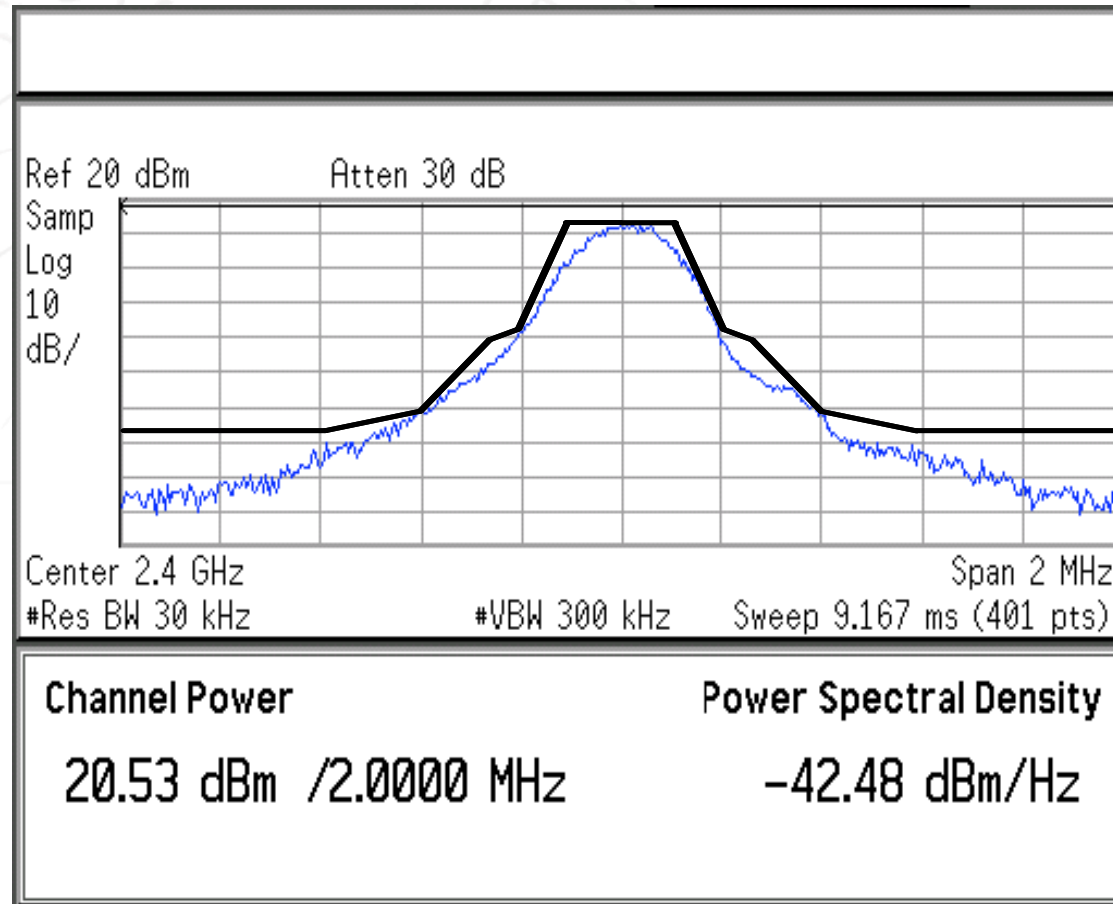
Freq = 2.4-GHz, 1-kHz tone spacing, Peak Power Mode

# Measured Efficiency at Back-Off



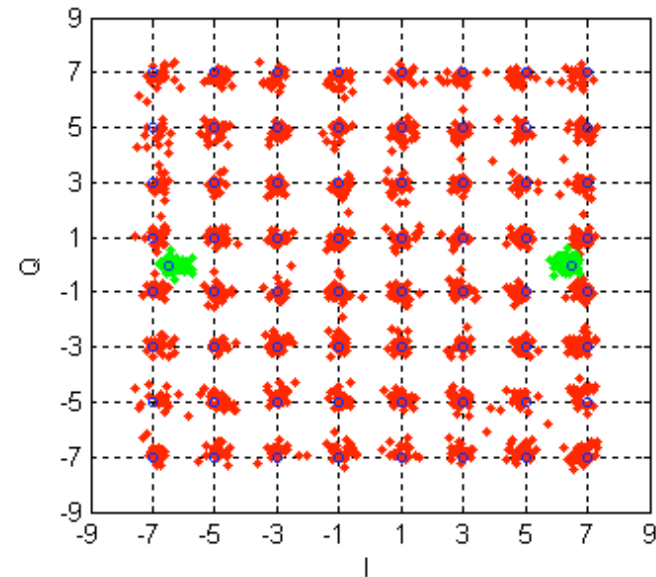
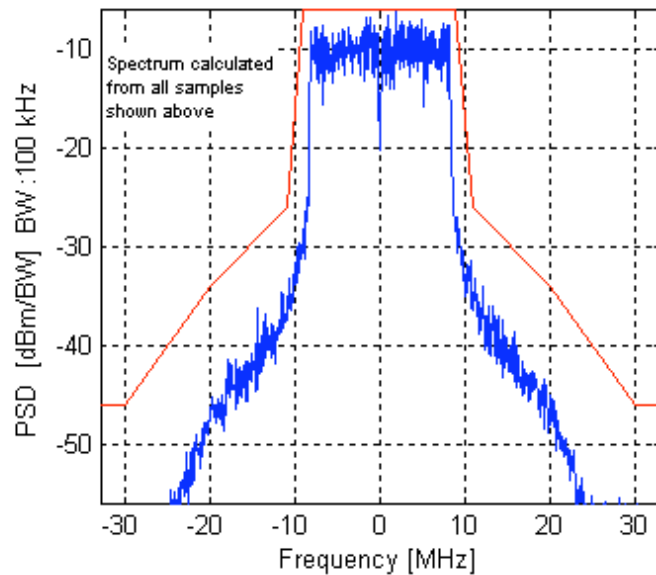
Note: at 2.5-dB back-off, one unit amplifier was turned off.

# Measurements with EDGE Signals



Freq = 2.4-GHz, Peak Power Mode

# Measurements with 802.11g Signals

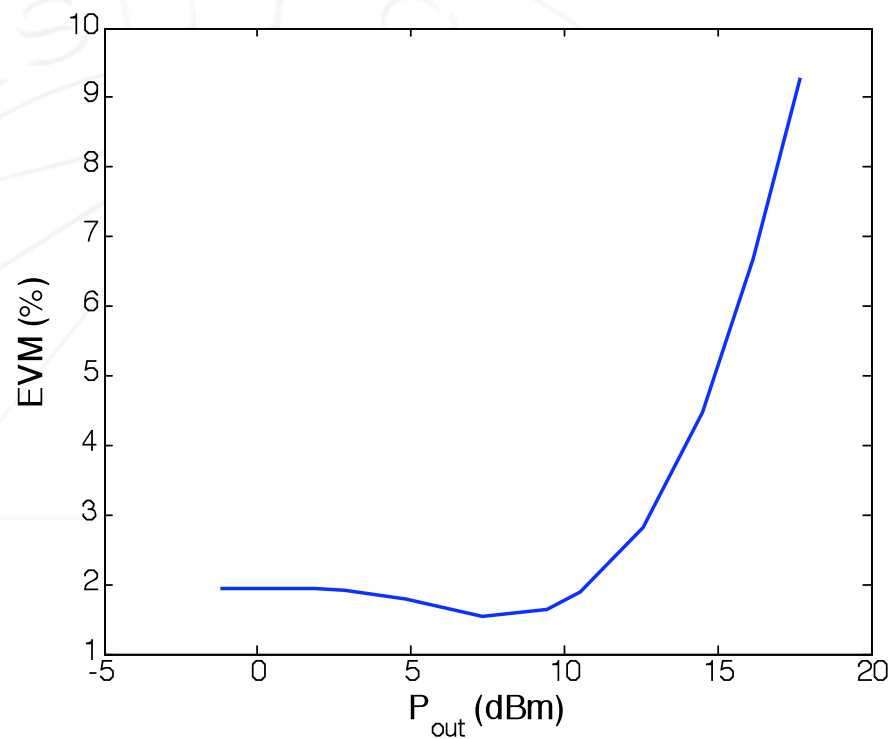


$$P_{\text{out}} = 14.5\text{-dBm} \quad \text{EVM} = 4.48\%$$

Freq = 2.4-GHz, Peak Power Mode

# EVM vs Output Power

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# Table of Performance

Technology	0.13- $\mu\text{m}$ RF CMOS
Supply voltage	1.2-V
DC Current	114-mA
$P_{-1\text{dB}}$	24-dBm
Drain efficiency	25%
Saturated Power	27-dBm
Drain efficiency	32%

UC Berkeley, EECS 242



# **A 5.8 GHz Linear Power Amplifier in a Standard 90nm CMOS Process using a 1V Power Supply**

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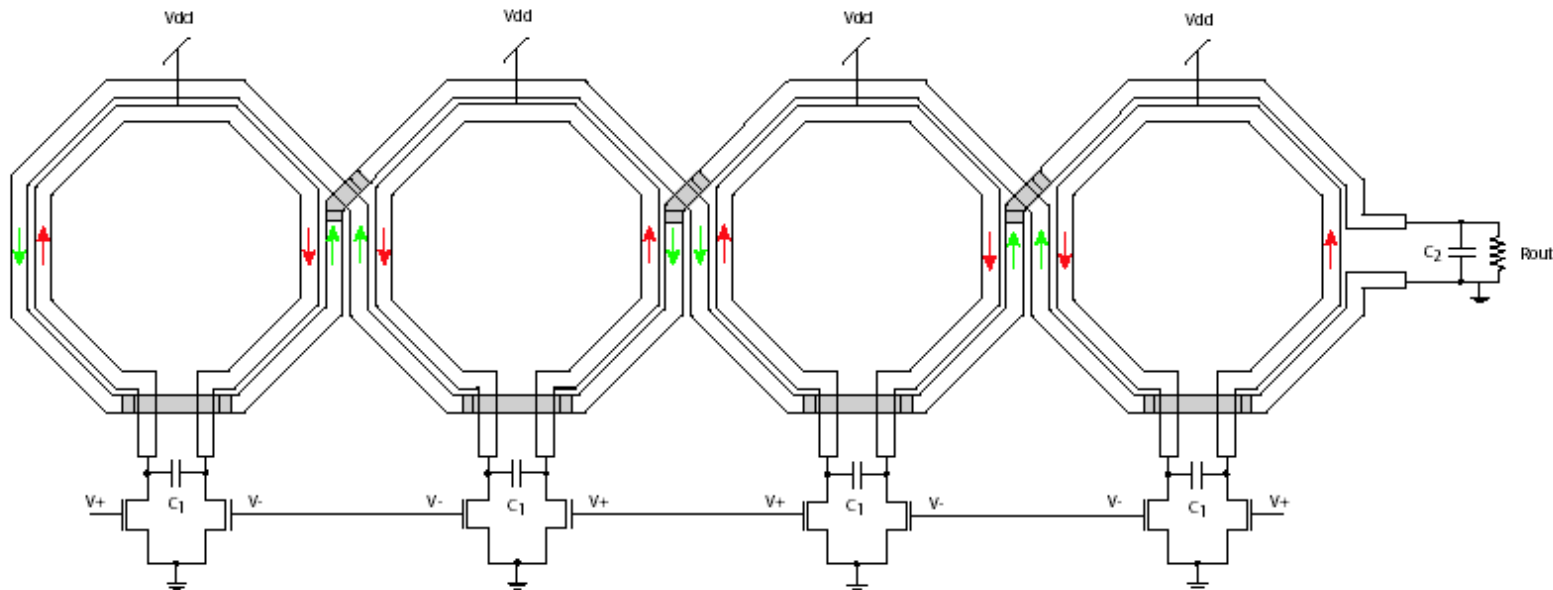
*RFIC 2007*

Peter Haldi, Debopriyo Chowdhury, Gang Liu and

Ali M. Niknejad

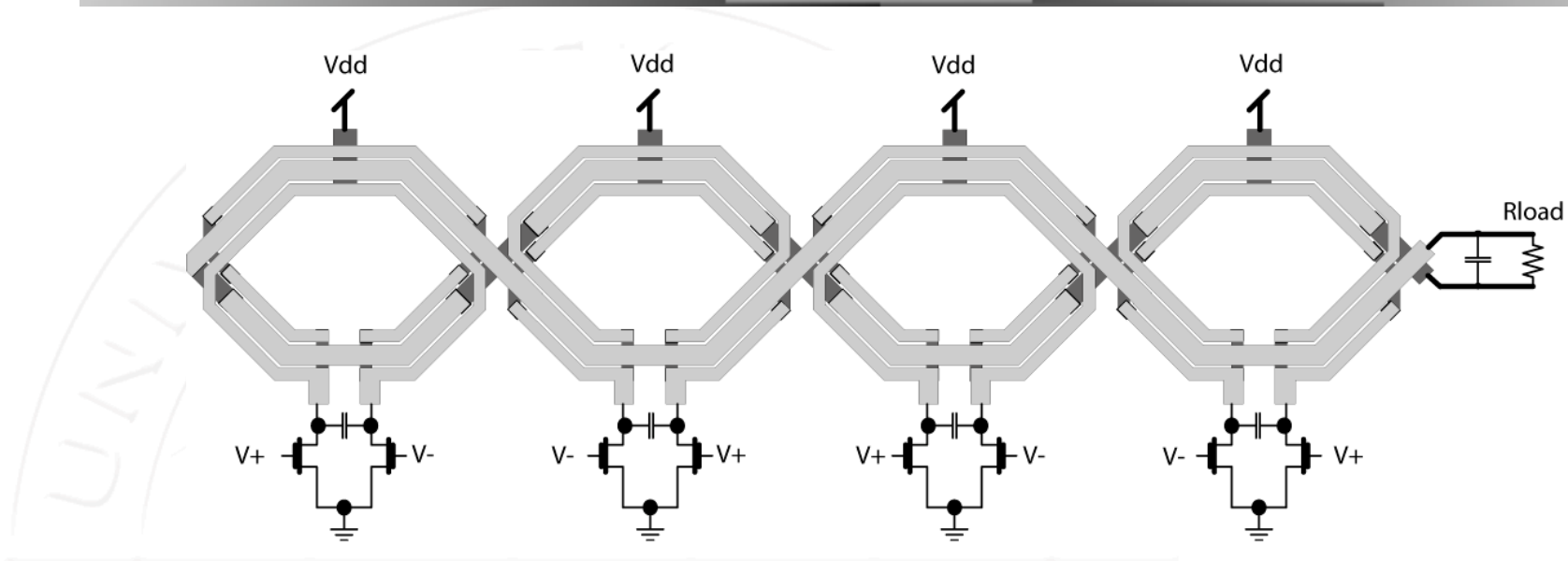
Berkeley Wireless Research Center, Dept. of EECS,  
UC Berkeley, Berkeley, CA 94704, USA

# New Transformer Network



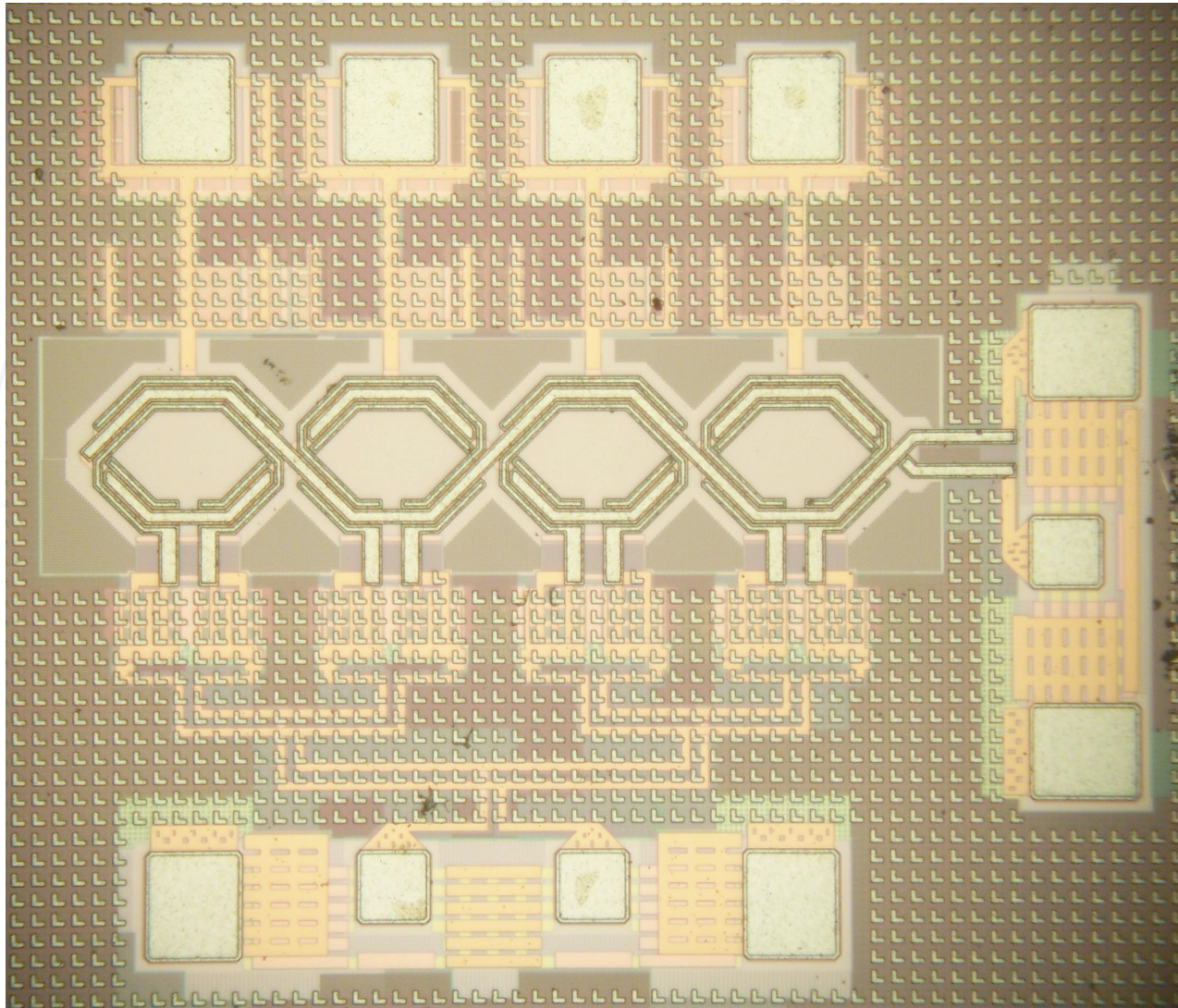
- Figure “8” style layout minimized the impact of lead inductance
- Lateral coupling used since top metal layer is most conductive and most distant from substrate
- Very good isolation characteristic due to flux inversion

# Improved Layout...



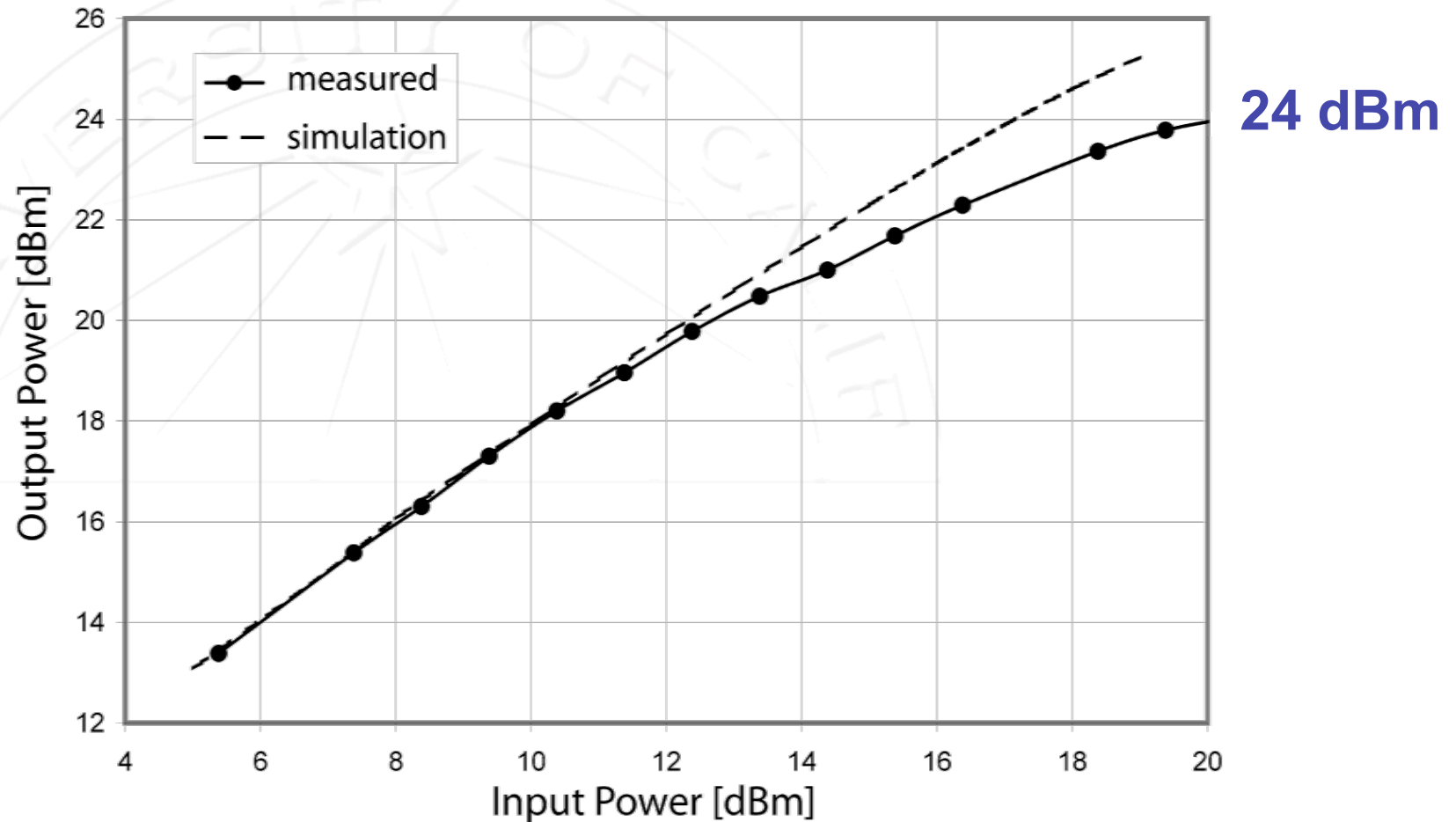
- Using two primary windings
  - Improved coupling
  - Lower loss (current crowding at edge of conductors)
  - More symmetric primary/secondary for optimal power transfer

# Prototype PA in Digital CMOS



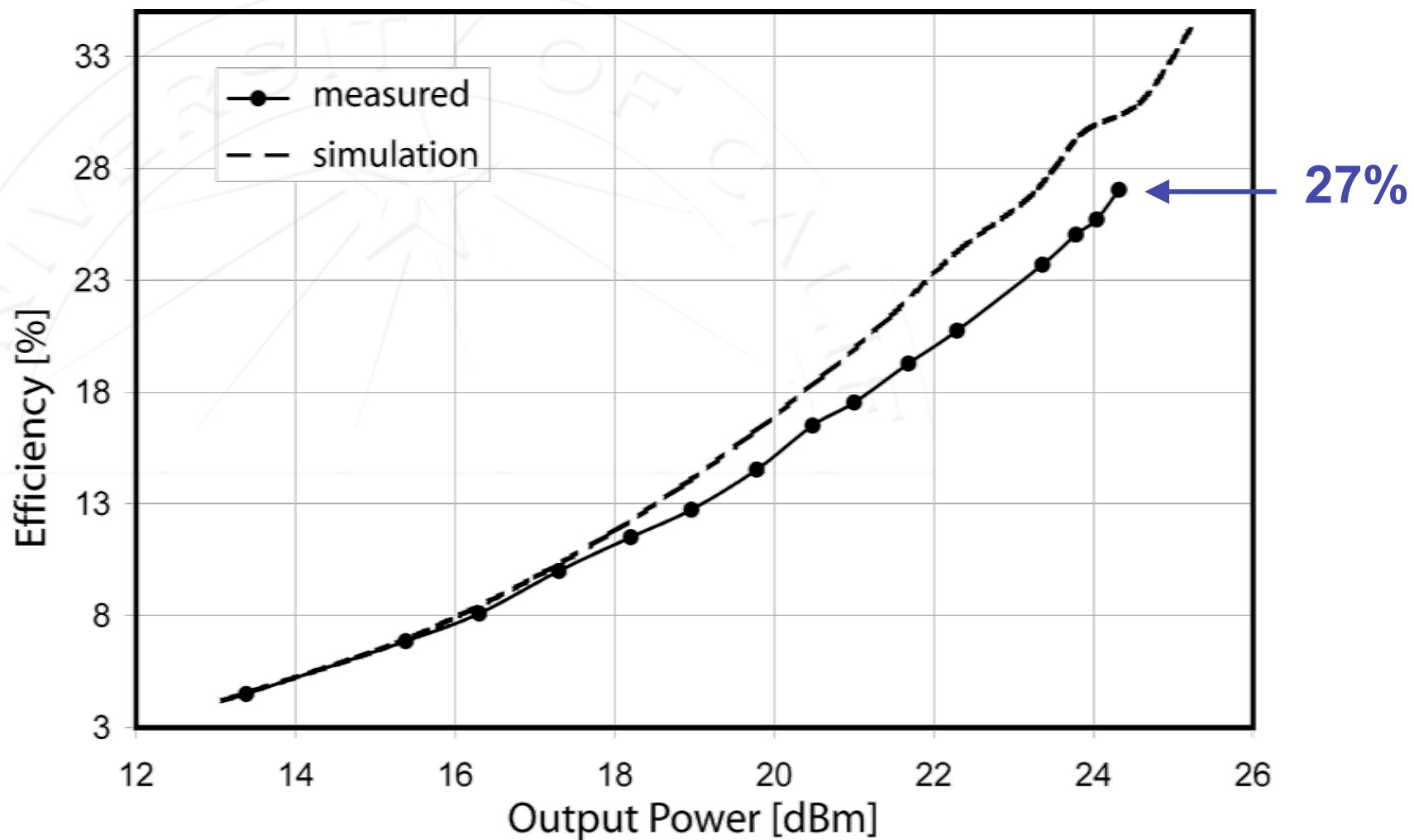
- Four stage differential design
- Single-ended 50Ω output
- Thin oxide 90nm transistors

# Measured Output Power

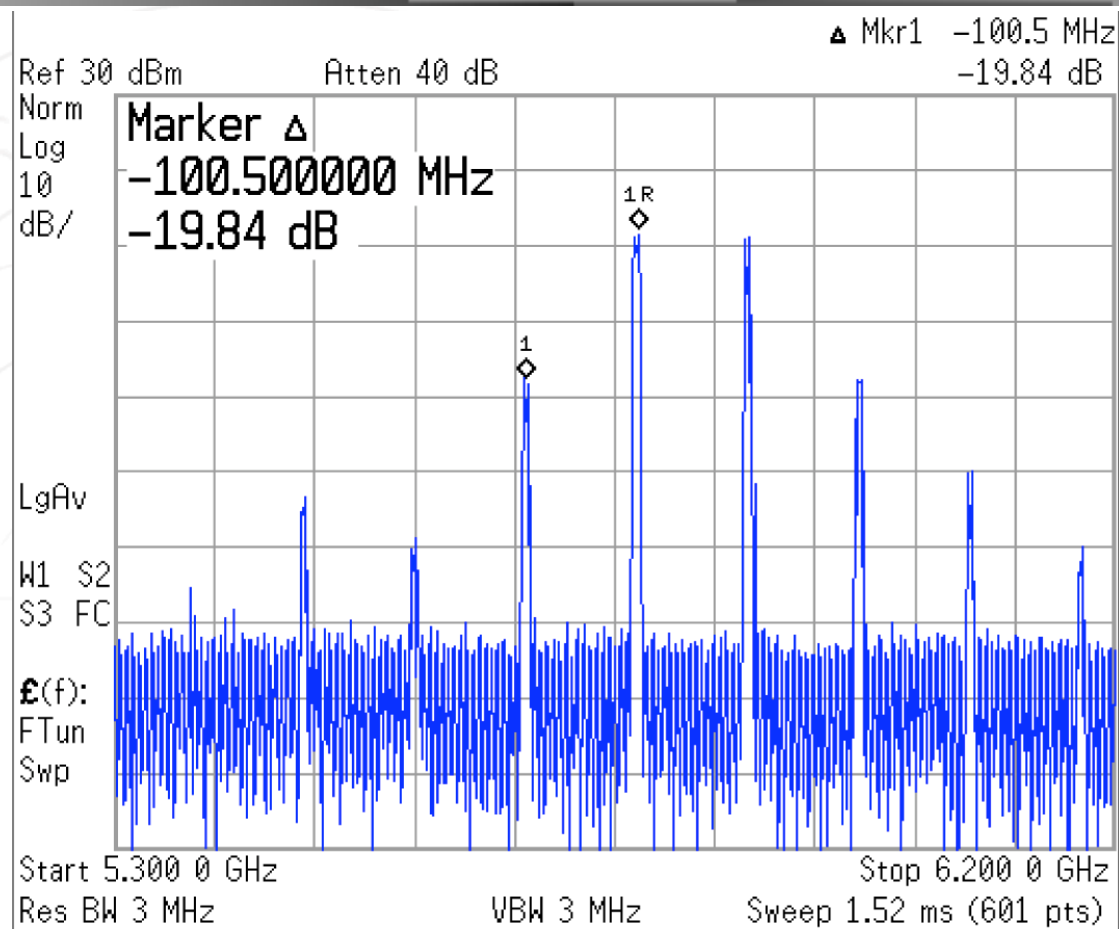


- Peak power is 24 dBm. Good match to simulation up to 1dB compression point.

# Measured Efficiency

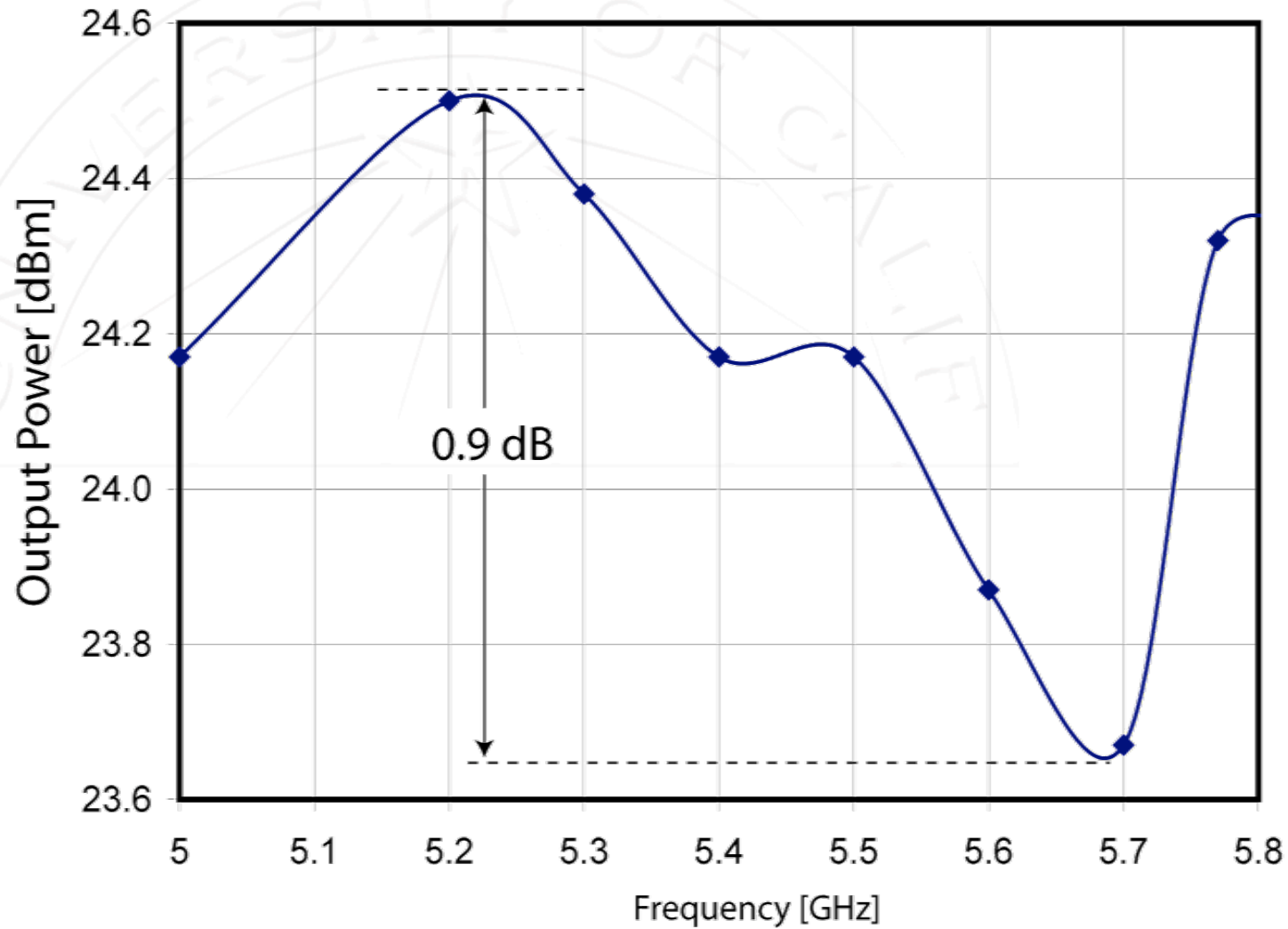


# PA Linearity



- IM3 = 28 dBc at output power of 20.5 dBm (200 MHz)
- IM3 has tone spacing dependence due to lack of good bypass (class AB stage). Verified with packaged version.

# Output Power vs Frequency





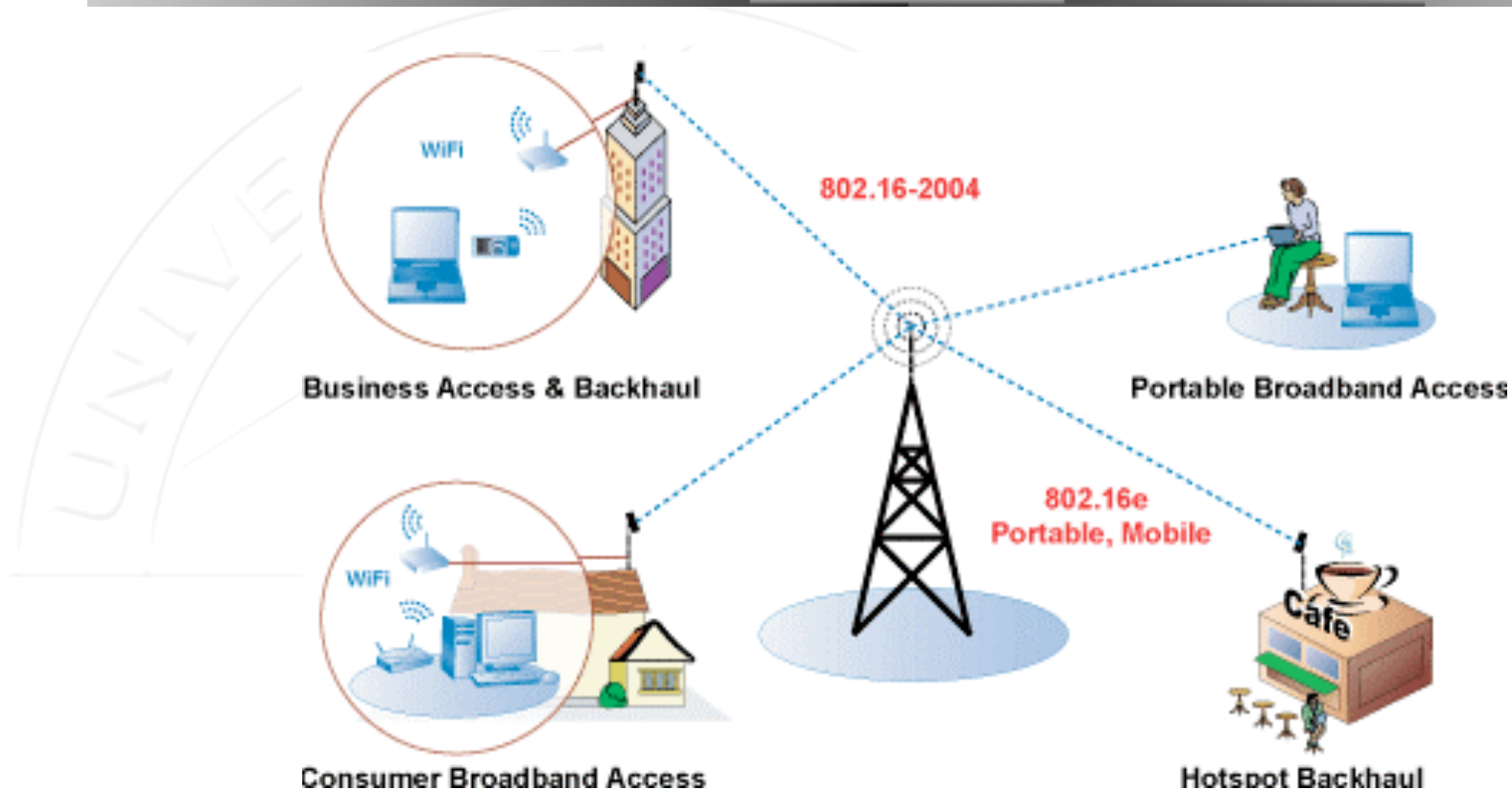
# CMOS “digital” Prototype

Process	Freq.	$V_{dd}$	$P_{1dB}$	IM3	Gain	$\eta$	Ref.	Notes
0.35 $\mu$ m CMOS	1.91 GHz	2.5V	23.5dBm		24.6 dB	35.3%	[19]	with driver, ext. RF chokes
0.5 $\mu$ m SiGe BiCMOS	1.75 GHz	3.3V	24dBm	37 dBc	23.9dB	29.2%	[20]	with driver, linearized
0.18 $\mu$ m standard CMOS	2.4 GHz	3.3V	24.5dBm		19.8 dB	31.3%	[9]	with driver
0.13 $\mu$ m CMOS	2.4 GHz	1.2V	24dBm	29dBc	10 dB	25%	[8]	
0.09 $\mu$ m CMOS	5.2-5.8 GHz	1V	23.3dBm	30.5dBc	13.8 dB	26%	this work	simulated results

Table 5.3: Comparison between state of the art linear power amplifiers.

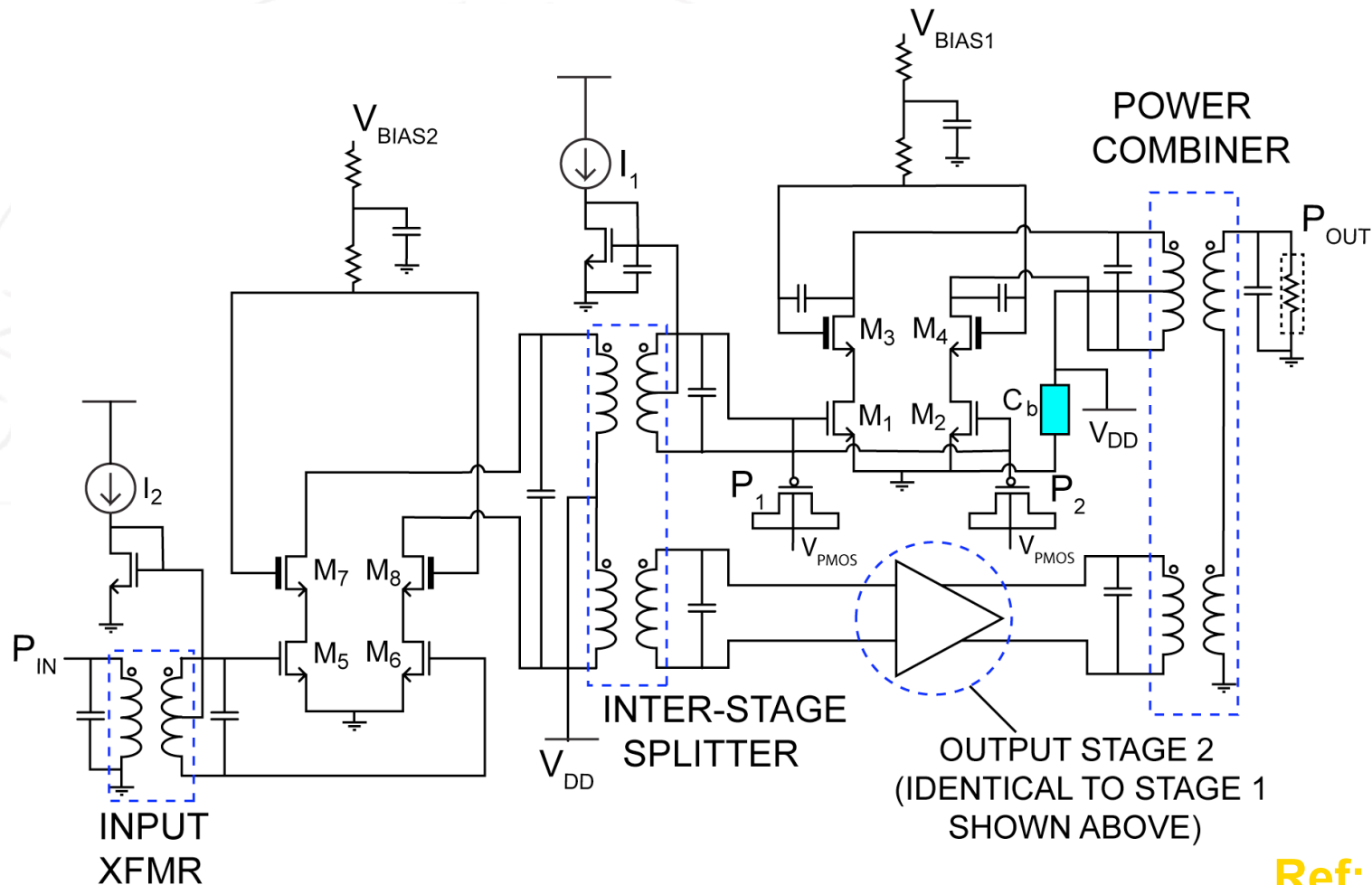
- New transformer layout has simulated efficiency of 75%
- State-of-the-art performance of 5 GHz linear PA
  - 24 dBm with 27% efficiency

# 4G Wireless Communication



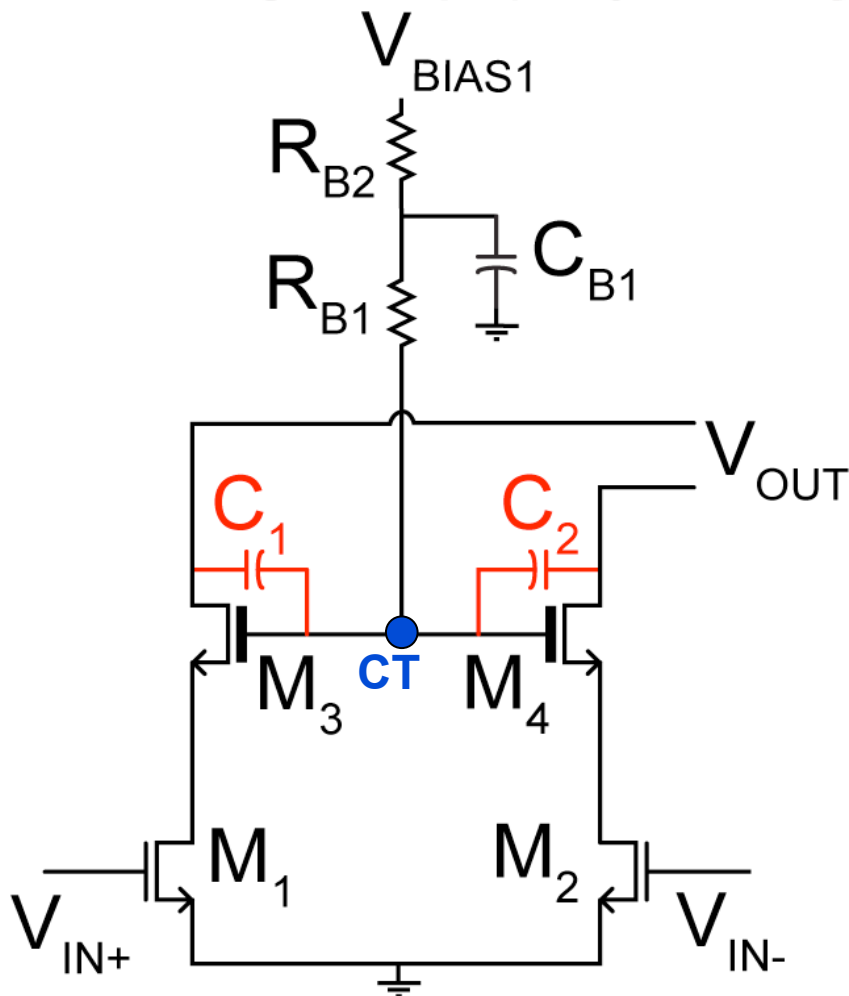
- IEEE 802.16 standard (Wireless MAN)
- Wireless data over long distances in a variety of ways

# Two-Stage WiMAX CMOS PA



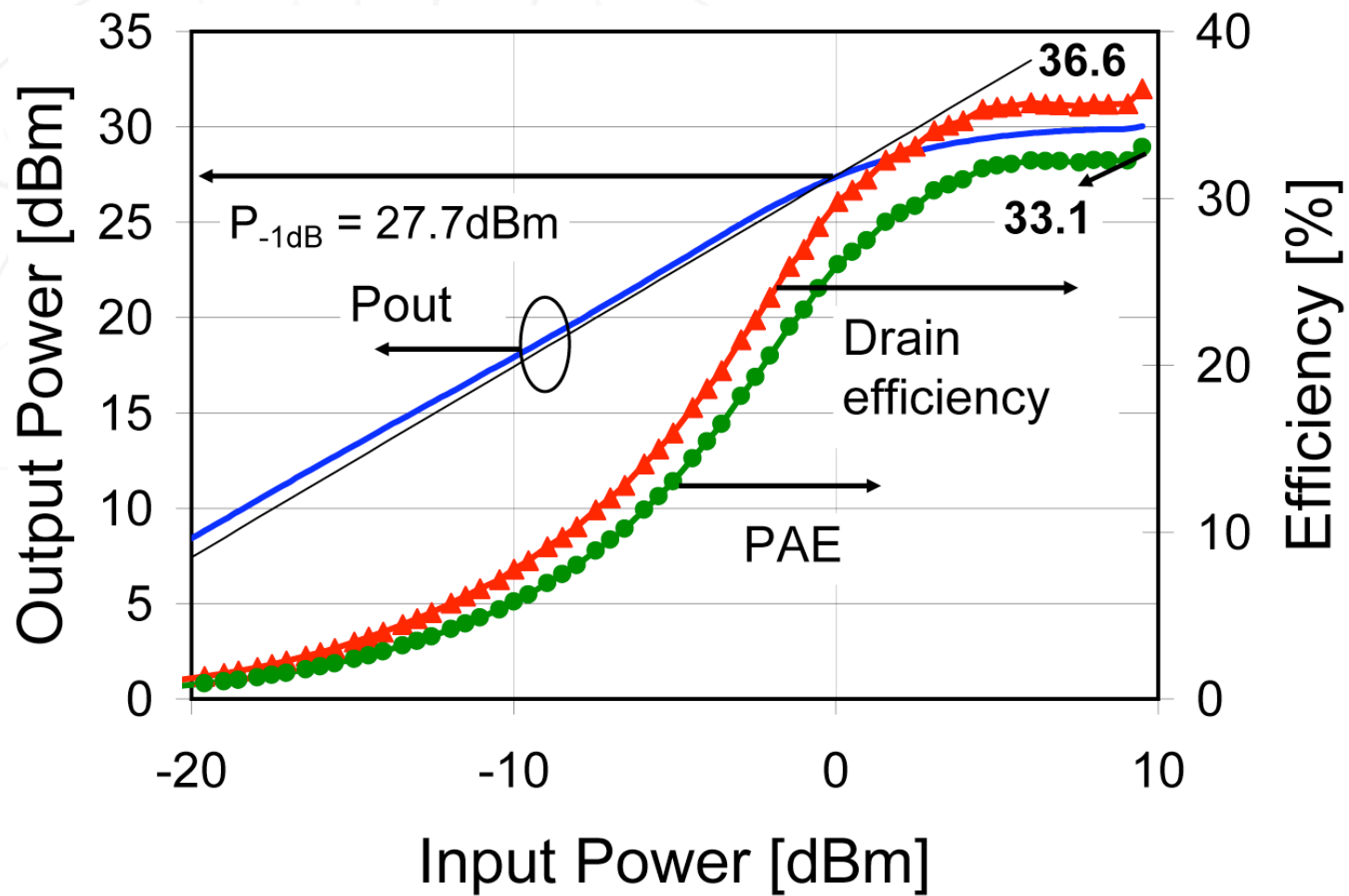
Ref: [Chow2]

# Output Stage Design

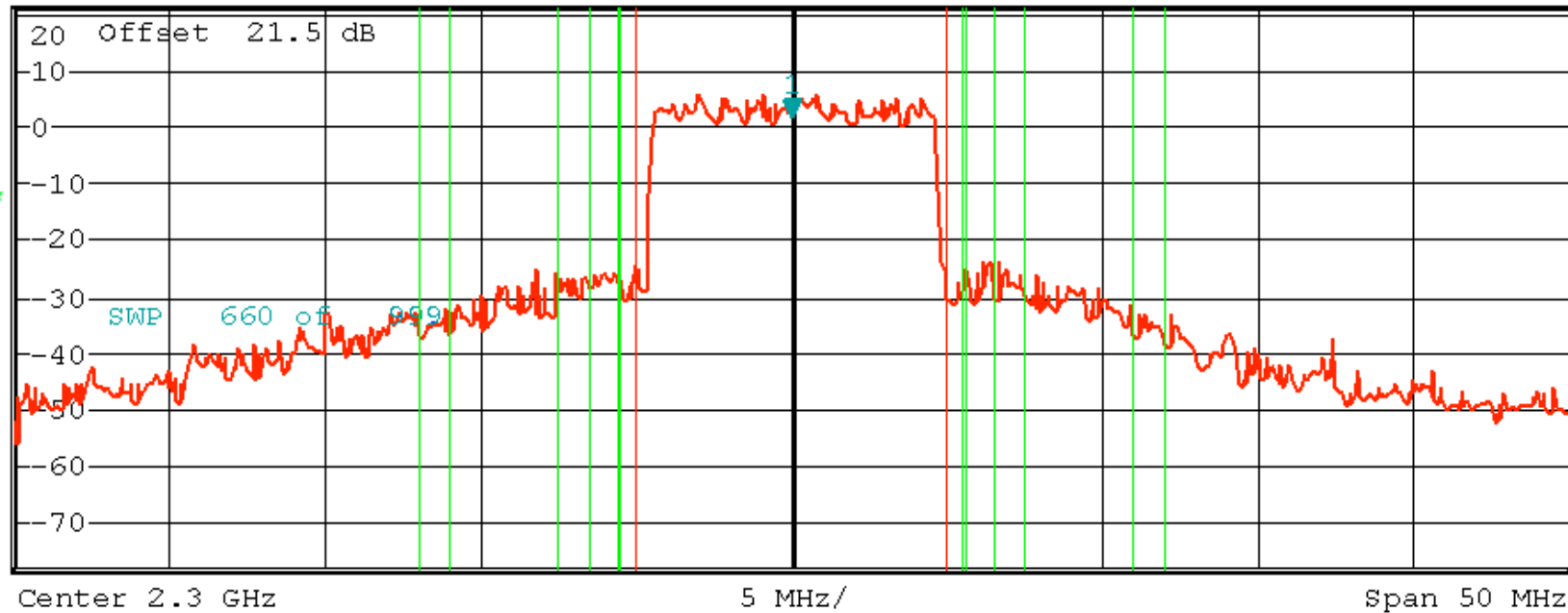


- Thick-oxide CG stage ( $V_{DD} = 3.3V$ )
- Dynamic gate biasing
- Capacitive divider
- Differential  $\rightarrow$  does not affect small signal gain

# Large-Signal CW Measurements

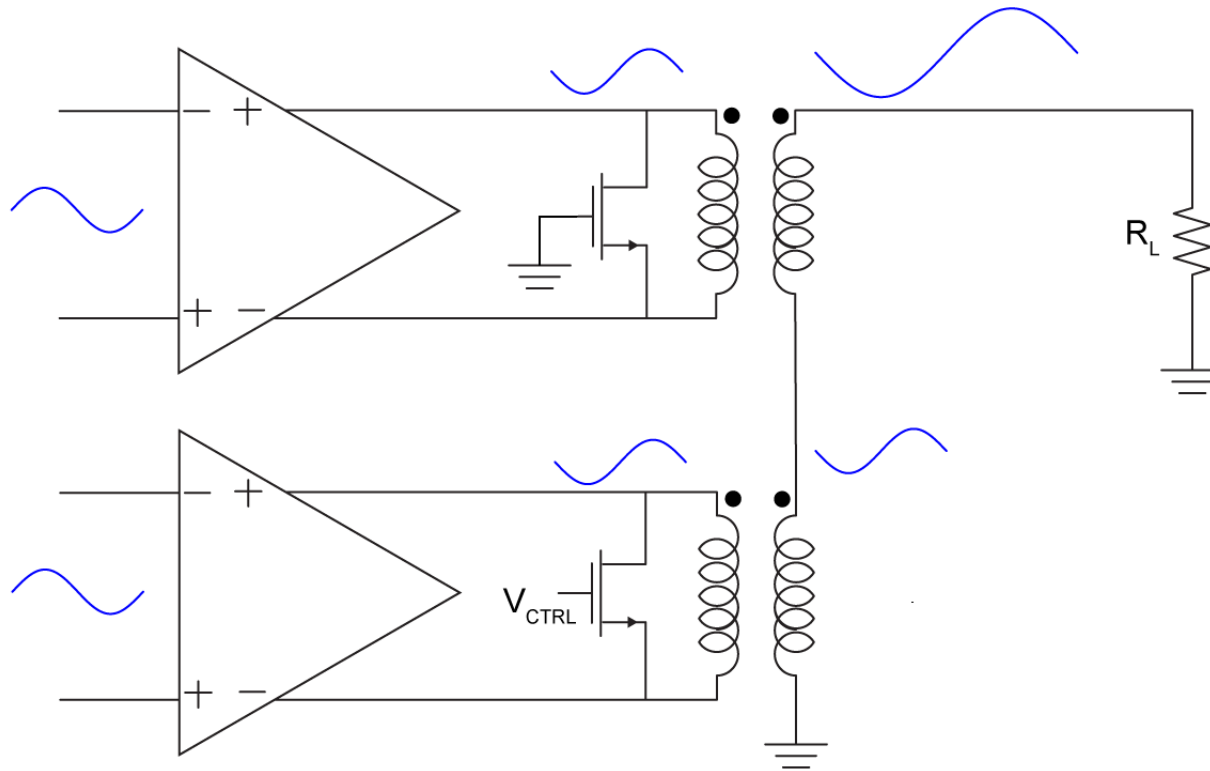


# Meeting the WiMAX Mask



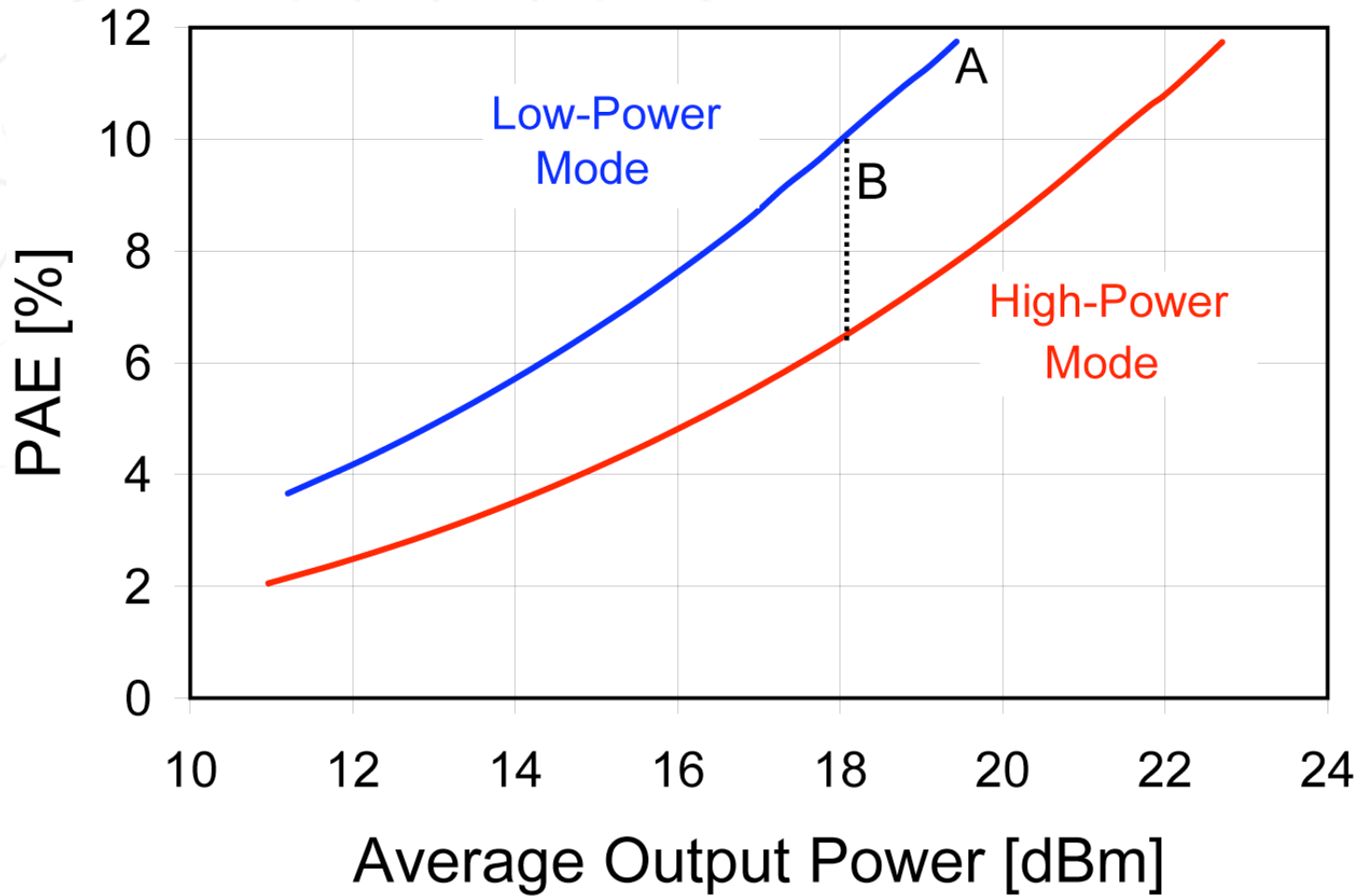
- Average Pout = 22.76 dBm
- Average drain efficiency = 15%, Average PAE = 12%
- Power of 2nd, 3rd and higher harmonics also meet FCC mask → possible to eliminate harmonic filter

# Back-Off Mode Implementation



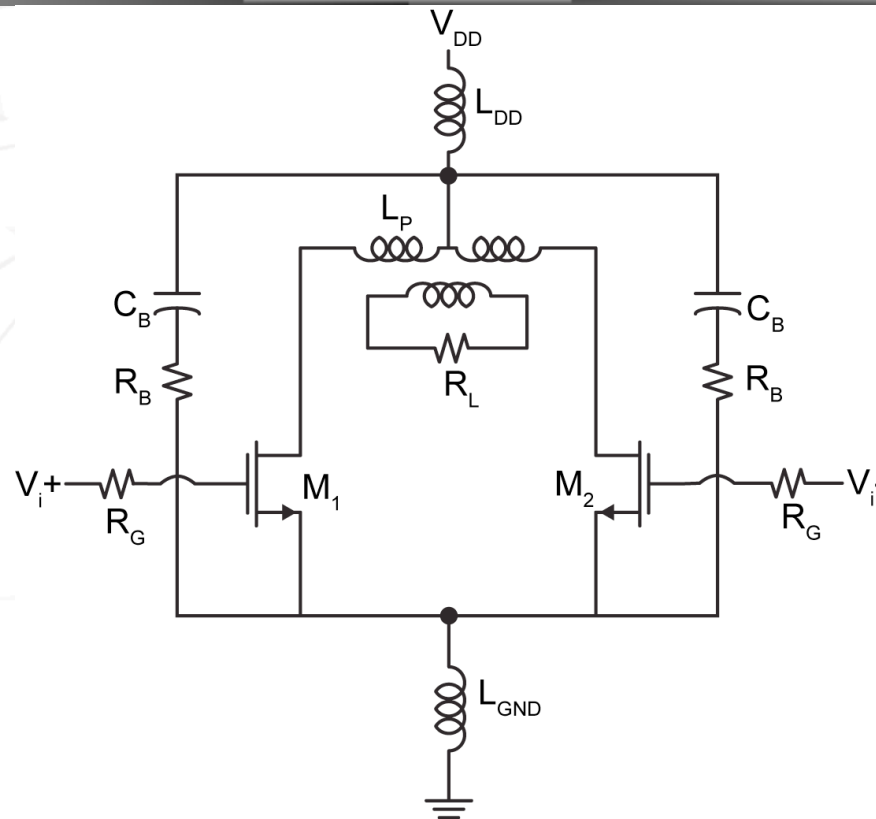
- Bottom stage powered-down for low-power mode
- $V_{ctrl}=0$  in high-power mode and  $2*V_{DD}$  in low-power mode

# Low Power Mode



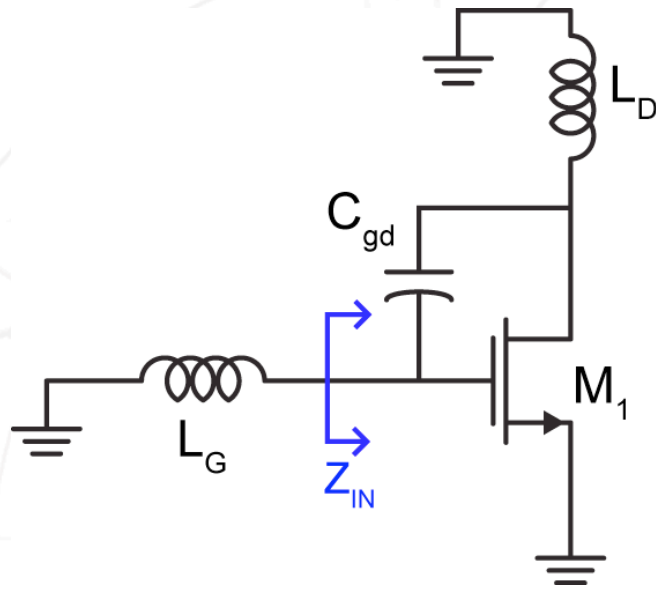


# Common-Mode Stability



- Pseudo-differential architecture  $\rightarrow$  common-mode oscillations possible
- Need to consider ground & supply inductances, bypass network

# A Simpler Structure



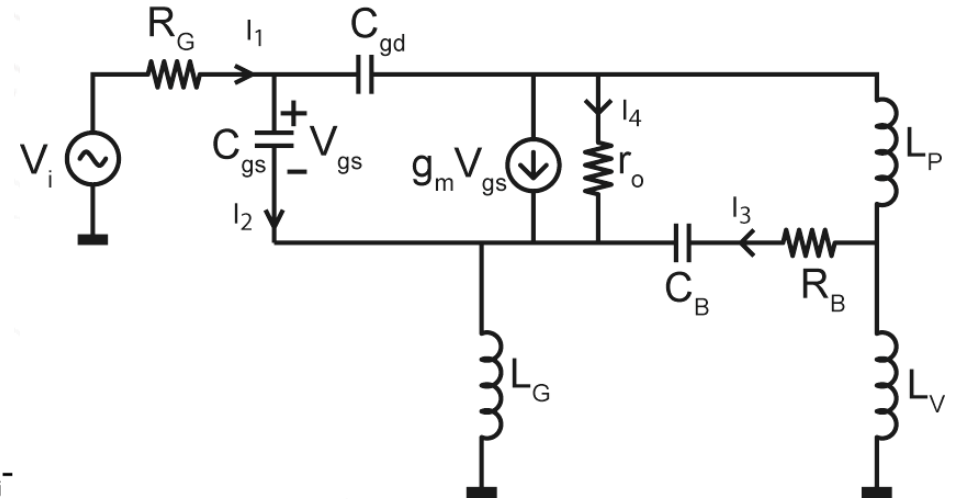
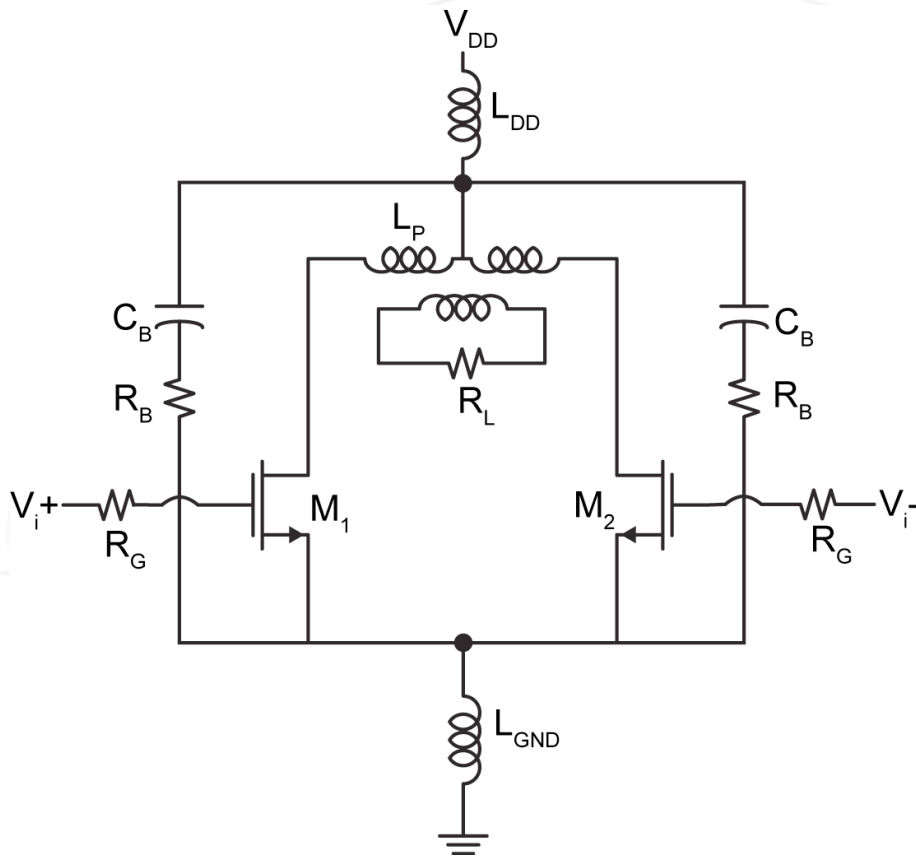
$$Z_{IN} = \frac{j(\omega L - \frac{1}{\omega C_{gd}})}{1 + j\omega g_m L_D}$$

- If  $(1/\omega C_{gd}) \gg (\omega * L)$ ,

$$Z_{IN} = \frac{1}{(1 + \omega g_m L_D)^2} \left[ \frac{1}{j\omega C_{gd}} - \frac{g_m L_D}{C_{gd}} \right]$$

Ref: [Cripps]

# Stability Analysis



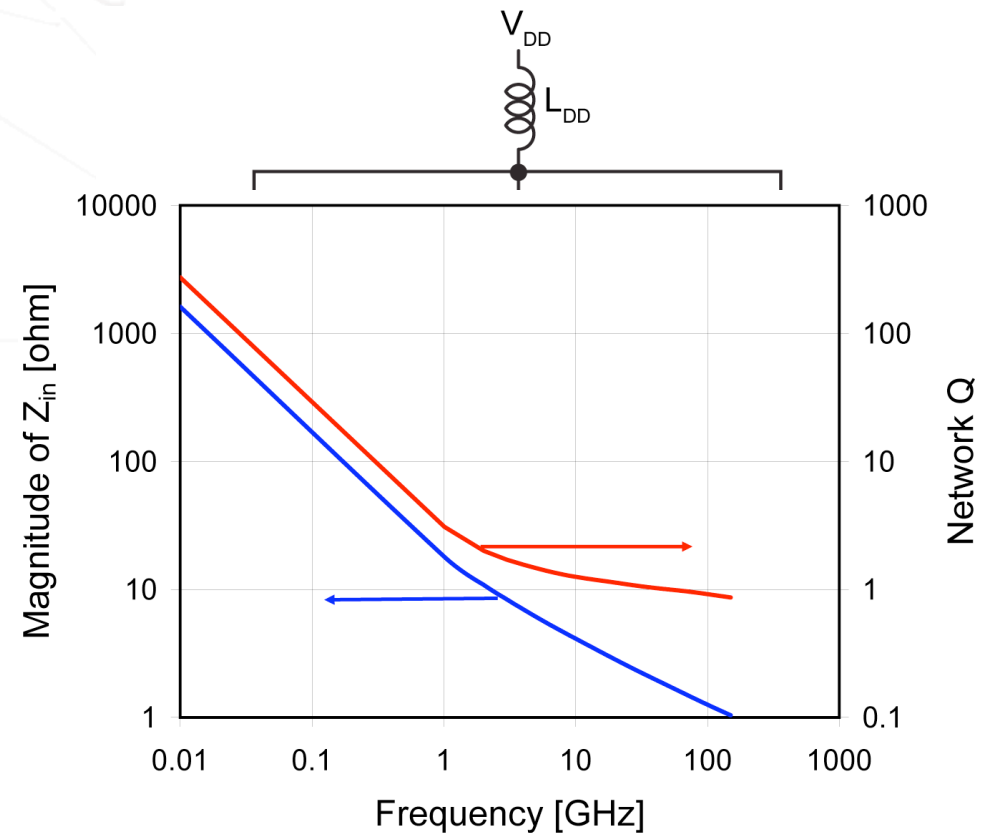
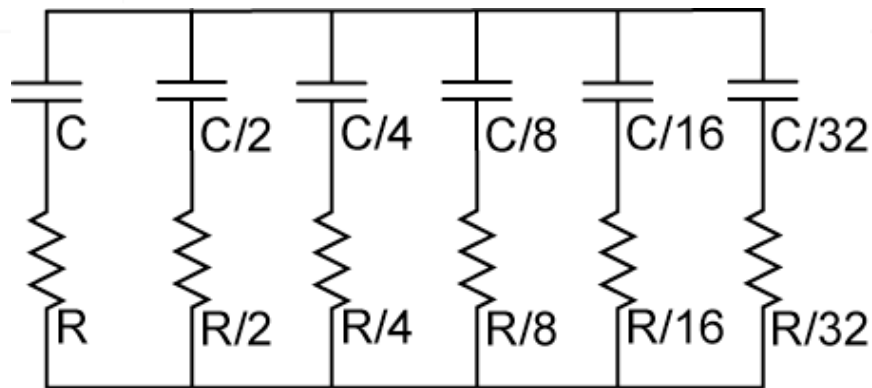
$$\begin{bmatrix} V_i \\ 0 \\ V_i \\ V_i \\ 0 \end{bmatrix} = [A] \times \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ V_{gs} \\ I_4 \end{bmatrix}$$

- For oscillation, [A] is singular

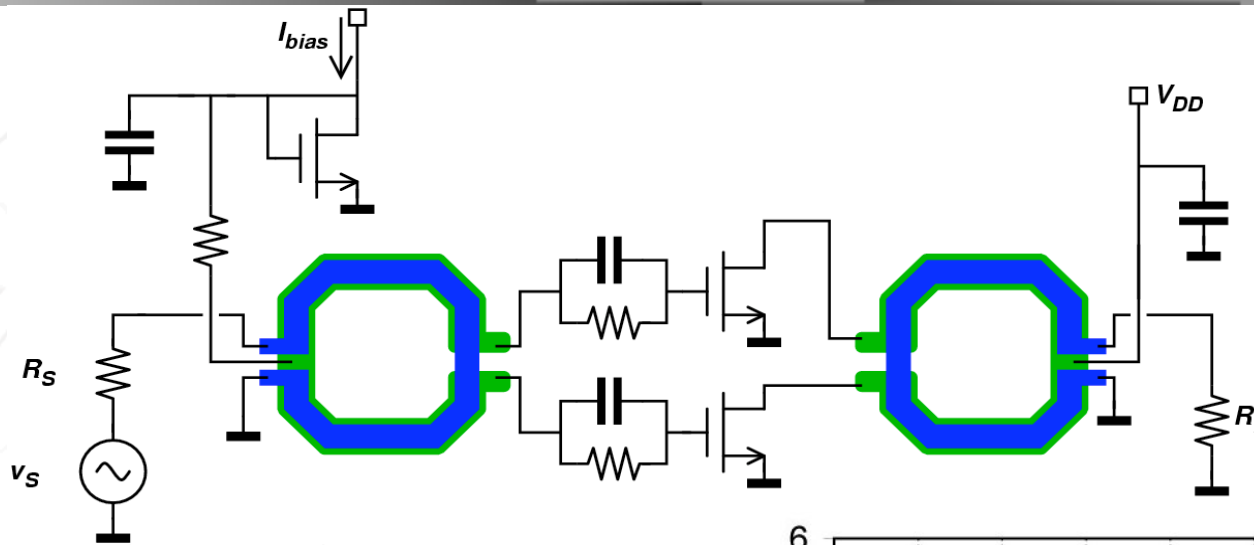
Ref: [Chow3]

# Stabilizing the PA

- Resistor in series with gate
- Resistor in series with bypass capacitor
- Staggered-RC bypass network
- Series RC-pair



# Series RC Pair



- Transistors have higher gain at lower frequency, transformers are wideband
- RC network  $\rightarrow$  loss around 35GHz without impacting 60GHz

Ref: [Kom]

