

EECS 242: Amplifier Design Examples

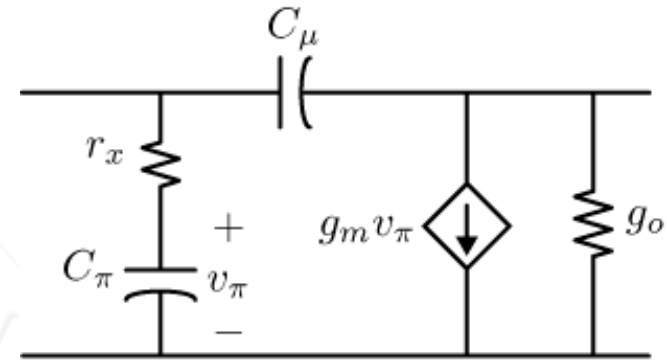
Professor Ali M Niknejad
Advanced Communication Integrated Circuits

University of California, Berkeley



Small-Signal Transistor Model

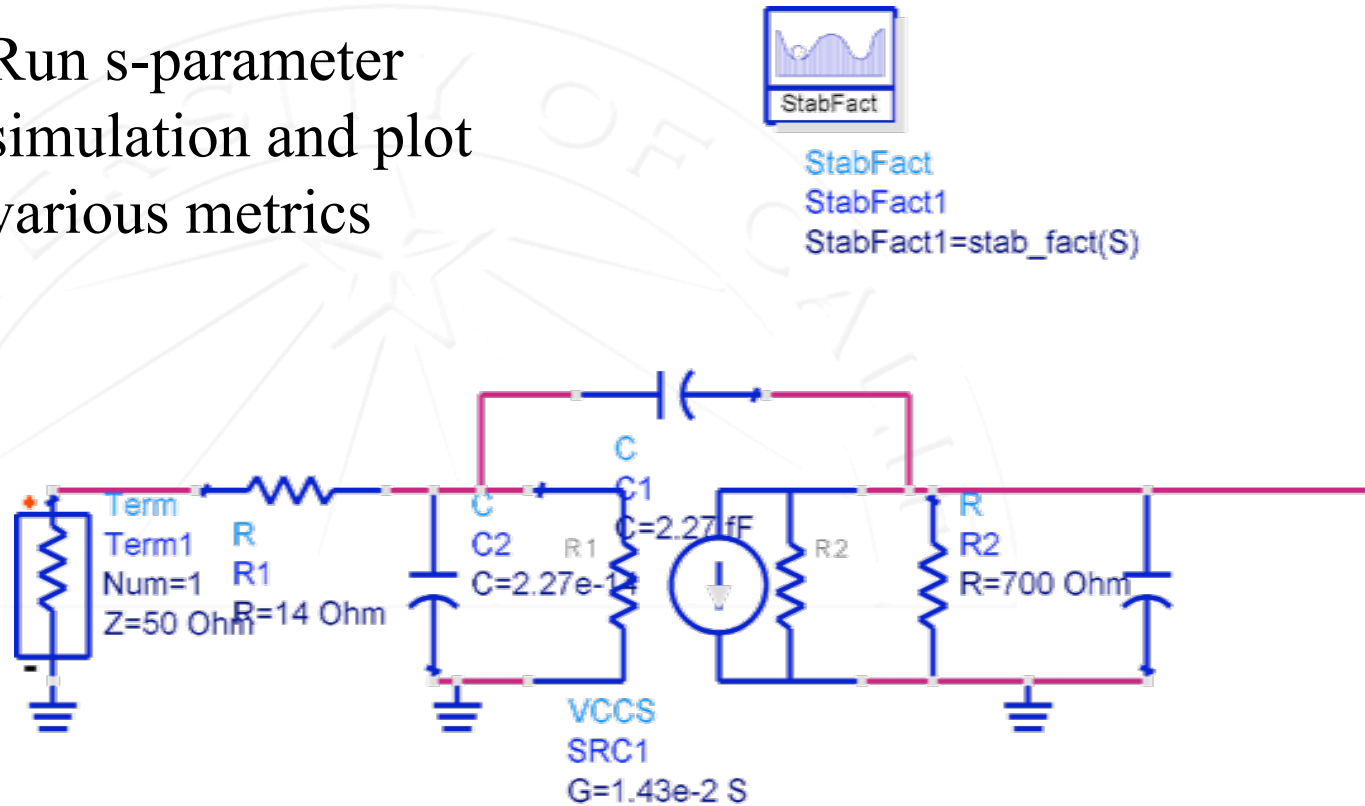
$$\omega_T = \frac{g_m}{C_{gs}} \quad g_m = \frac{2I_{ds}}{V_{dsat}}$$
$$C_{gd} = \mu C_{gs} \quad A_{v,0} = g_m r_o$$
$$r_x = \frac{1}{5g_m}$$



- Intrinsic transistor model
- Using basic equations, let's assume we have the following process:
 - $f_T = 100$ GHz
 - $A_{v0} = 10$, $V_t = 0.3$ V, $V_{gs} = V_{dd} = 1$ V, $V_{dsat} = 0.7$ V, $I_{ds} = 5$ mA
 - $g_m = 14.3$ mA/V, $r_o = 700$ Ω , $C_{gs} = 22.7$ fF
 - $C_{gd} = 0.1 C_{gs} = 2.27$ fF
 - $C_{db} = 10$ fF (arbitrary)

Simulation Setup (ADS)

- Run s-parameter simulation and plot various metrics



StabFact
StabFact1
StabFact1=stab_fact(S)



GaCircle
GaCircle1
GaCircle1=ga_circle(S,2,51)

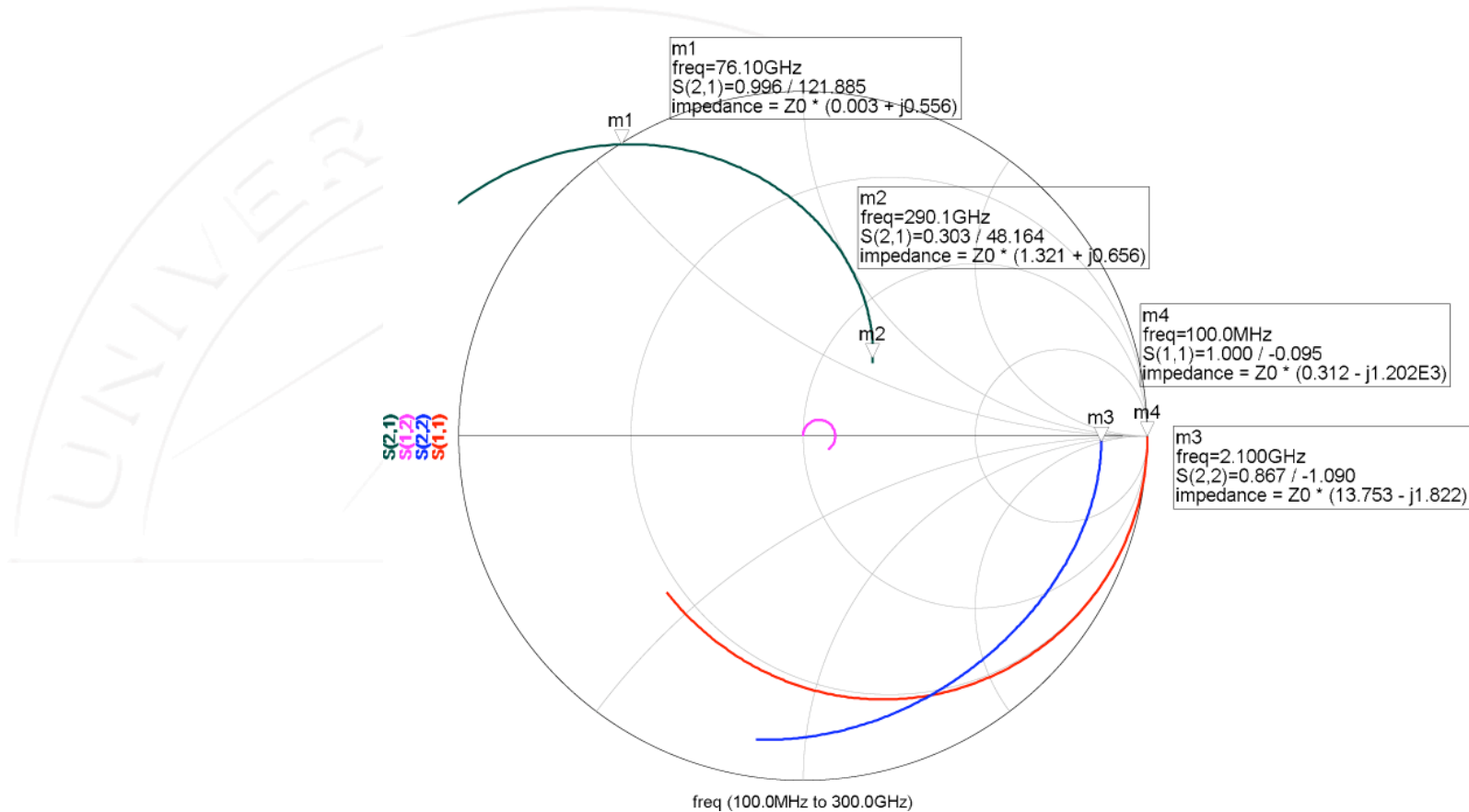


GpCircle
GpCircle1
GpCircle1=gp_circle(S)



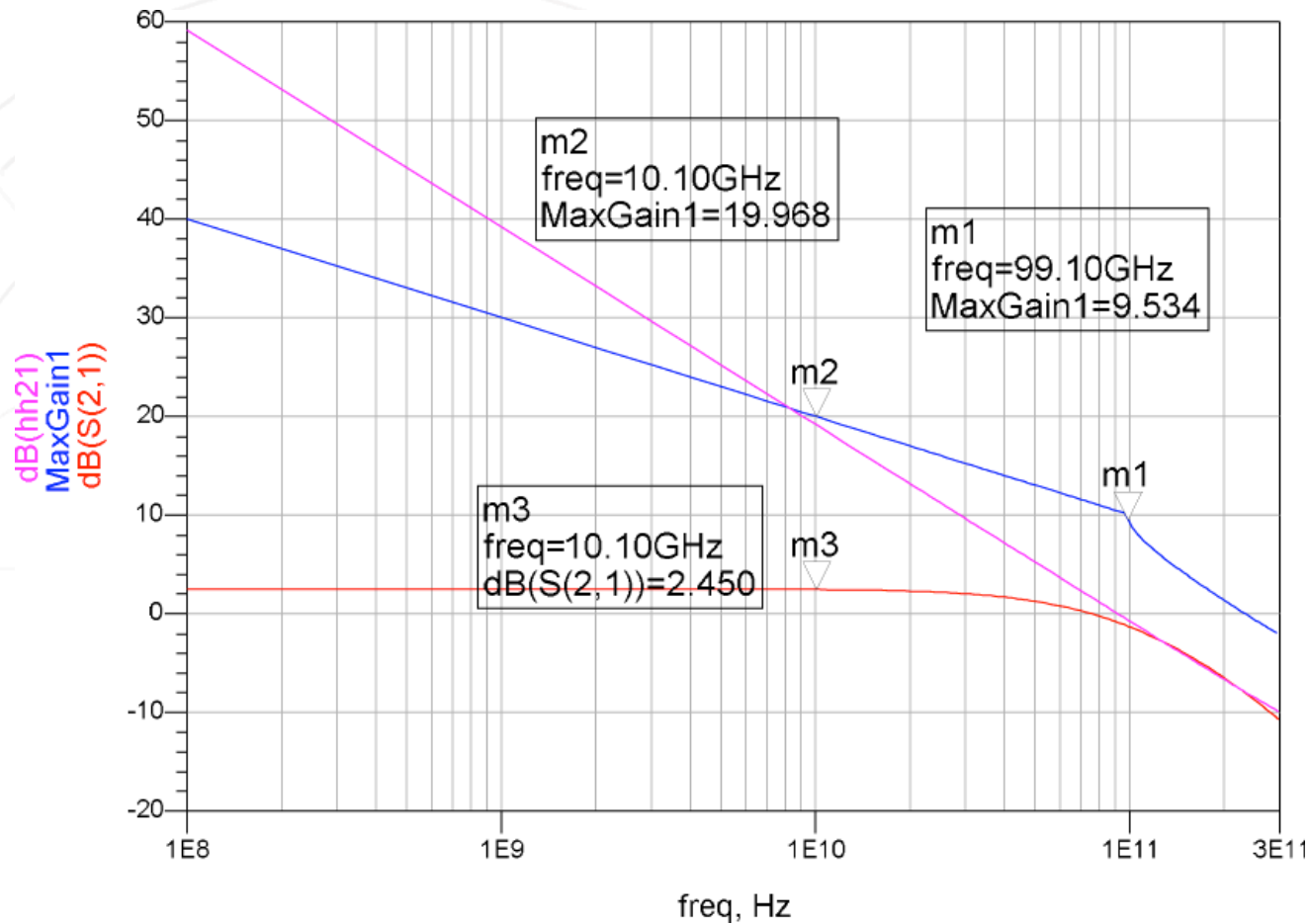
S_StabCircle
S_StabCircle
S_StabCircle

S-Parameter Simulations



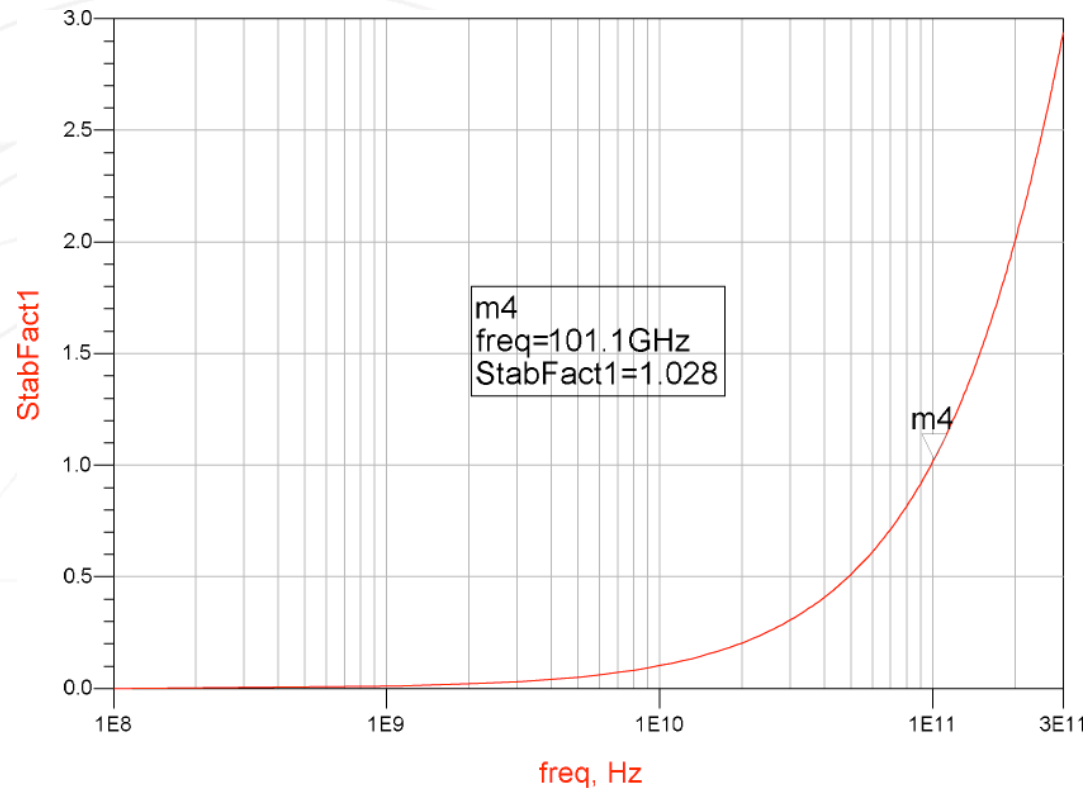
- Note $|S_{21}| < 1$ above 76 GHz, $|S_{12}|$ is relatively small
- At low frequency, S11 and S22 dominated by capacitance

Maximum Gain Plots



- $F_{max} > F_t$ ($F_{max} \sim 237$ GHz)

Stability Factor



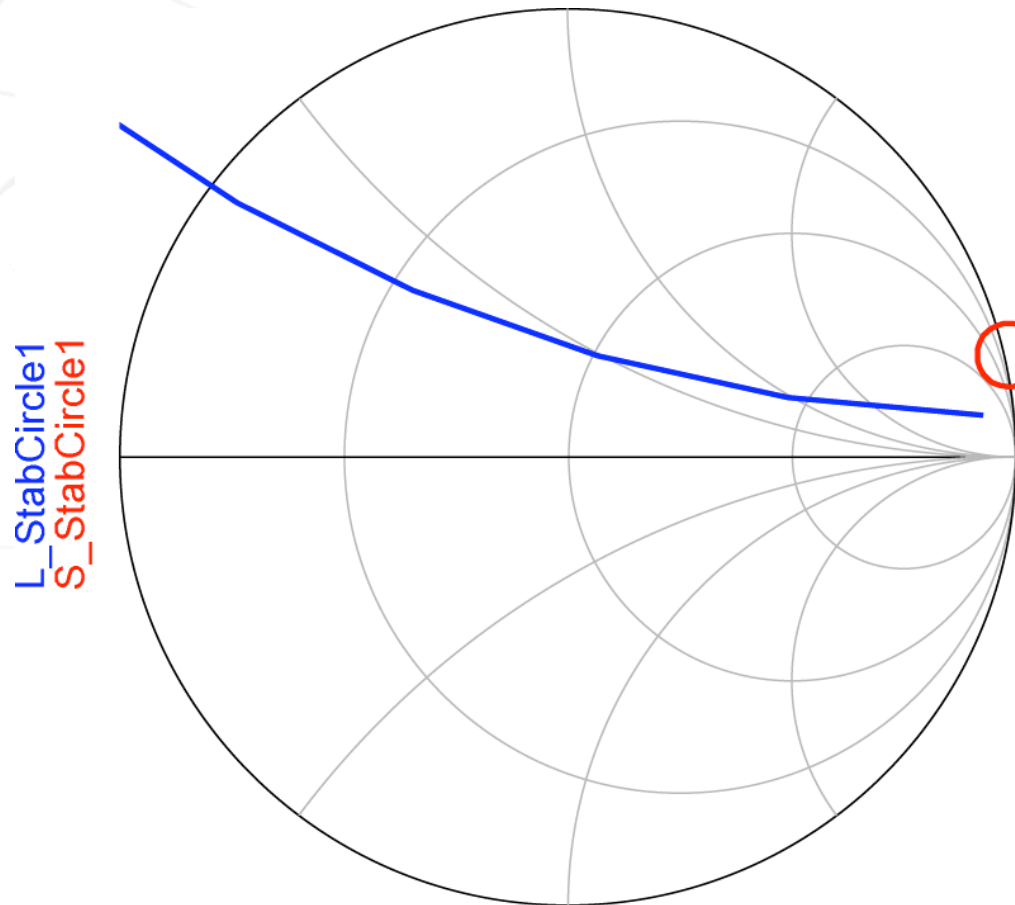
- Device is unconditionally stable only after 100 GHz!
- For a stable amplifier, need to add loss to input/output to make $K > 1$. The larger K , the more “safe” the design, but the less gain we can extract.

Example: 10 GHz Design

- Using this transistor, let's design an amplifier.
- Since it's bilateral, it's easier to work with the operating power gain, which is only a function of the load impedance.
- We'll notice that the source instability circle only crosses the unity Smith chart over a small region. So it's safe to assume that we can pick the optimum load and then conjugate match the input (without stability issues).
- We can always check to make sure this is true in the design.

Source/Load Stability Circles

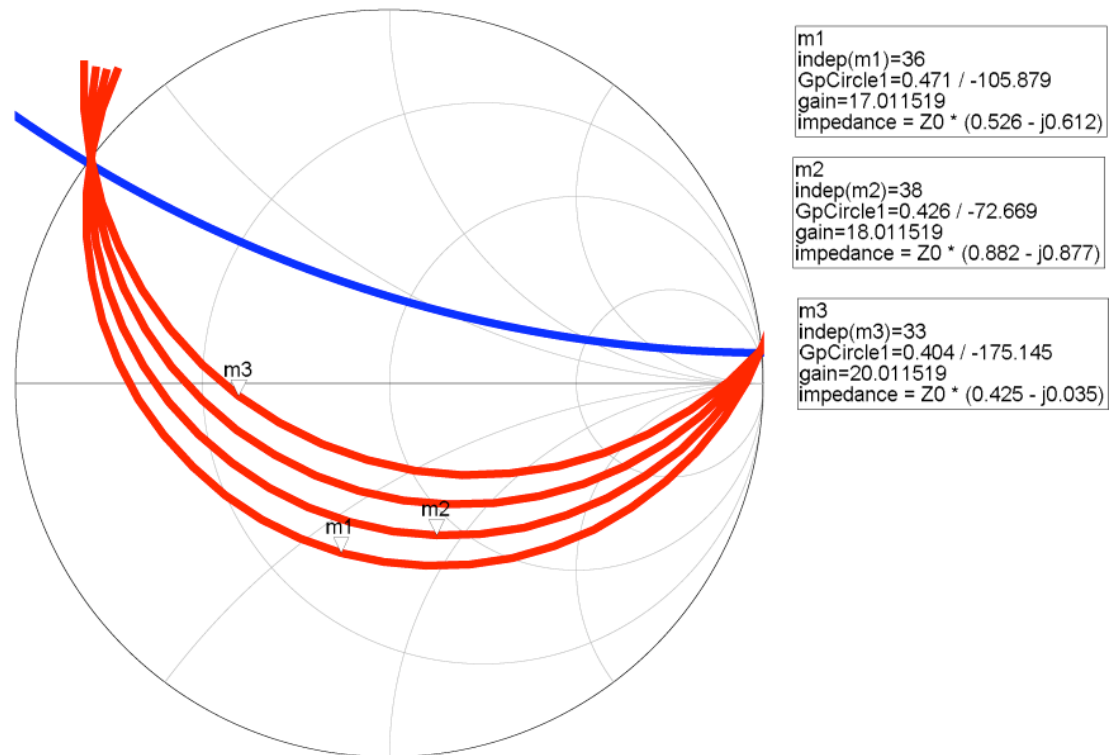
- Since $|S_{11}| < 1$ and $|S_{22}| < 1$, the origin is stable
- The source instability region is very small.
- The load requires careful design.



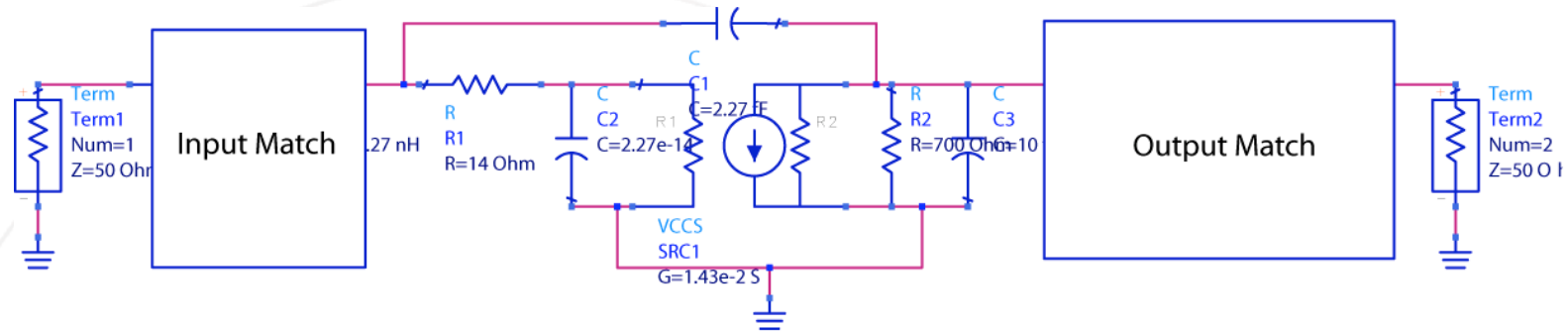
indep(S_StabCircle1) (0.000 to 51.000)
indep(L_StabCircle1) (0.000 to 51.000)

Power Gain Circles

- Any point on a constant power gain circle that does not lie in the instability region is a potential load.
- Must double check that the source stability is also satisfied for conjugate match.



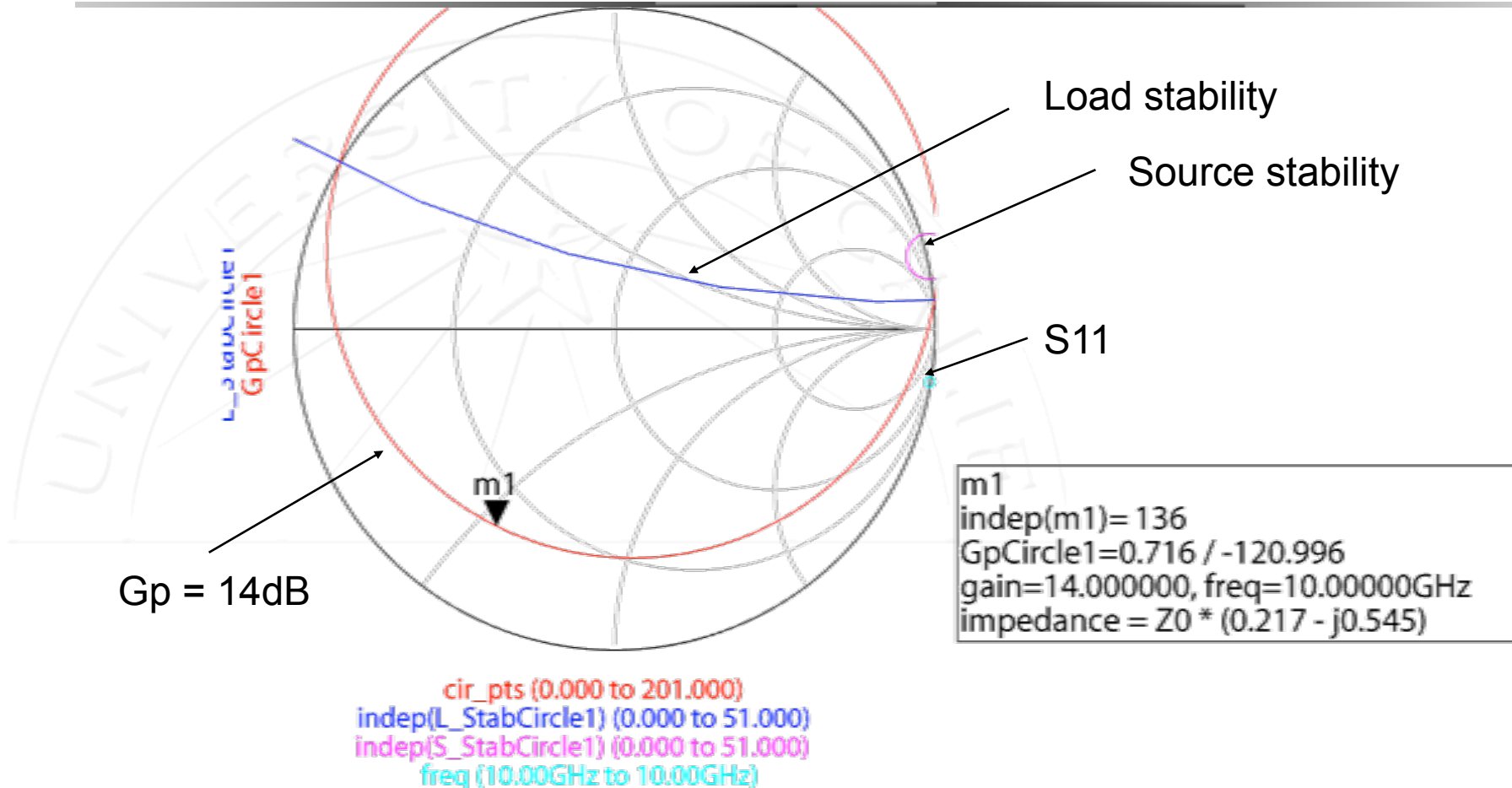
Example Amplifier Design



freq	S(1,1)	S(1,2)	S(2,1)	S(2,2)	MaxGain1
10.00 GHz	0.997 / -9.508	0.013 / 83.194	1.327 / 171.4...	0.866 / -5.018	20.012

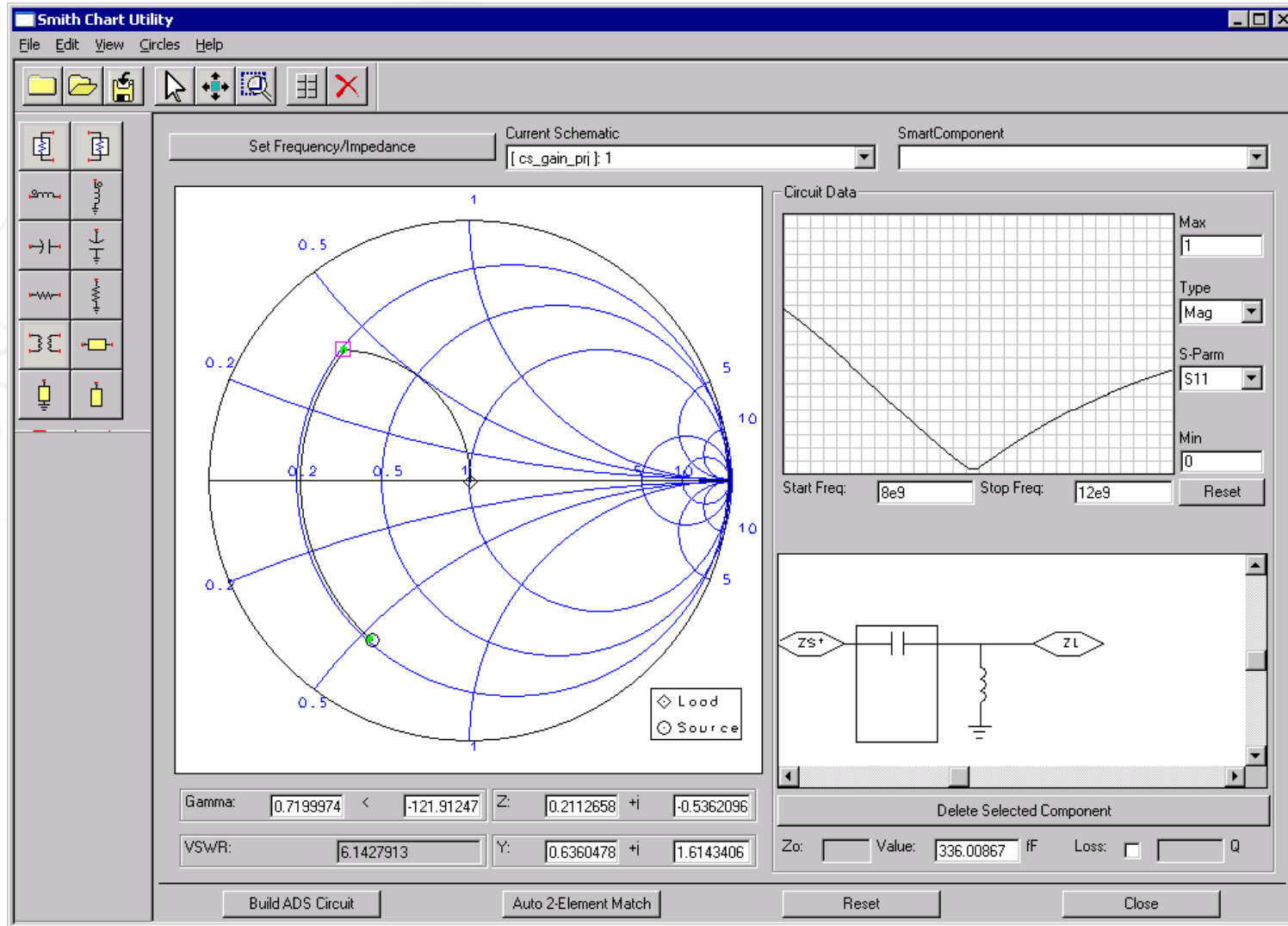
- Design a single stage amplifier with $G = 14$ dB and input match.
- Since input must be matched, let's select the load for gain/stability.
- $MSG = 20$ dB; back-off by 6 dB and plot $G_p = 14$ dB circles. Also plot load stability.
- Select load far away from instability region.

Output Load Circles



- Point m1 is far away from instability region for load.

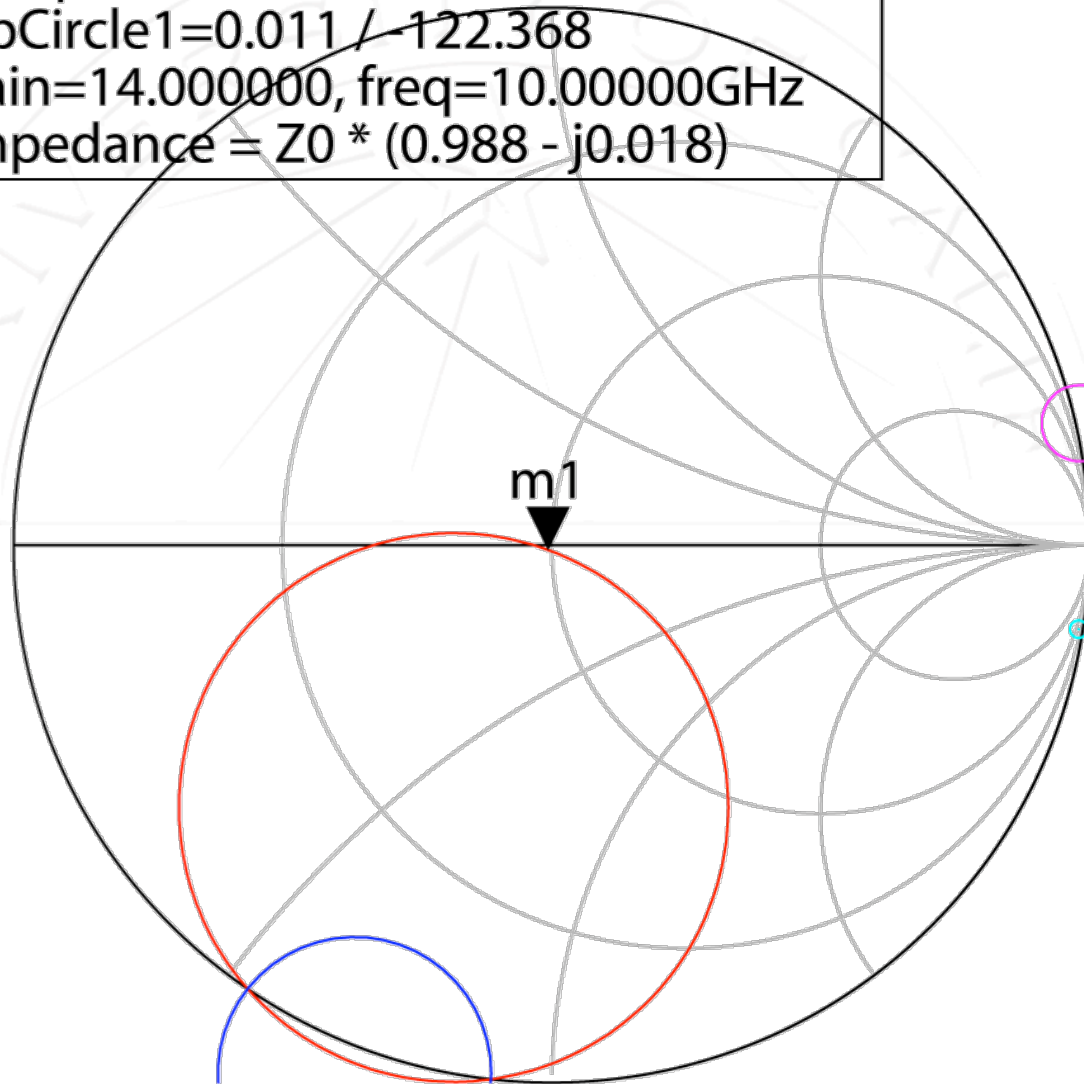
Output Matching Network



Output Load Match

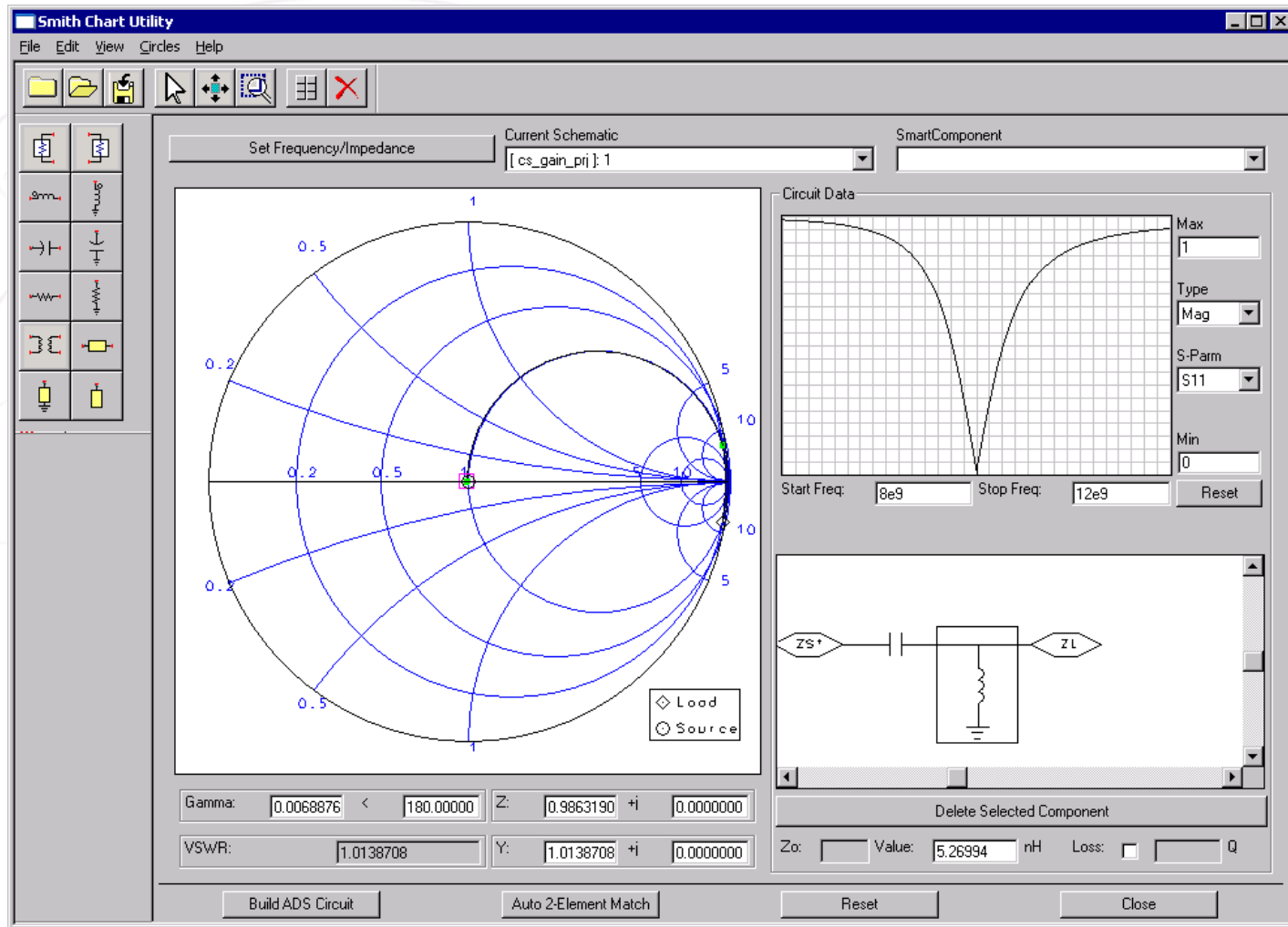
m1
indep(m1)=39
GpCircle1=0.011 / -122.368
gain=14.000000, freq=10.000000GHz
impedance = $Z_0 * (0.988 - j0.018)$

GpCircle1

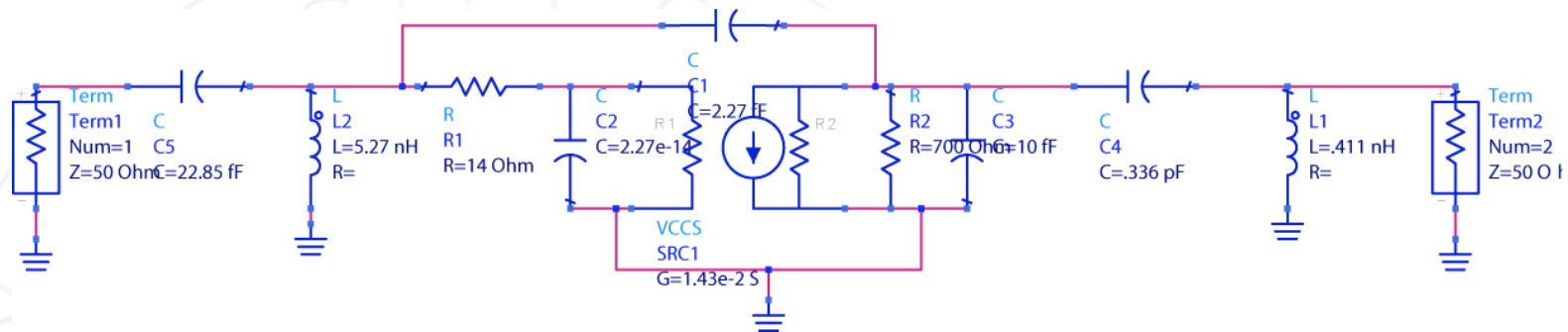


- Note that the $G_p=14\text{dB}$ circle crosses origin
- Origin still in stable region.
- Power gain is low due to input mismatch (-4 dB)
- Since S_{11} is “stable”, design input matching network for imp match

Input Match



Complete Amp Schematic

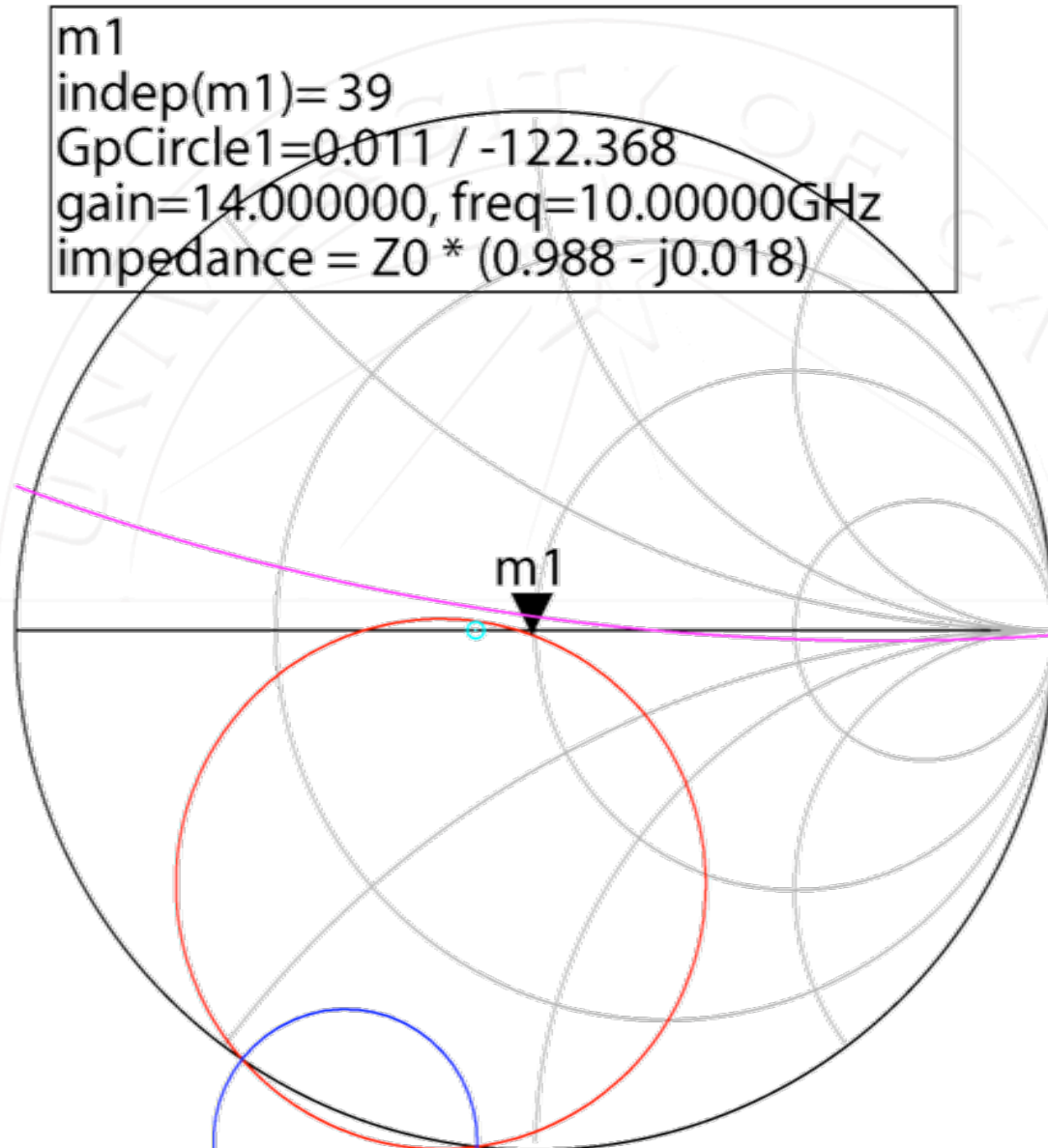


- Out match is simple L matching network; component values are reasonable.
- Other possibilities include T-line/stub matching.
- Input match component values are not very practical but okay for demonstration.

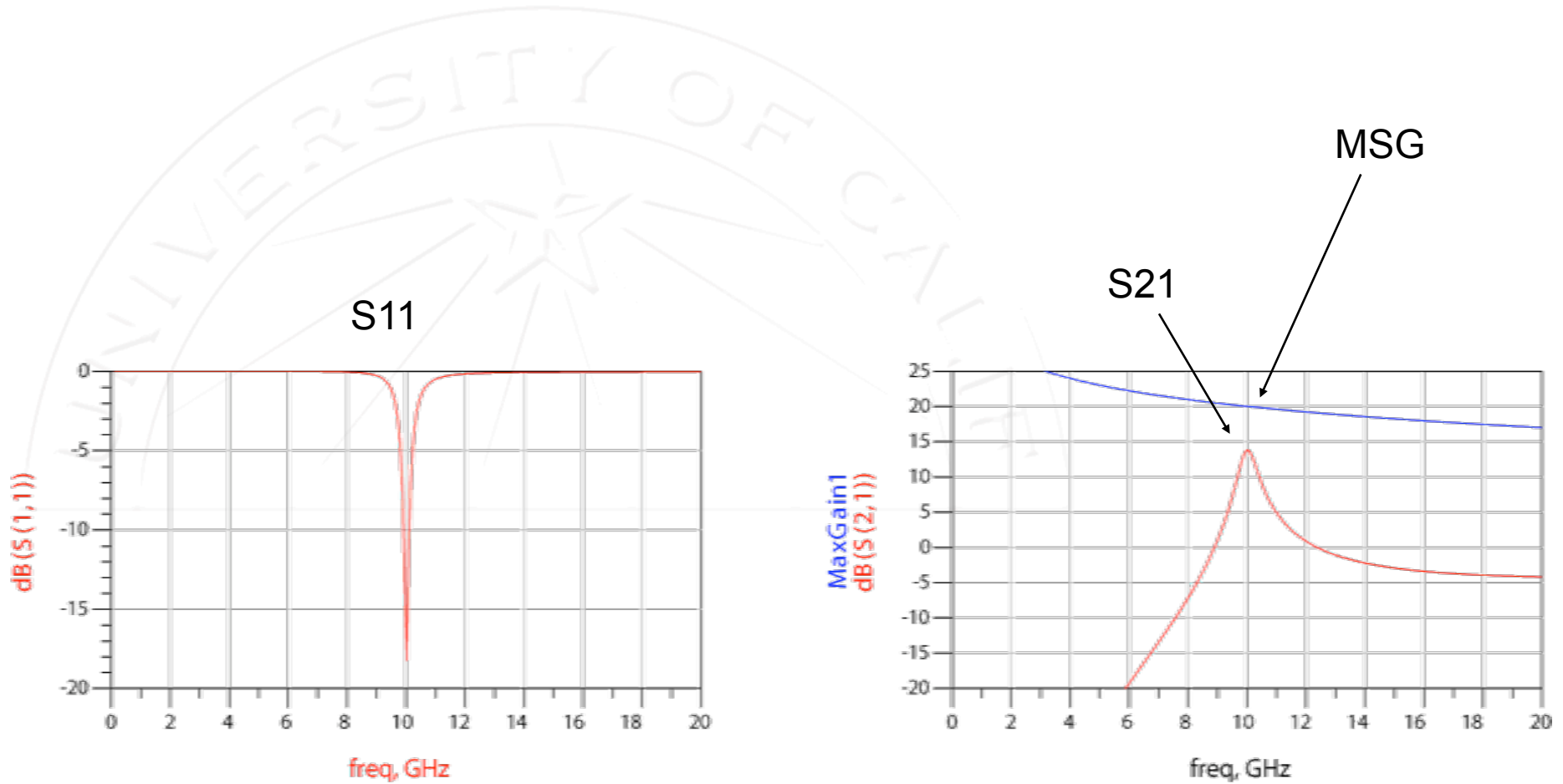
Source Matching

m1
indep(m1)= 39
GpCircle1=0.011 / -122.368
gain=14.000000, freq=10.000000GHz
impedance = $Z_0 * (0.988 - j0.018)$

- Input is matched and now the realized power gain is 14 dB
- The source stability circle, though, is dangerously close to the origin.



Match/Gain Plots



Comments on Design

- Input match looks good ($S_{11} < 0.11$)
 - Power gain is as desired: $G = 14$ dB
 - Output match is terrible ($S_{22} \sim 1$) and close to instability!
 - We see that this design requires some iteration to arrive at the best input/output match pair to give gain and good stability.
-
- In practice a lossy matching network (or added loss/feedback to device) helps to create a good match.