EECS 240
Analog Integrated Circuits

Lecture 7: Current Sources

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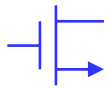
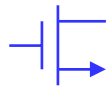


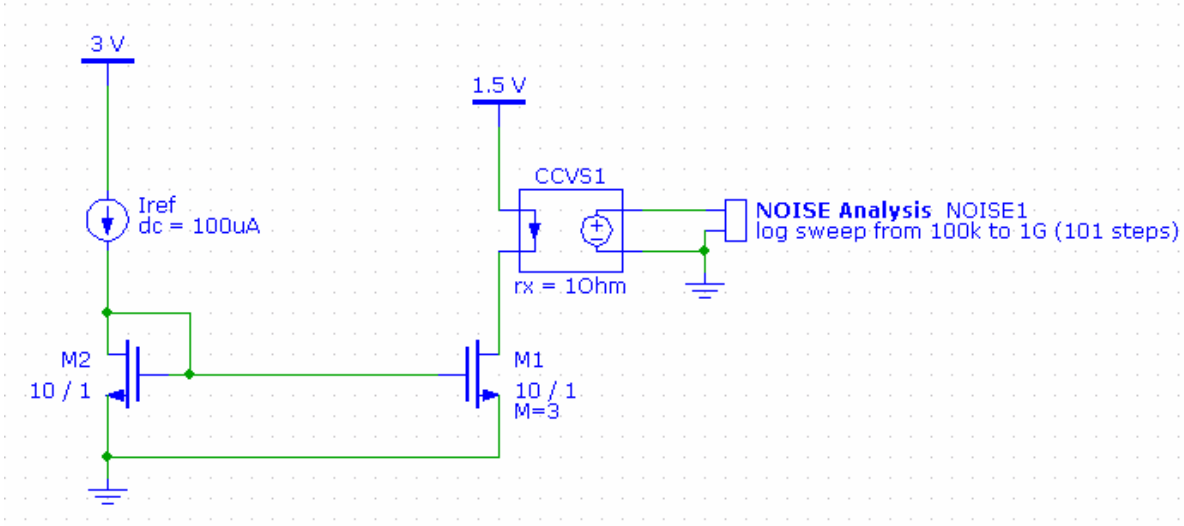
Bias Current Sources

- Applications
- Design objectives
  - Output resistance (& capacitance)
  - Voltage range (V_{min})
  - Accuracy
  - Noise
- Cascoding
- High-Swing Biasing



Current Mirror

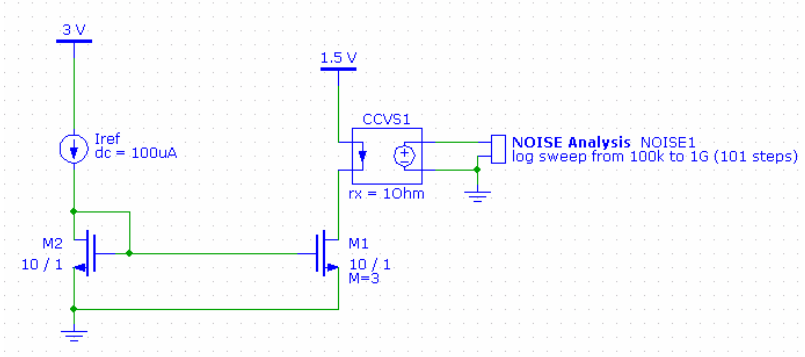
- Bias
- Noise
- Cascoding



Noise

$$\overline{i_{on}^2} = \overline{i_{d1}^2} + M^2\overline{i_{d2}^2}$$
$$= 4k_BT\gamma\left(g_{m1} + M^2 g_{m2}\right)\Delta f$$
$$= 4k_BT\gamma g_{m1}\left(1+M\right)\Delta f$$
$$= 4k_BT\frac{1}{R_N}\Delta f$$

$$R_N = \frac{1}{g_{m1}}\frac{\gamma^{-1}}{1+M}$$
$$= \frac{r_o}{a_{v0}}\frac{\gamma^{-1}}{1+M} << R_o = r_o$$



- M2 (and I_{ref}!) can add noise
  - Choose small M (power penalty), or
  - Filter at gate of M1
- Current source FOMs
  - Output resistance R_o
  - Noise resistance R_N
  - **Active sources boost R_o, not R_N**

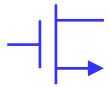
V_{min} versus Noise

$$V_{\min} = k \times V^* \qquad \text{typ.} \quad k = 1...2$$

$$R_N = \frac{1}{g_{m1}} \frac{\gamma^{-1}}{1+M}$$

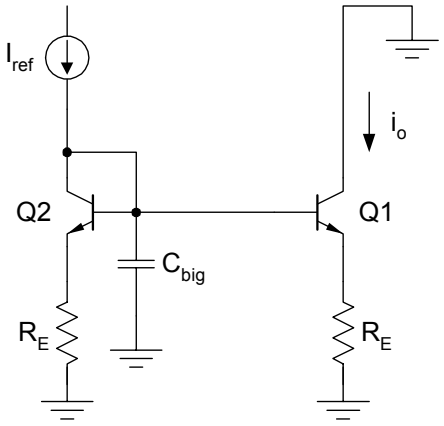
$$= \frac{V_{\min}}{2KI_D} \frac{\gamma^{-1}}{1+M}$$

- Voltage required for large Ro (saturation): V_{min} ~ V* (based on intuition from square-law model)
- Minimizing noise (for given I_D):
  → large R_N
  → **large V_{min} (k >> 1)**
- At odds with signal swing (to maximize the dynamic range)



Bipolar's, GaAs, …

$$\overline{i_{on}^2} = \underbrace{\overline{i_{cn}^2}\left|\frac{1}{1+g_m R_E}\right|^2}_{\text{BJT}} + \underbrace{\overline{i_{Rn}^2}\left|\frac{g_m R_E}{1+g_m R_E}\right|^2}_{R_E}\Delta f \qquad \left(\overline{i_b^2}=0\right)$$



a) $g_m R_E = 0$ $\qquad \overline{i_{on}^2} = 2k_B T g_m \Delta f$

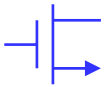
$$R_N = \frac{2}{g_m} = \frac{2V_t}{I_C} \qquad \text{set by } I_C$$

b) $g_m R_E >> 1$ $\qquad \overline{i_{on}^2} = 4k_B T \frac{1}{R_E}\Delta f$

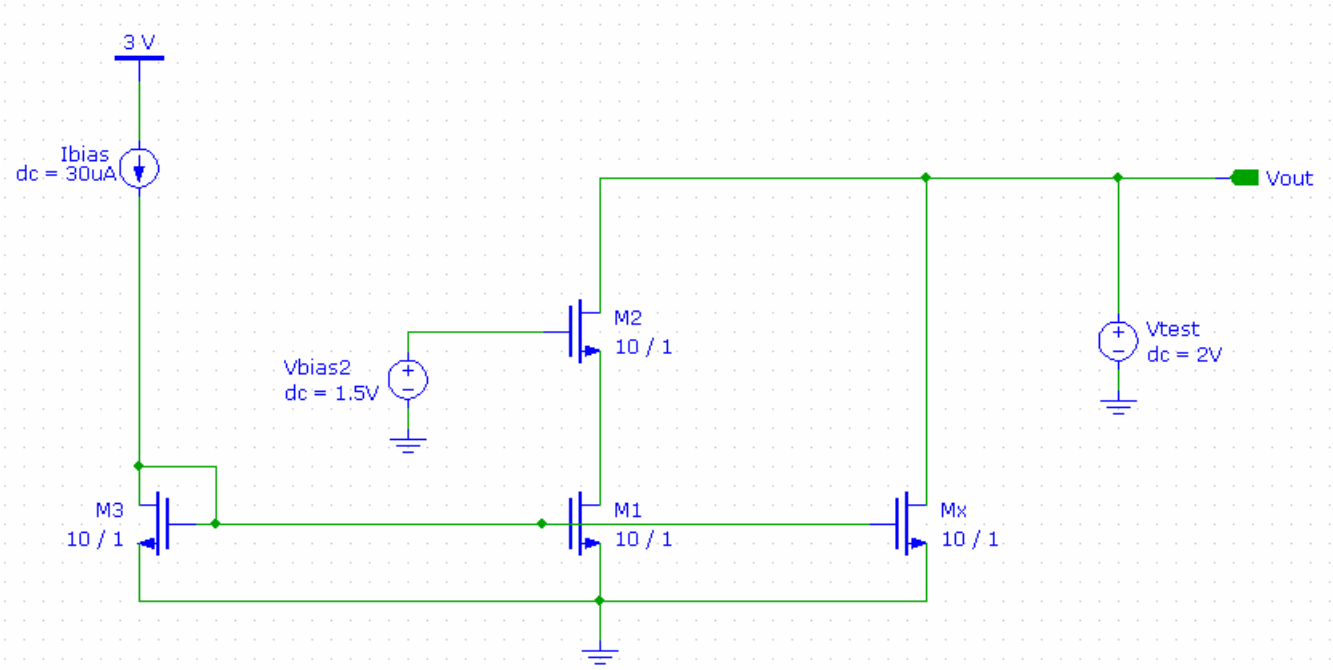
$$R_N = R_E = \frac{V_{\min}}{I_C}\frac{V_{\min} - V_{ce}^{sat}}{V_{\min}}$$

compare $\qquad R_{N,MOS} = \frac{V_{\min}}{I_D}\frac{\gamma^{-1}}{2K}$

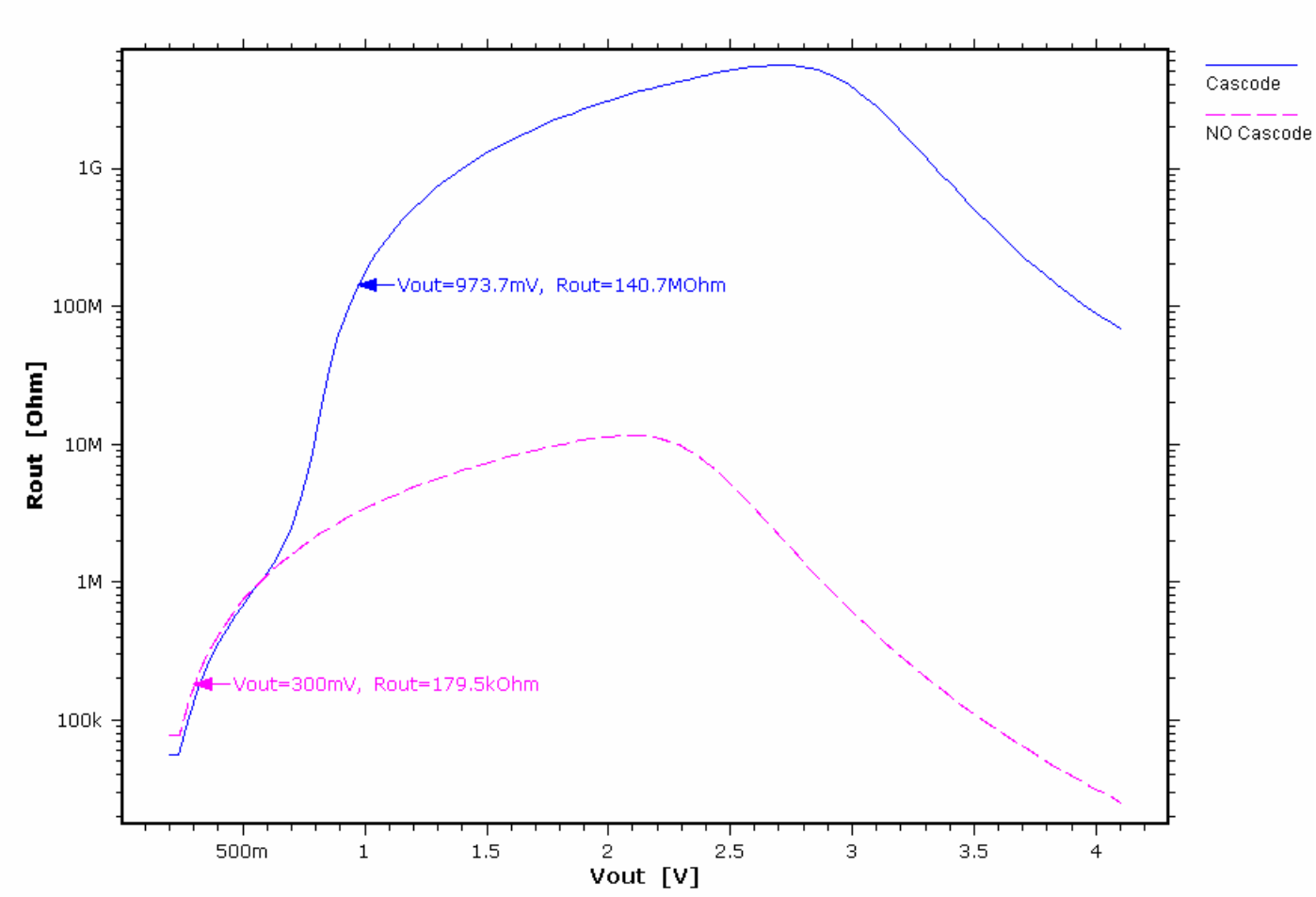
- BJT and R_E contribute noise
- Increasing R_E lowers overall noise
- BJT and MOS exhibit essentially same noise / V_{min} tradeoff
- Lowest possible noise source is a resistor (and large V_{min}, V_{DD})



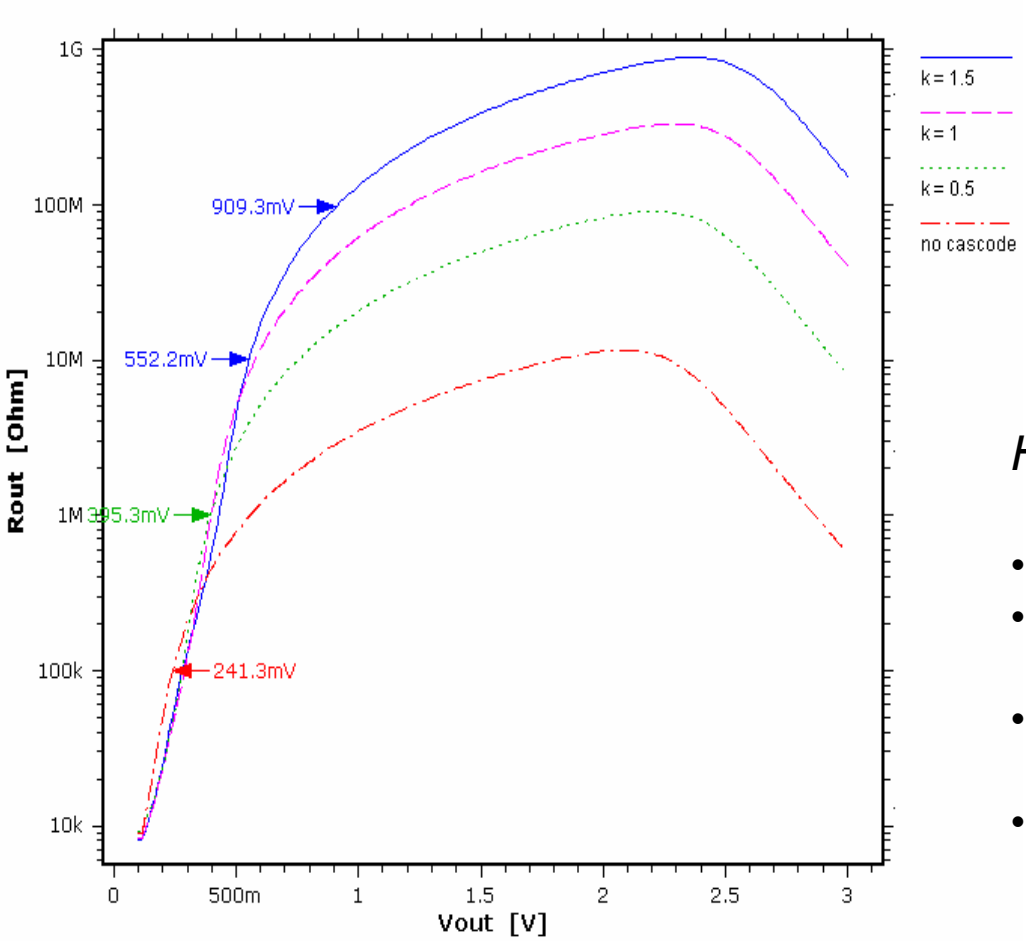
Cascoding



Output Resistance



$R_{out} = f(k)$



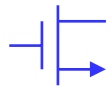
$$V_{DS1} = kV_1^*$$

How choose k? Issues:

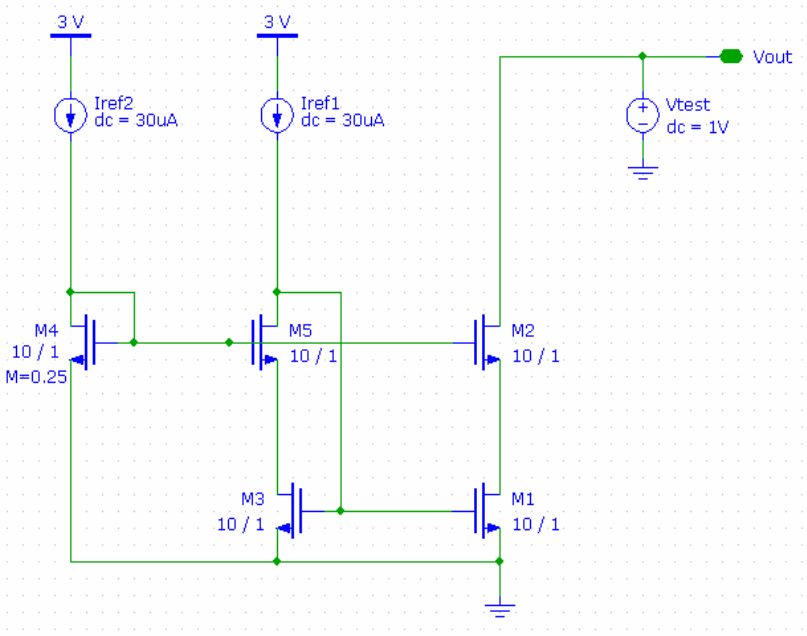
- Swing versus R_o
- Large k useful only for large V_{min} simultaneously
- Note: small or no penalty for large k and small V_{min}
- → typically choose k>1

High-Swing Cascode Biasing

- Need circuit for generating V_{bias2}
- Goal: Set V_{bias} such that $V_{DS1} \approx kV^*$
  - $k > 1$ (typical: 1 … 2)
  - Important for high R_{out}
  - No penalty for moderate R_{out}
- Design for insensitivity to
  - Process variations (μ, C_{ox}, V_{TH}, γ, …)
  - Reference current I_{ref}

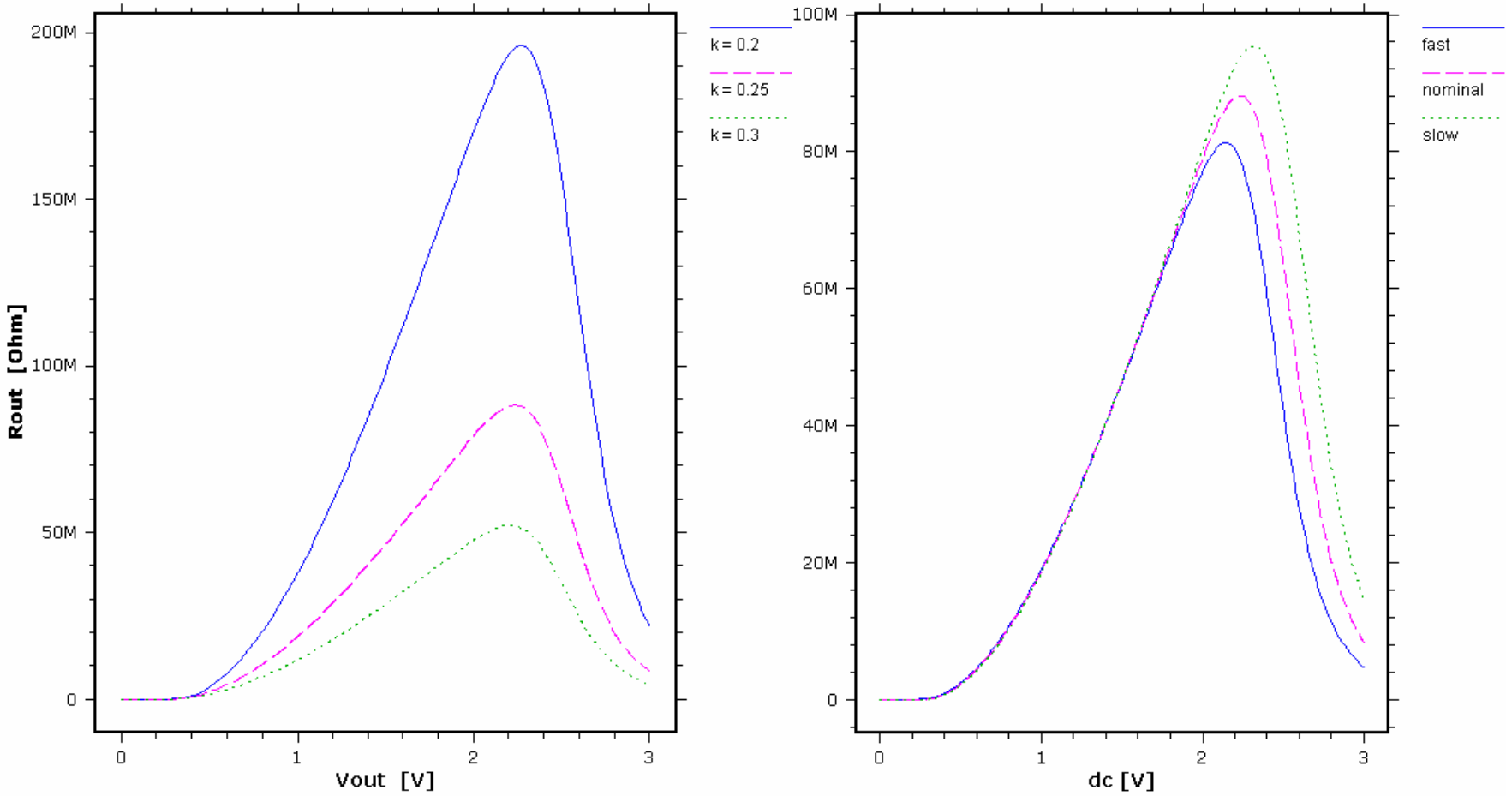


High-Swing Bias 1

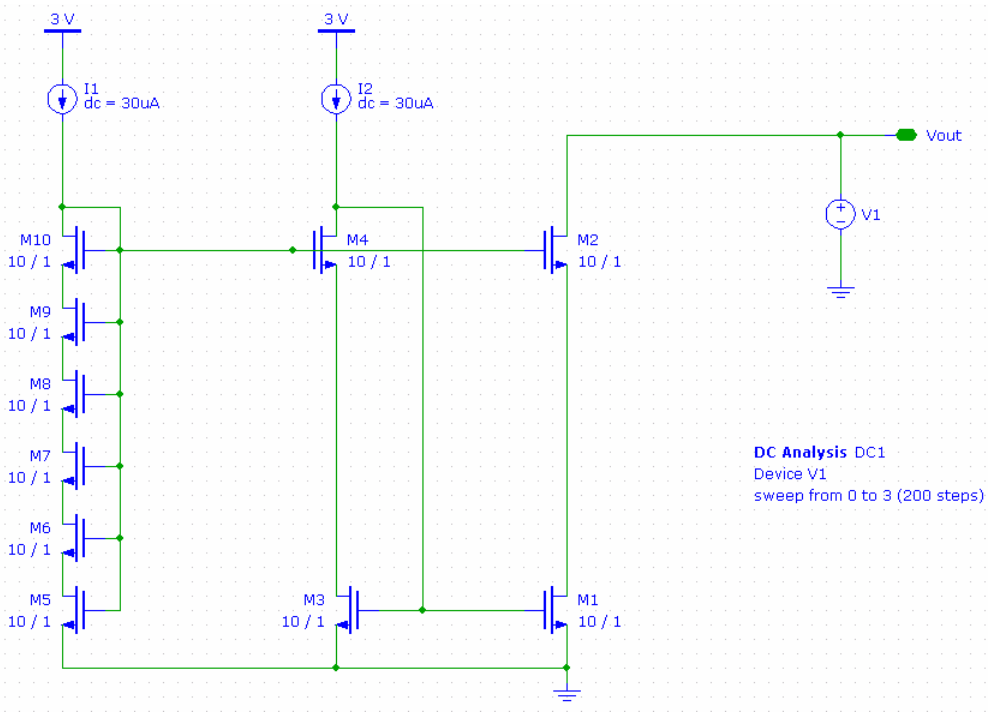


- M_4 quarter size or less
  - M=1/5 for high R_{out}
  - Note: M ≠ k
- M_5 sets $V_{DS3} = V_{DS1}$: improves matching
- Sensitive to body-effect
- $L_{current\text{-}source} = L_{cascode}$
- Simple

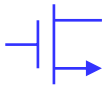
R_{out}



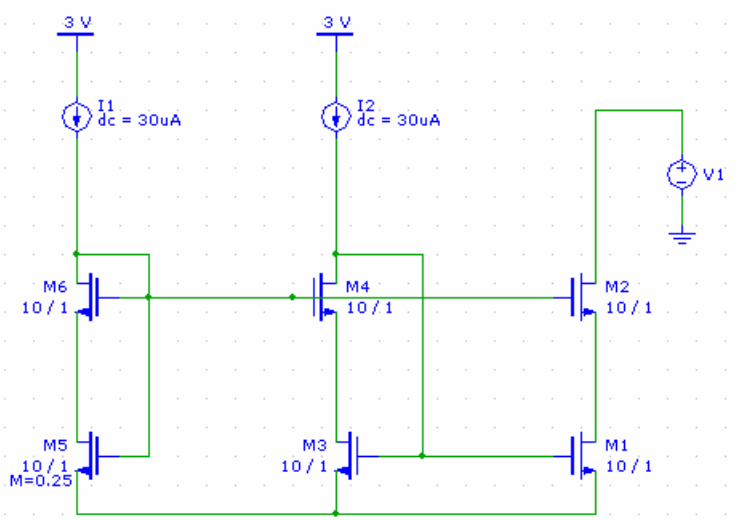
High-Swing Bias 2



- M5 … M10 replace quarter size device
- All devices same size
- Less sensitive to body-effect
- $L_{current\text{-}source} = L_{cascode}$



High-Swing Bias 3



- M_5 in triode & smaller
- All other devices same size
- Sensitive to body-effect
- $L_{current\text{-}source} = L_{cascode}$

Device Sizing

Objective:

$$V_{DS5} = R \times V_{d1}^{sat}$$

Square-law:

$$I_{D5} = \mu C_{ox} m_5 \frac{W}{L}\left(V_{GS5} - V_{TH5} - \frac{V_{DS5}}{2}\right)V_{DS5}$$

$$I_{D6} = \frac{1}{2}\mu C_{ox} \frac{W}{L}\left(V_{GS6} - V_{TH6}\right)^2$$

with

$$I_{D5} = I_{D6}$$

$$V_{GS5} = V_{GS6} + V_{DS5}$$

$$V_{GS6} = V_{TH6} + V_{d6}^{sat} \quad \text{with} \quad V_{d6}^{sat} = V_{d1}^{sat}$$

substitute

$$\left(V_{d6}^{sat}\right)^2 = m_5\left(V_{DS5} + 2V_{d6}^{sat} + 2\Delta V_{TH}\right)V_{DS5}$$

solve:

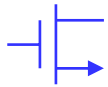
$$V_{d6}^{sat} = m_5 V_{DS5}\left(1 + \sqrt{1 + \frac{1}{m_5} + \frac{2}{m_5}\frac{\Delta V_{TH}}{V_{DS5}}}\right)$$

$$R = \frac{1}{m_5\left(1 + \sqrt{1 + \frac{1}{m_5} + \frac{2}{m_5}\frac{\Delta V_{TH}}{V_{DS5}}}\right)}$$

Examples:

$m_5 = 1/3, \ \Delta V_{TH}=0V$
$R = 1$

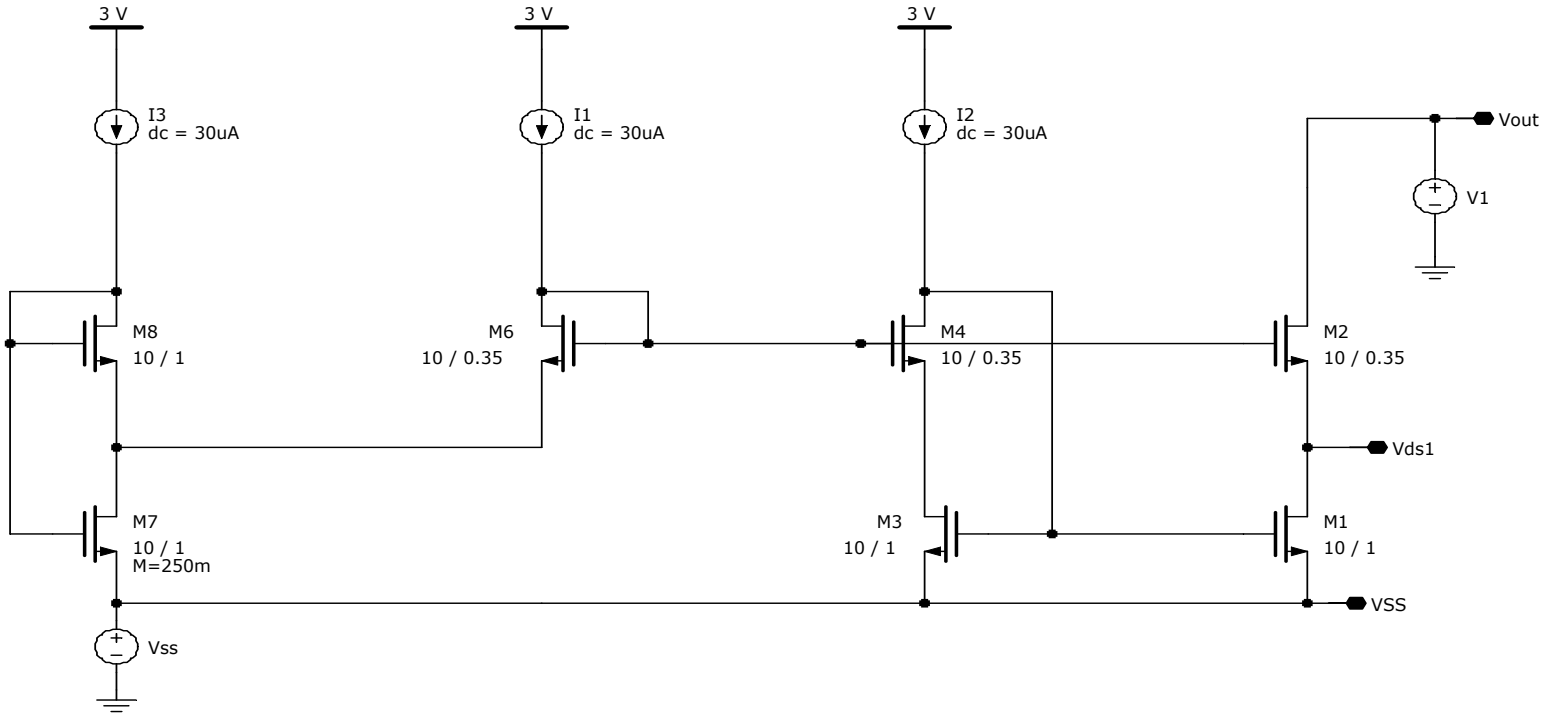
$m_5 = 1/4, \ \Delta V_{TH}=0V$
$R = 1.55$



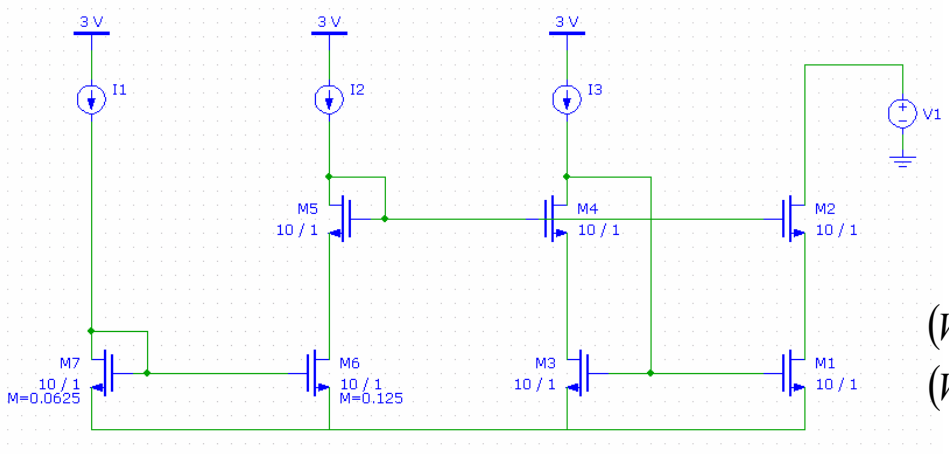
Different Device Length

High Swing Cascode Bias 3:
Current Source and Cascode have different Channel Length

DC Analysis DC1
Device V1
sweep from 0 to 3 (51 steps)



High-Swing Bias 4



$$I_{D7} = \tfrac{1}{2}\mu C_{ox}\left(\tfrac{W}{L}\right)_7 \left(V_{d7}^{sat}\right)^2$$

$$I_{D6} = \mu C_{ox}\left(\tfrac{W}{L}\right)_6 \left(V_{d7}^{sat} - \tfrac{1}{2}V_{DS6}\right)V_{DS6}$$

solve:

$$V_{DS6} = V_{d7}^{sat}\left[1 - \sqrt{1-m}\right] \quad \text{with} \quad m = \frac{(W/L)_7}{(W/L)_6}$$

e.g.:

$$(W/L)_7 = 1/16 \qquad \text{for} \qquad V_{d7}^{sat} = 4V_{d1}^{sat}$$

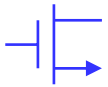
$$(W/L)_6 = 1/8 \qquad m = 0.5$$

then

$$V_{DS6} = 0.3V_{d7}^{sat} = 1.2V_{d1}^{sat}$$

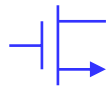
- M_6 in triode
- Insensitive to body effect
- Current source and cascode device length may differ
- Need 3 reference sources (increased power dissipation)
- *Large device ratios*

Ref: Carlos A. Laber, Chowdhury F. Rahim, Stephen F. Dreyer, Gregory T. Uehara, Peter Kwok, Paul R. Gray; *Design considerations for a high-performance 3-μm CMOS analog standard-cell library*, IEEE Journal of Solid-State Circuits, vol. 22, pp. 181 - 189, April 1987.

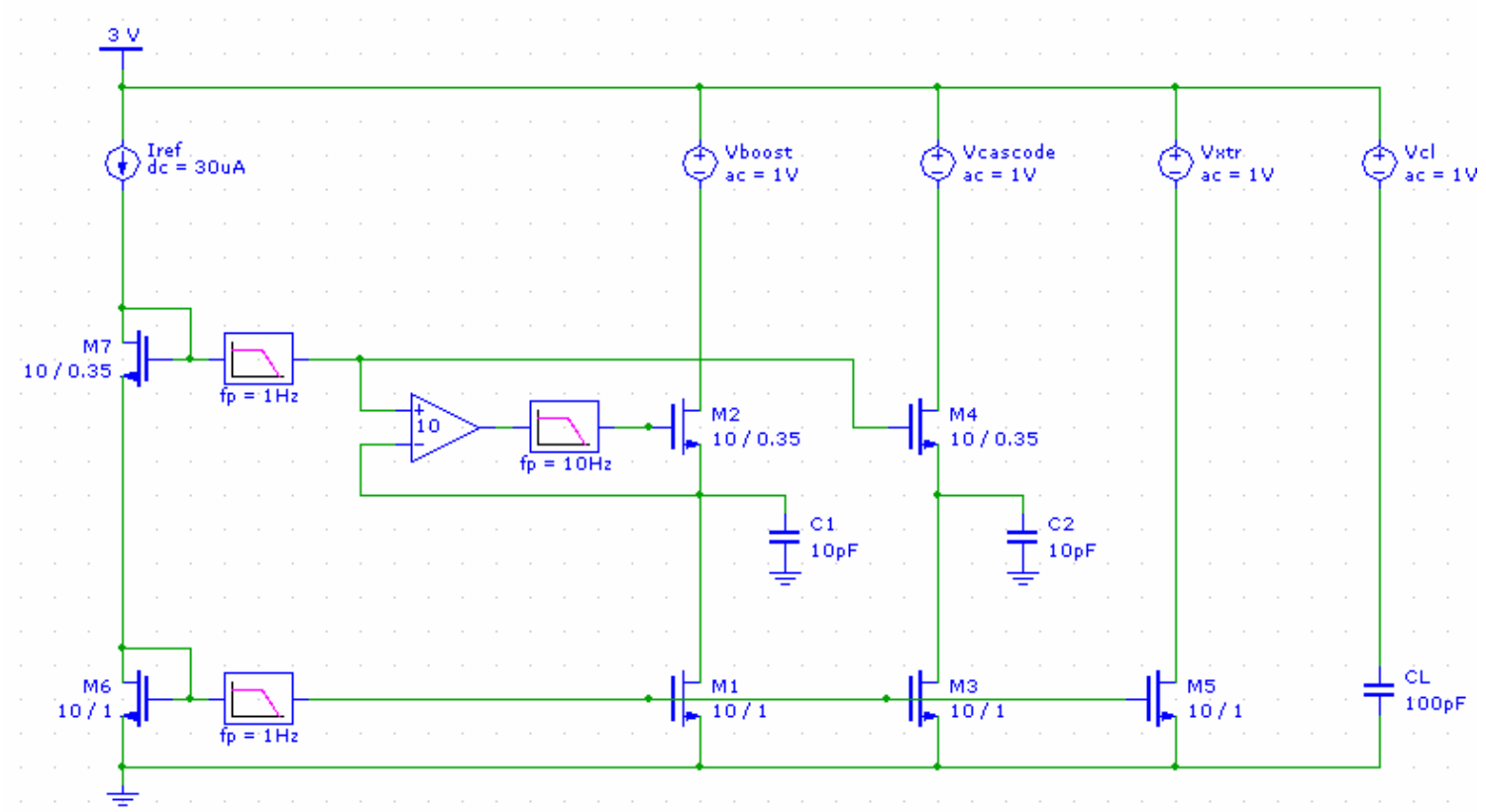


Gain Boosting

- Use feedback to further increase R_{out}
  - No increase of V_{min} (unlike double cascode)
- Local feedback → potential instability
- Beware of doublets (slow settling)
- Noise enhancement

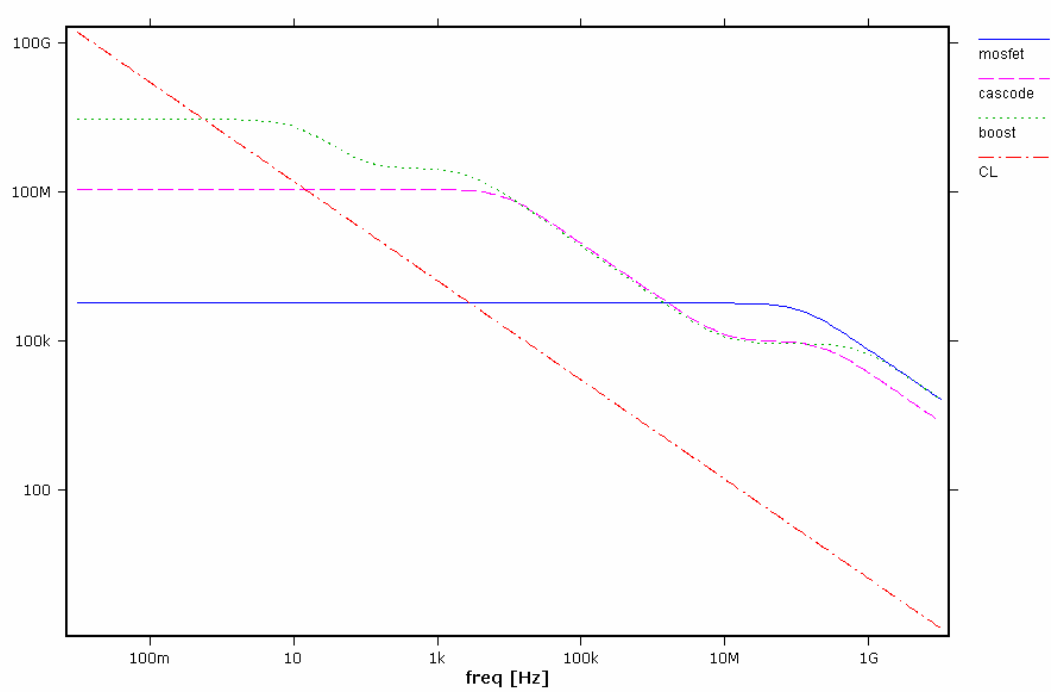


Gain Boosting Analysis



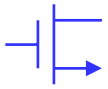
Note: C1 & C2 would not be present in an actual circuit (or smaller). They are added here to separate pole frequencies.

Z_{out}

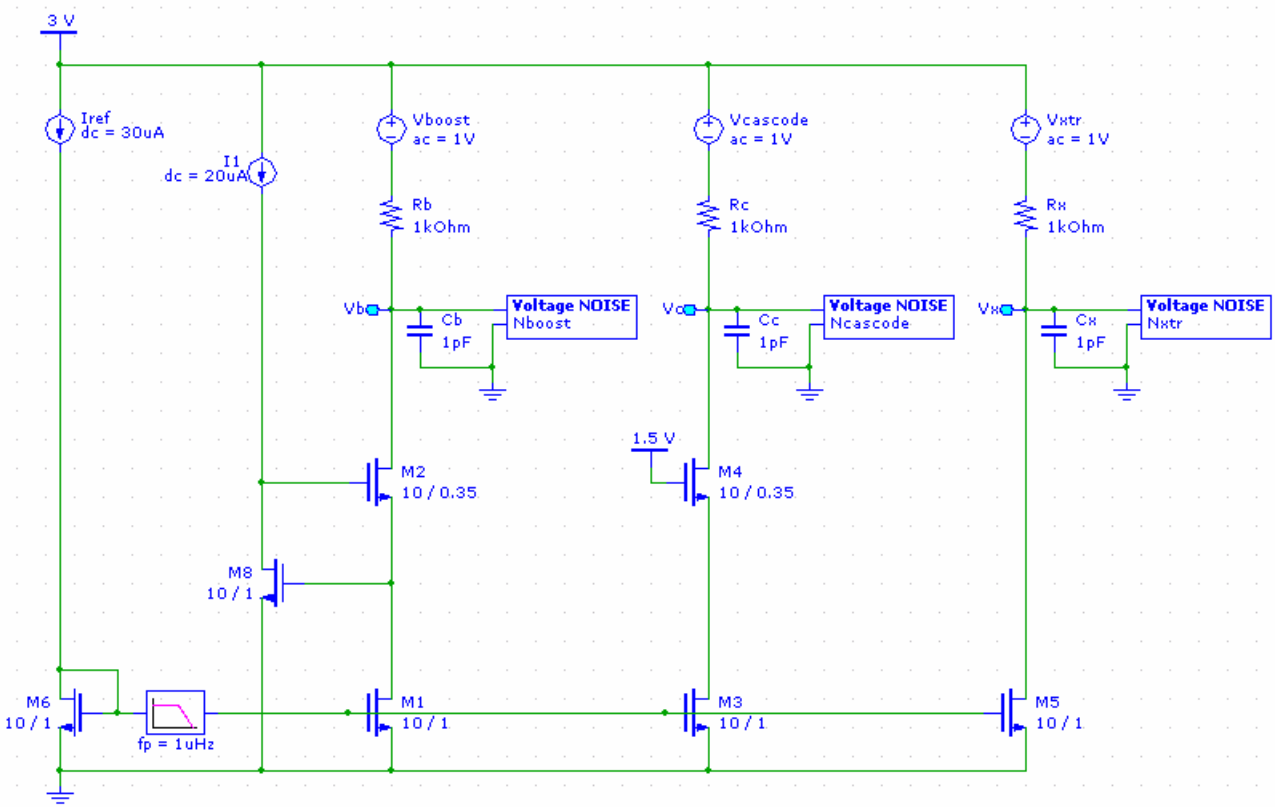


- $Z_{total} = Z_{boost} // Z_{CL}$
- Doublets → slow settling
- Booster bandwidth tradeoff:
  - push doubled above closed-loop bandwidth
  - ensure stability (nondominant pole at source of M_2)

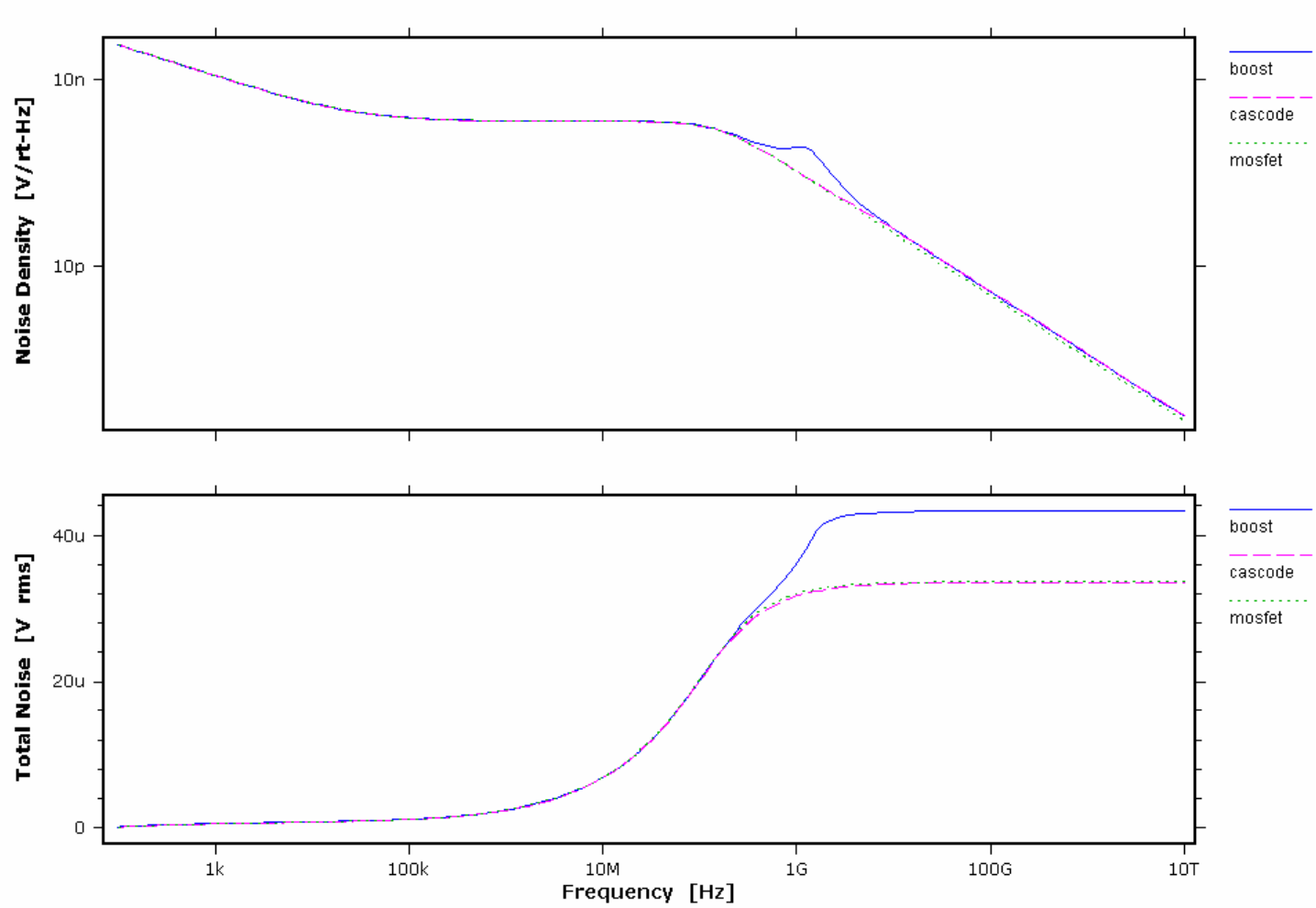
Ref: Klaas Bult, Govert J. G. M. Geelen; *A fast-settling CMOS Op amp for SC circuits with 90-dB DC gain*, IEEE Journal of Solid-State Circuits, vol. 25, pp. 1379 - 1384, December 1990.



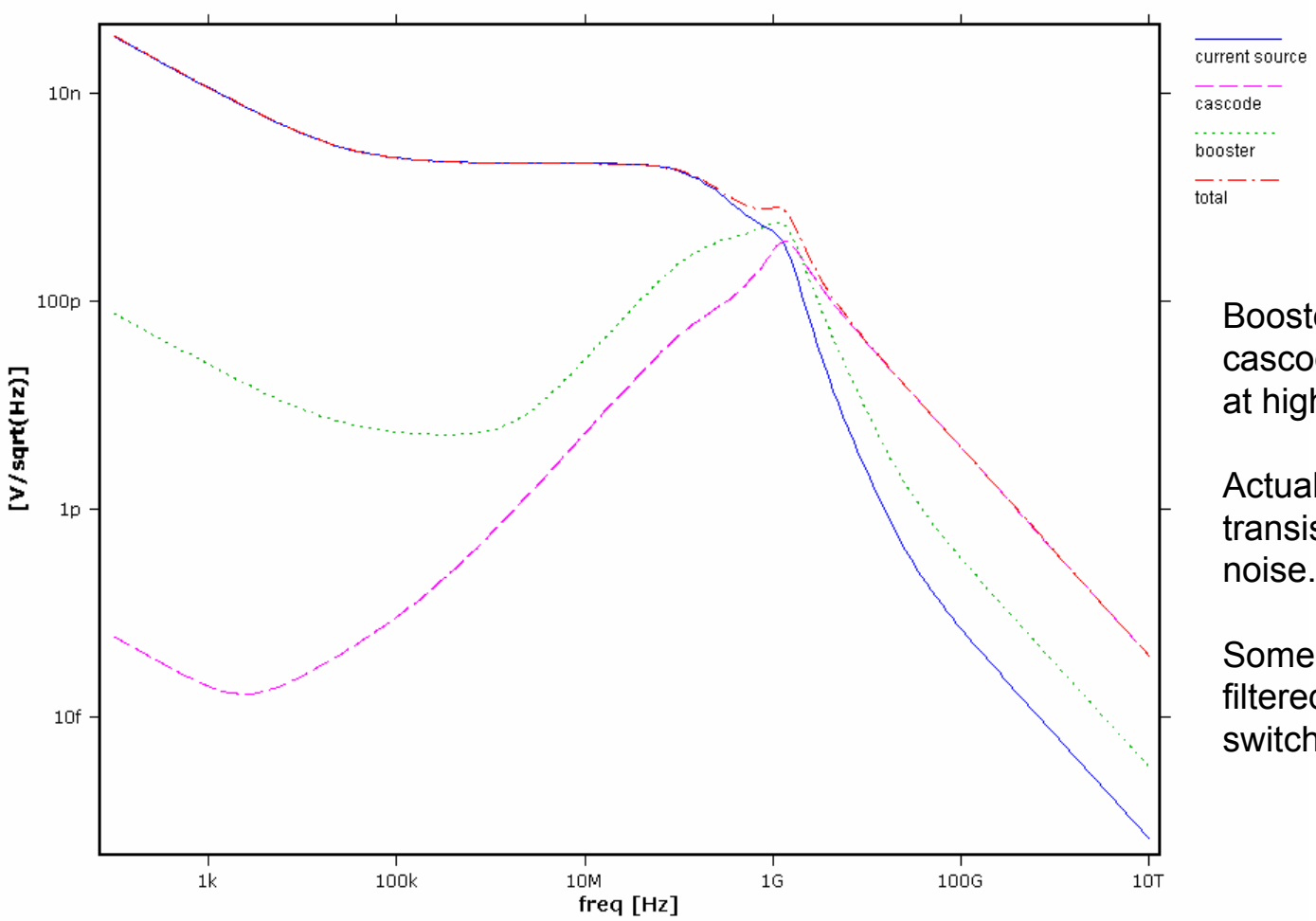
Noise Analysis



Noise Summary



Noise Detail

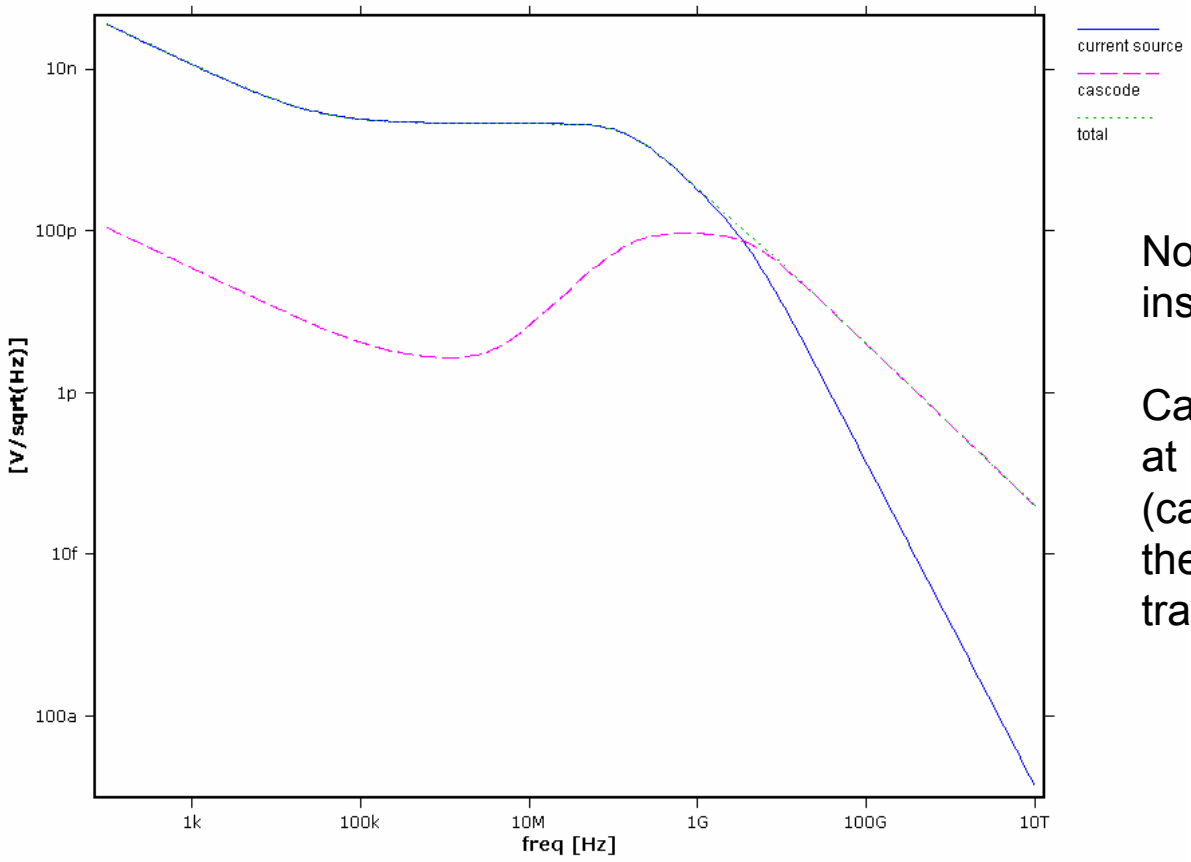


Booster amplifier and cascode contribute noise at high frequency.

Actual boosters have more transistors → additional noise.

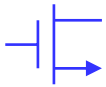
Some noise might be filtered out by sampling switch.

Cascode Noise



Noise from cascode often insignificant.

Can contribute substantially at high frequency with lots of (capacitive) degeneration at the source of the cascode transistor (poor layout).



If it works, do it again!

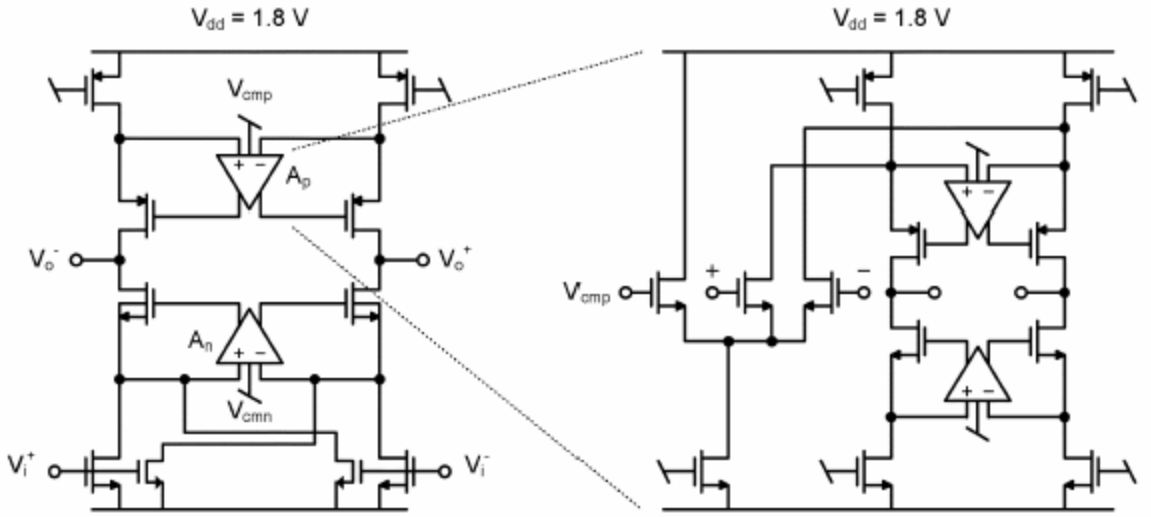
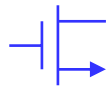


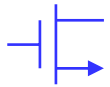
Fig. 8. Nested CMOS gain-boosting technique.

- Since in advanced scaled CMOS gmro is small, we can use nested gain boosting for higher output impedance.
- Watch out for pole-zero doublets!



Matching

- Systematic mismatch
  - ΔV_{DS}
  - source resistance
  - gradients
- Random mismatch
  - Δ (W/L)
  - ΔV_{TH}



Random Mismatch

- Model:
  (we need an equation with W/L in it …
  resort to square-law)

$$I_{D1} = \tfrac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH1})^2$$

$$I_{D2} = \tfrac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH2})^2$$

- Mismatch:
  ΔI_D, $\Delta(W/L)$, ΔV_{TH}

$$\Delta I_D = I_{D1} - I_{D2} \qquad I_D = 0.5(I_{D1} + I_{D2})$$

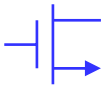
$$\Delta\left(\frac{W}{L}\right) = \left(\frac{W}{L}\right)_1 - \left(\frac{W}{L}\right)_2 \qquad \left(\frac{W}{L}\right) = 0.5\left[\left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2\right]$$

$$\Delta V_{TH} = V_{TH1} - V_{TH2} \qquad V_{TH} = 0.5(V_{TH1} + V_{TH2})$$

- Substitute:

$$\frac{\Delta I_D}{I_D} = \frac{\Delta\left(\frac{W}{L}\right)}{\left(\frac{W}{L}\right)} - \frac{2\Delta V_{TH}}{V_{GS} - V_{TH}}$$

- → choose large V_{GS}-V_{TH} (V*)



Mismatch Example

$$\sigma_{\Delta\left(\frac{W}{L}\right)\Big/\left(\frac{W}{L}\right)} = 1\%$$

$$\sigma_{\Delta V_{TH}} = 3\text{mV}$$

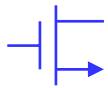
$$V_{GS} - V_{TH} = 300\text{mV}$$

$$\sigma^2_{\frac{\Delta I_D}{I_D}} = \sigma^2_{\Delta\left(\frac{W}{L}\right)\Big/\left(\frac{W}{L}\right)} + \frac{4\sigma^2_{\Delta V_{TH}}}{(V_{GS}-V_{TH})^2}$$

$$= (0.01)^2 + \left(\frac{2\times 3}{300}\right)^2 = (100+100)\times 10^{-6}$$

$$= \underline{(1.4\%)^2}$$

- Represent mismatch as random quantities
- Variances (squares!) add … like noise
- Use large V* (or degeneration) for good current mirror matching



Yield

- Yield = fraction of good dies

- E.g. need ±2.8% matching
  $\sigma = 1.4\%$,
  $k = 2.8 / 1.4 = 2$

  yield = 0.954 = 95.4%

- Typical design goal:
  $\pm 3\sigma$ ("6σ"), i.e. k=3

k	Yield
0.2	0.159
0.4	0.311
0.6	0.451
0.8	0.576
1.0	0.683
1.2	0.766
1.4	0.838
1.6	0.890
1.8	0.928
2.0	0.954
2.2	0.972
2.4	0.984
2.6	0.991
2.8	0.995
3.0	0.997