24.6 64GHz and 100GHz VCOs in 90nm CMOS Using Optimum Pumping Method

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90nm high performance logic CMOS technology provides transistors which are typically conditionally stable at frequencies well into the millimeter-wave range (Fig. 24.6.1); and unconditionally stable at frequencies close to f_{max}. The unconditional stability allows the use of simultaneous complex conjugate matching at input and output ports of every transistor in the VCO. This matching optimally pumps energy from the active device to the passive network (optimal pumping) which is essential at frequencies close to f_{max}, where transistors have little gain.

In a typical negative-G_m LC oscillator/VCO (Fig. 24.6.2), it is required that the negative resistance, R_{in}, appearing at terminals "a" and "b" in Fig. 24.6.2 be smaller than the parallel resistance of the tank network [1]. No consideration is given to an optimum value for R_{in}. Nevertheless, optimum pumping is accomplished by considering the generalization of the LC oscillator network and its equivalent unraveled version. A signal entering transistor M1's gate (node "a"), appears at M1's drain and travels through the general passive network to enter the gate of transistor M2. This signal appears at its drain, travels through the general passive network and re-appears back at point "a". In one cycle this signal experiences the same change in phase and amplitude as if it had traveled along the equivalent unraveled infinite network shown in Fig. 24.6.2 from its node "a" to its node "a* ". Every single transistor in the unraveled infinite network is considered part of a chain of amplifiers. Since the transistors are unconditionally stable at frequencies close to f_{max}, the required Z^*_G and Z_L for simultaneous conjugate matching is readily calculated from their reflection coefficients [2]. Hence the general network transforms the impedance at the gate of each transistor, Z_G, into the required load impedance, Z_L, at the drain of the transistor of the preceding stage. In a lossless passive network, this impedance transformation preserves the coefficient of mismatching, M_S, along the unraveled chain [2].

Depending on the transistor technology, the number of stages required for a multiple-of-360° phase shift in the signal may be awkwardly high. Figure 24.6.3 shows how delay lines are added in three possible cases for the optimum pair Γ_s and Γ_L. The impedance transformation along these distributed networks crosses the horizontal-axis of the Smith-chart along one of its transmission lines. At this crossing a lossless transmission line segment of characteristic impedance defined by the crossing point is added to the VCO's passive network without disturbing the optimum pumping impedance transformation. The length (delay) added depends on the number of stages desired for the final VCO. It is important to note the optimum pumping method exploits the unconditional stability of the transistor whereas standard microwave approaches exploit device instability for oscillator design [2-4].

In this work, no commercial CMOS model was used. 90nm logic CMOS transistors were laid out and characterized by S-parameter measurements up to 50GHz. The transistor S-parameters were extrapolated to 64GHz and 100GHz. The distributed passive networks were realized using microstrip-on-die, with ground plane in metal-1 and traces in metal-7 layer. Electromagnetic Field solutions of the passive network were found using a commercial program [5]. The ground plane in metal-1 isolated the passive networks from silicon substrate losses.

External harmonic mixers were used to heterodyne the high-frequency VCO signal to lower frequencies for measurements (Fig. 24.6.4). Waveguided-probes [6] deliver the signal from the on-wafer probe to the harmonic mixers with only 1.1dB insertion loss. The harmonic mixers however presented 35dB conversion loss. Signals were tapped from the VCO's core at its lowest impedance (lowest swing) with a high-impedance tap for minimum disturbance of oscillations. The $^1/_4$-wavelength-transmission-line tap from VCO core to the transistor buffer further diminished the measured signal. The pads are part of the buffer output network and microstrip stubs were added to properly tune the pad impedance to the maximum buffer gain as shown in Fig. 24.6.5. The 64GHz and 100GHz VCOs signal were measured and centered at 63.6GHz and 103.9GHz, respectively. Calculations, based on simulation, showed that a -65dBm measured signal for both 64GHz and 100GHz meant a 0.4 Vp-p swing at the VCOs' cores at their largest swing point. Both VCOs used a 1.0V power supply and drew 20mA (64GHz) and 30mA (100GHz) of current. Both VCOs are completely functional from -50°C to 110°C. The center frequency changed approximately 5GHz (100GHz) and 3GHz (64GHz) in this temperature range, because of the relatively small temperature dependence of the phase shift of the passive network in the VCO core. Consistently, the gains for both VCOs are in the range of 2GHz/V, body bias or supply voltage control.

Phase noise was measured by heterodyning the VCO's signal to a chosen 1.5 GHz intermediary frequency (IF). Further down-conversion to baseband was used to stabilize the VCO frequency with negative feedback applied to the frequency control voltage. The phase noise is -85dBc/Hz @ 10Mhz offset, at 1.5GHz IF for the 100GHz 1-transistor core VCO in Fig. 24.6.6. It is estimated the actual phase noise of both the 64GHz and 100GHz is better than -110dBc/Hz at 10MHz due mainly to the much larger swing at the VCO's core. A 4-transistor 100GHz VCO showed about a 12dB improvement in phase noise @10MHz offset in comparison to the 1-transistor 100GHz VCO. No sub-harmonic existed; hence 64GHz and 100GHz are actually the fundamental frequencies at which the VCOs oscillate. Figure 24.6.7 summarizes the experimental results, which place 90nm CMOS competitively with other technologies for mm-wave design [7,8].

Acknowledgements:
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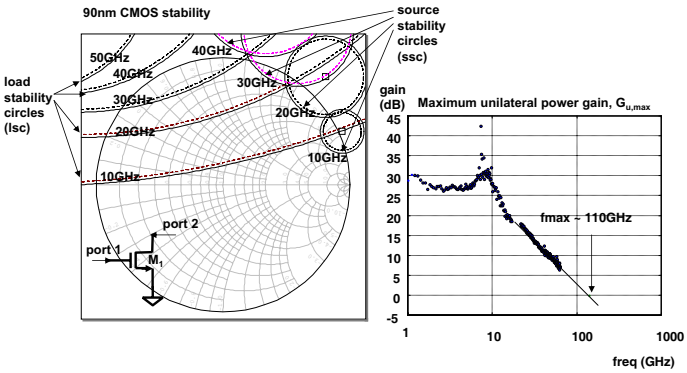

Figure 24.6.1: 90nm CMOS stability and fmax.

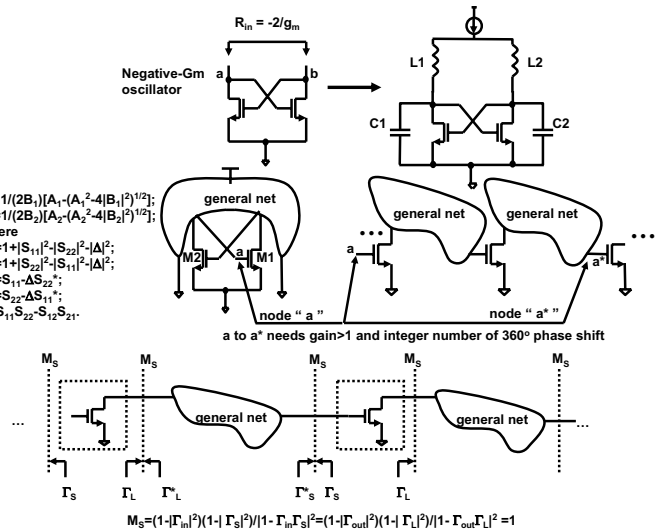

Figure 24.6.2: Negative-Gm, generalized passive network and optimum pumping.

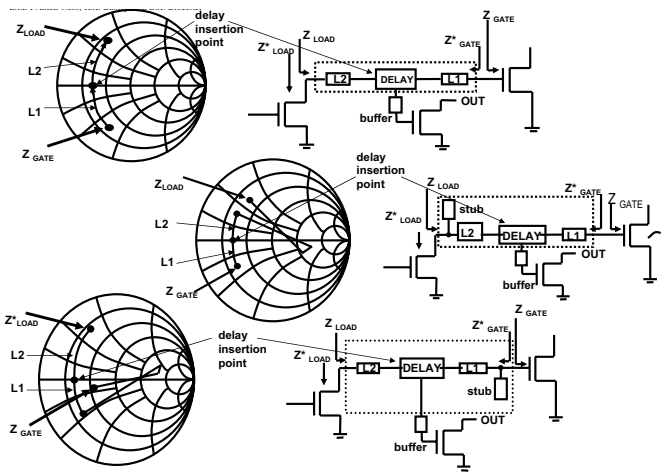

Figure 24.6.3: Adding tranmission-line delay without disturbing optimum pumping.

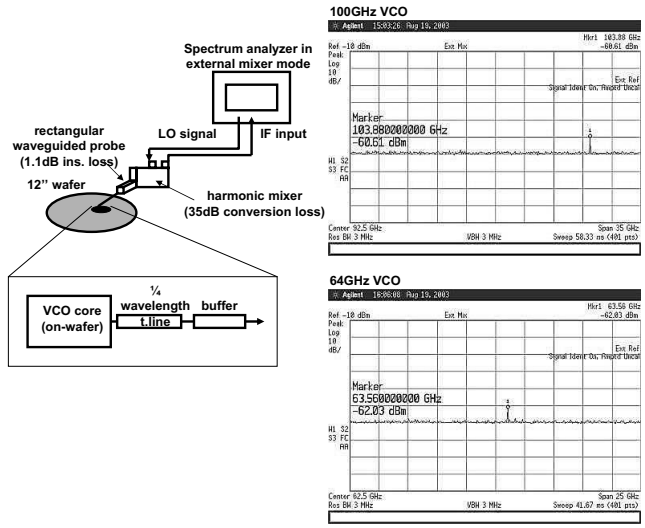

Figure 24.6.4: On-wafer measurement setup.

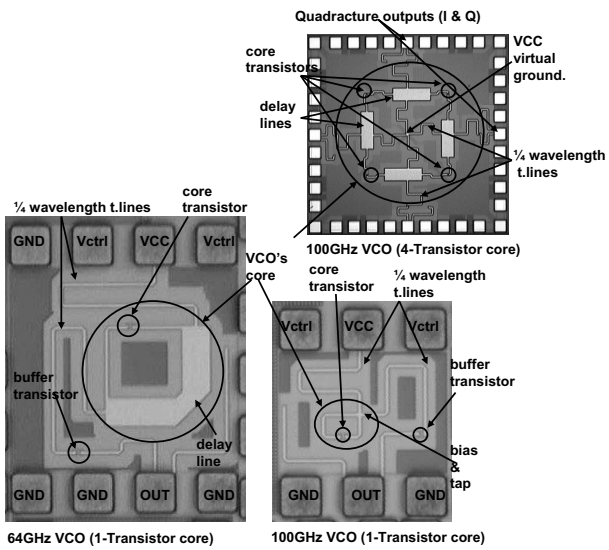

Figure 24.6.5: Die photos and microstrip network description.

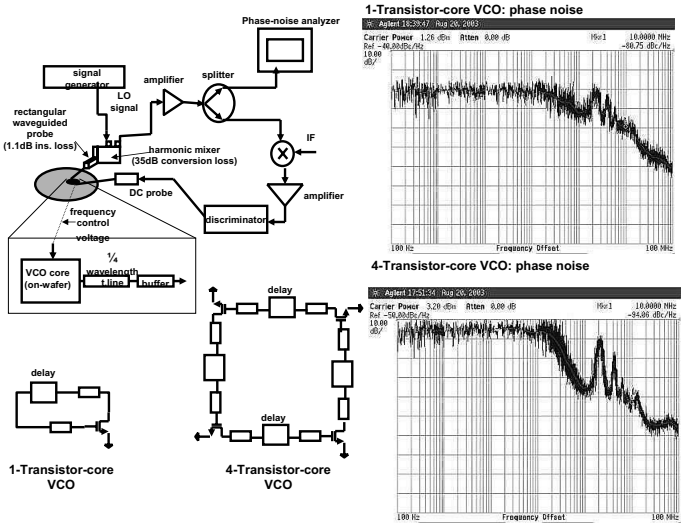

Figure 24.6.6: Heterodyne structure for phase noise measurements.

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	Topology	Digital CMOS	Transistor size (W)	Power supply	Current	Max oscillation swing at core	VCO gain	Center frequency temperature variation (-50°C to 110°C)	Phase noise
100GHz VCO	1-Transistor core	90 nm	45 μm	1V	30mA	~ 0.4Vp-p*	2GHz/V	~5GHz	< -110dBc/Hz @10MHz*
100GHz VCO	4-Transistor core	90nm	45 μm	1V	120mA	~ 0.4Vp-p*	2GHz/V	~5GHz	< -110dBc/Hz @10MHz*
64GHz VCO	1-Transistor core	90 nm	45 μm	1V	20mA	~ 0.4Vp-p*	2GHz/V	~3GHz	< -110dBc/Hz @10MHz*

* Based on measurements but back-calculated with help of simulations to refer back to VCO's core.

Figure 24.6.7: Summary of experimental results.