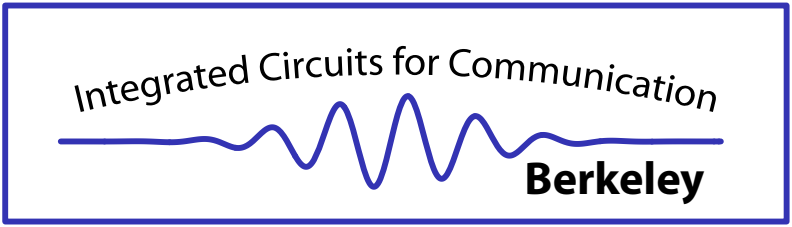

Phase Locked Loops (PLL) and Frequency Synthesis

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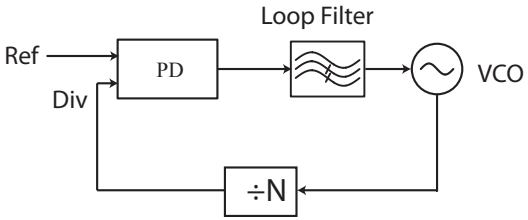
Phase Locked Loop Block Diagram



- Phase Locked Loops (PLL) are ubiquitous circuits used in countless communication and engineering applications.
- Components include a VCO, a frequency divider, a phase detector (PD), and a loop filter.

Phase Locked Loops

- A PLL is a truly mixed-signal circuit, involving the co-design of RF, digital, and analog building blocks.
- A non-linear negative feedback loop that locks the *phase* of a VCO to a reference signal.
- Applications include generating a clean, tunable, and stable reference (LO) frequency, a process referred to as *frequency synthesis*
- Other applications: Frequency modulation and demodulation (a natural "FM" modulator/demodulator). Clock recovery for high speed communication, and the generation of phase synchronous clock signals in microprocessors.
- Electronic PLLs are common, but optical and mechanical also used.

Frequency Synthesizer

- In a frequency synthesizer, the VCO is usually realized using an LC tank (best phase noise), or alternatively a ring oscillator (higher phase noise, smaller area).
- The reference is derived from a precision XTAL oscillator. The divider brings down the high frequency of the VCO signal to the range of the reference frequency. The PD compares the phase and produces an error signal, which is smoothed out by the loop filter and applied to the VCO.
- When the system locks, the output phase of the VCO is locked to the XTAL. That means that the frequency is also locked. The output frequency f_{out} is therefore an integer multiple of the reference f_{ref}

$$f_{ref} = f_{out}/N \qquad\qquad f_{out} = N \times f_{ref}$$

Programmable Divider

- By making the divider N programmable, we can tune the VCO frequency in either integer steps of the reference (integer-N architecture) or in fractional amounts (fractional-N architecture).

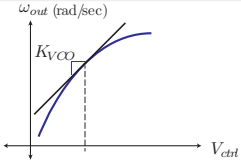
$$\Delta f = (N + p)f_{ref} - Nf_{ref} = pf_{ref}$$

- In a fractional divider, $p < 1$ and is realized by dithering the divider between N and $N + 1$ using a sigma-delta modulator.
- In practice, the programmable divider is made of up asynchronous high-speed dividers followed by programmable CMOS dividers (counters).
- The high speed dividers are sometimes in CML, which runs faster than CMOS, and has superior noise immunity and generation due to the differential nature. Injection locked or TSPC dividers are also useful for very low power high frequency operation.

Capture Range and Linear Model

- A PLL is described by several parameters, such as the *locking range*, or the range of frequencies for which it will stay locked. The *capture range* is the frequency range for which it will lock from an initially unlocked state. The capture range is smaller than the locking range.
- These parameters are hard to derive analytically and require simulation. But the dynamics of the loop, such as settling time, the noise transfer characteristics (phase noise), can be derived from a linear model.
- Therefore it is useful to derive a linear model by assuming the system is close to lock, or in lock. The most convenient variable is *phase*, and not frequency, in the linear model. Since phase and frequency are related, it's easy to go back and forth.

K_{VCO}



$$F_{VCO} = K_{VCO} V_{ctrl}$$

$$K_{VCO} = \frac{\partial F_{VCO}}{\partial V_{ctrl}}$$

- The VCO tuning curve is generally non-linear and given by a plot of output frequency versus control voltage. But when the PLL is in lock, the control voltage V_{ctrl} varies only around a small region around the lock point. We can therefore model the VCO linearly.
- Since we are interested in the phase, and observing that frequency is the time derivative of phase, we can derive

$$\Phi_{VCO} = \frac{1}{s} F_{VCO} = \frac{K_{VCO}}{s} V_{ctrl}$$

- The VCO is therefore an implicit *integrator* in the loop. This is an important fact to consider when designing a PLL.

Divider Linear Model

- From a voltage input-output characteristic, the divider is a non-linear block that simply acts like a counter. For N input edges, only one output edge occurs.
- But in terms of phase, it's a linear block

$$F_{Div} = \frac{F_{VCO}}{N}$$

$$\Phi_{Div} = \int_{-\infty}^{t} F_{Div}(\tau)d\tau = \int_{-\infty}^{t} \frac{F_{VCO}}{N}(\tau)d\tau$$

$$= \frac{1}{N}\int_{-\infty}^{t} F_{VCO}(\tau)d\tau = \frac{1}{N}\Phi_{VCO}$$

- The linear gain is just the division ratio.

Multiplier Phase Detector

- The most classic phase detector (PD) is a multiplier. Consider the product of two sinusoids offset by some phase ϕ. The product is simply given by

$$e(t) = AB\cos(\omega t)\cos(\omega t + \phi) = \frac{AB}{2}\left(\cos(\phi) - \cos(2\omega t + \phi)\right)$$

- After a low-pass filter (LPF), the high frequency term at twice the frequency is filtered out

$$< e(t) >= \frac{AB}{2}\cos(\phi)$$

- The slope of the phase detector around zero is given by

$$K_{PD} = \frac{de(t)}{d\phi} = -\frac{AB}{2}sin\phi$$

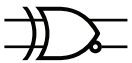
Multiplier Phase Detector (cont)

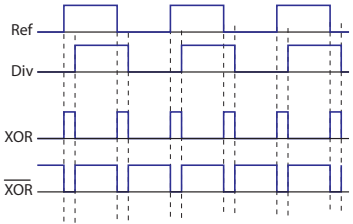
- In locked condition, the phase deviations are small and we can make the simple linear approximation

$$K_{PD} \approx -\frac{AB}{2}$$

- Note that this system will lock the VCO onto the quadrature of the reference signal.
- The negative sign is not much concern, because it can be absorbed into other gain blocks which have positive or negative gains, depending on how they are designed. We must ensure that the overall loop has negative phase shift to form negative feedback.
- Some designers reserve the option to swap the inputs of the PD just to be sure they can change things in case they make an error!

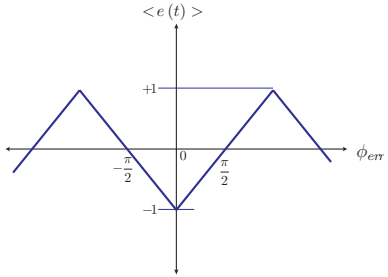
XOR Phase Detector

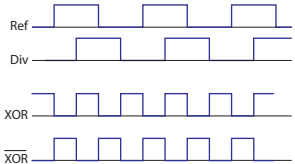




- The differential XOR gate acts very much like a multiplier. The best way to derive the transfer function is just to draw some ideal digital signals at the inputs and outputs and to find the average level of the output signal.
- Note that the output is at twice the input frequency (just like the multiplier) and a DC shift, which depends on the relative balance of the waveforms.
- The average value of the output is a linear function of the phase difference, which is exactly what we want.

XOR Phase Detector





- A sketch of the transfer curve shows that the system will also lock in quadrature (if perfectly balanced). The slope of the line determines the PD gain, $K_{PD} = \frac{1}{\pi}$
- Note that in quadrature the duty cycle of the positive and negative outputs is balanced, which produces a zero average output.
- Also note that the PD function is also periodic, much like the multiplier. In fact, the schematic of a XOR (CML) and a multiplier are very similar except for the signal levels.

Phase Detector Linear Model

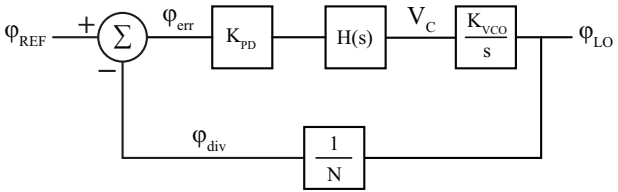
- As we have seen, the phase detector is actually a non-linear block that only extracts the phase on an average sense. We use the PD average behavior in the linear model.
- On average, the PD produces an error signal by taking the difference between the reference phase and the divided VCO phase. The PD gain is related to the slope of the transfer function

$$e(t) = K_{PD}(\Phi_{ref}(t) - \Phi_{Div})$$

Loop Filter

- The loop filter is an linear filter that smooths out the error signal and is a critical part of the system under the control of the designer.
- Passive *RC* and active filters are both used to realize the loop filter.
- Ideally the voltage on the control node of a VCO should settle to a DC value to avoid *reference spurs*. In other words, if we apply a periodic waveform on the control line, we get FM side-bands which are undesirable. Since the PD block is non-linear and non-ideal, even in lock it can produce a waveform that needs to be filtered to minimize reference spurs.

Complete Linear Model



- The loop gain is given by

$$A(s) = \frac{K_{PD}H(s)K_{VCO}}{Ns}$$

Closed-Loop Gain

- The closed loop gain is given by

$$G(s) = \frac{A}{1 + Af} = \frac{\frac{K_{PD}H(s)K_{VCO}}{s}}{1 + \frac{K_{PD}H(s)K_{VCO}}{Ns}}$$

- This is simplified to

$$G(s)/N = \frac{K_{PD}H(s)\frac{K_{VCO}}{N}}{s + K_{PD}H(s)\frac{K_{VCO}}{N}}$$

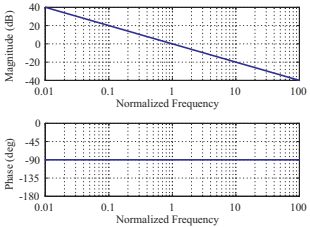
Noise Transfer Function

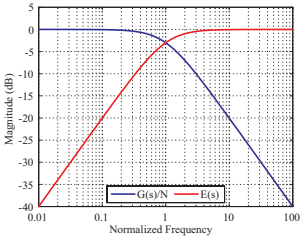
- If we consider the phase noise coming out of the VCO, its transfer function to the output is different and given by (also the transfer function for the error signal)

$$E(s) = \frac{1}{1 + A(s)} = \frac{s}{s + K_{PD} H(s) \frac{K_{VCO}}{N}}$$

- The VCO noise is therefore attenuated by the loop gain, which is very nice since the reference is usually much more spectrally pure than the VCO (it is typically constructed using a high-Q quartz resonator) whereas the VCO uses a low Q on-chip tank (inductor + varactor).
- Note that when the loop gain drops (outside of the bandwidth of the PLL), the noise of the PLL is essentially governed by the free-running noise of the VCO.

Case 1: No Loop Filter





- If we omit a loop filter, $H(s) = 1$, the loop gain is given by $A(s) = \frac{1}{Ns} K_{PD} K_{VCO}$ and the closed loop gain and error function are low-pass and high-pass respectively

$$G(s) = \frac{K_{PD} K_{VCO}}{s + K_{PD} \frac{K_{VCO}}{N}}$$

$$E(s) = \frac{s}{s + K_{PD} \frac{K_{VCO}}{N}}$$

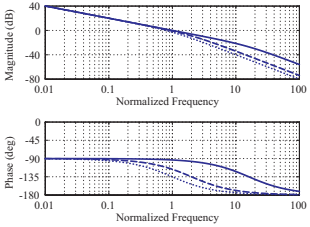
Case 1 (cont)

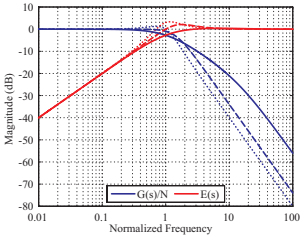
- The system has a 90° phase margin, and the loop bandwidth is given by

$$\omega_c = \frac{K_{PD} K_{VCO}}{N}$$

- Within the loop bandwidth, the output phase follows the input phase and the noise of the VCO is rejected. Outside of the band, the phase is determined by the free running VCO.

Case 2: 1 Pole LPF





- A simple LPF is used

$$H(s) = \frac{1}{1 + \frac{s}{\omega_p}}$$

- This renders the closed-loop response to be a second order function

$$G(s) = \frac{\omega_0^2}{s^2 + \frac{\omega_0 s}{Q} + \omega_0^2}$$

Case 2: 1 Pole LPF (cont)

- The natural frequency is given by

$$\omega_0 = \sqrt{K_{PD}\frac{K_{VCO}}{N}\omega_p}$$

- The Quality factor is given by

$$Q = \sqrt{\frac{K_{PD}K_{VCO}}{N\omega_p}}$$

- Since the transfer function is second order, the dynamics are well known (peaking behavior).
- One adjusts ω_p and the loop gain to set the phase margin. Loop gain increase reduces phase margin for a given ω_p.

Steady-State Step Response

- The steady-state response of the system is given by the Final Value Theorem. For instance, the final value of the error signal is given by

$$\lim_{t\to\infty} \Phi_e(t) = \lim_{s\to 0} sE(s)\phi_{in}(t)$$

- If the input is a step function, $\phi_{in} = \Delta\phi/s$, so we have

$$\lim_{s\to 0} s\frac{s}{s + K_{PD}\frac{K_{VCO}}{N}H(s)}\frac{\Delta\phi}{s}$$

$$= \lim_{s\to 0} \frac{s}{s + K_{PD}\frac{K_{VCO}}{N}H(s)}\Delta\phi = 0$$

Frequency Step

- On the other hand, if the frequency of the input goes through a step change, that corresponds to a ramp function to the phase

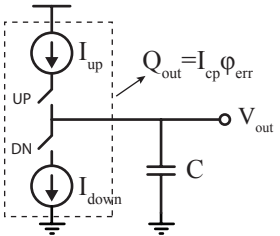
$$\phi_{in} = \frac{\Delta\omega}{s^2}$$

- which means the at the error due to a frequency step is given by

$$\lim_{s\to 0} s\frac{s}{s + K_{PD}\frac{K_{VCO}}{N}H(s)}\frac{\Delta\omega}{s^2} = \frac{\Delta\omega}{K_{PD}\frac{K_{VCO}}{N}H(0)}$$

- Unless the loop filter $H(s)$ has infinite DC gain, the loop will have a non-zero phase error if there is a frequency step.
- To remedy this, we should add another integrator into the loop. PLL's are characterized by the number of integrators in the loop. So far we have been using a type-I PLL, which has only 1 integrator (the VCO itself).

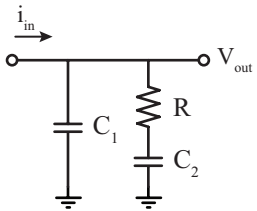
Charge Pump Integrator



$$H(s) = I(s) \times \frac{1}{sC} = (I_{up} - I_{down})\frac{1}{sC}$$

- A popular way to build a second integrator into the loop (note the first is the VCO) is to use a current source and a load capacitance.
- The current source is implemented by two sources that can pump current into and out of the capacitor. The *UP* and *DN* (Down) signals are controlled by a Phase Frequency Detector (PFD).

Lead/Lag Filter



$$H(s) = \frac{1 + \frac{s}{\omega_z}}{s(C_1 + C_2)\left(1 + \frac{s}{\omega_p}\right)}$$

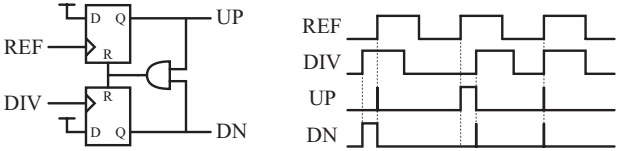
$$\omega_z = \frac{1}{R_1 C_2}$$

$$\omega_p = \frac{C_1 + C_2}{R_1 C_1 C_2}$$

- Often the load capacitance is replaced with a lead/lag filter impedance to improve the stability of the loop. Typically the capacitor C_2 is much larger than C_1, so the pole occurs at a much higher frequency.

$$H(s) \approx \frac{1}{sC_2}(1 + s/\omega_z)$$

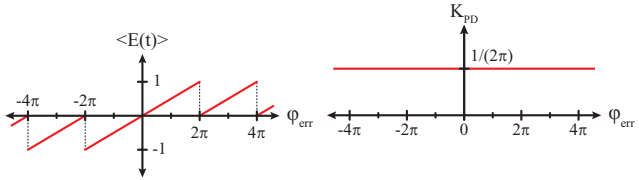
Phase-Frequency Detector



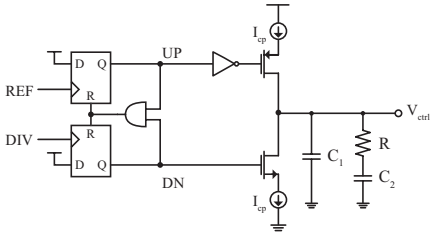
- The charge pump is usually driven by a Phase-Frequency Detector (PFD), which is an edge sensitive circuit that measures the arrival time of the reference edge relative the divider edge. When a single edge arrives, the output goes high until the second edge arrives, at which time the output signal is reset to ground.
- The "UP" signal will output a one if the reference edge arrives before the divider. Likewise, the "DOWN" signal will produce a one if the divided edge arrives before the reference edge.

Phase-Frequency Detector (cont)

- Unlike the XOR/multiplier, the circuit is sensitive to not only the phase difference, but also the sign of the phase difference.
- If VCO clock is faster than the reference (higher frequency), then its edges will always arrive earlier, which will activate the "DOWN" signal which will slow down the VCO. This functionality allows it to function as a frequency detector.
- The transfer characteristic is derived by observing the average output signal.

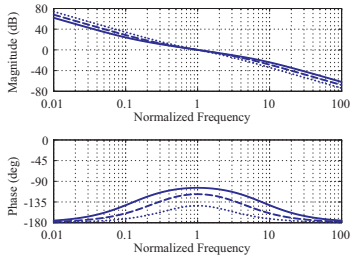


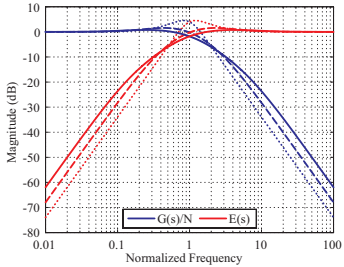
PFD + Charge Pump



- By using the up and down signals to control the charge pump, we can dump or remove charge from the integrating capacitor, and control the VCO. The functionality the PD and the first integrator are built-in to this block.
- If neither the up/down signal is activated, the capacitors hold the charge and the VCO frequency is fixed. This happens in steady state.
- Any leakage or mismatch between the up/down currents will cause ripples on the control line and therefore reference spurs to be generated. The charge pump devices are sized to minimize the mismatch.

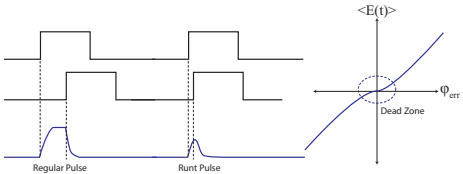
Loop Gain / Closed Loop Gain





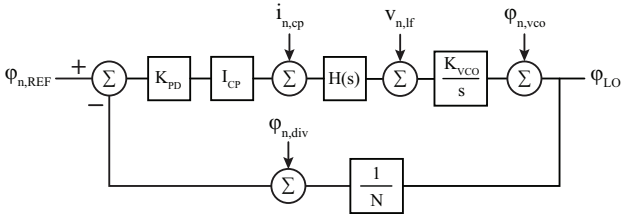
- The overall transfer function is now type-II (two integrators) and third-order. There is always some peaking in the transfer curves.

Charge Pump Runt Pulses



- Assume that the frequency/phase of the divider and reference are nearly matched so that the phase error is small. Ideally a shorter and shorter duty cycle signal would be generated, but as the duty cycle approaches the rise time of the pulses, the pulse amplitude will begin to decay, thus lowering the gain of the PDF. We see that the gain of the PDF flattens for small inputs.
- The solution to this problem is to force the up/down pulses to have a minimum on-time. To produce a small output, therefore, both up and down signals will remain on simultaneously.

Noise Analysis



- Consider a PLL with a charge pump in the loop. Since the gain of the charge pump is $I_{CP} \cdot Z(s)$, and $Z(s)$ is used to realize the loop gain filter, $Z(s) = H(s)$, we now have another knob to tune the loop gain.
- Earlier we derived the transfer function from the input and VCO output ports. The expression is easily modified to include the charge pump

$$STF = \frac{\Phi_{out}}{\Phi_{ref}} = \frac{\frac{K_{PD} I_{CP} K_{VCO} H(s)}{s}}{1 + \frac{K_{PD} I_{CP} K_{VCO} H(s)}{Ns}} = \frac{K_{PD} I_{CP} K_{VCO} H(s)}{s + K_{PD} I_{CP} \frac{K_{VCO}}{N} H(s)}$$

Phase Noise Summary

- As before, the transfer function for the VCO noise is given by (HPF)

$$NTF_1 = \frac{\Phi_{out}}{\Phi_{N,VCO}} = \frac{1}{1 + \frac{K_{PD} I_{CP} K_{VCO} H(s)}{Ns}} = \frac{s}{s + \frac{K_{PD} I_{CP} K_{VCO} H(s)}{N}}$$

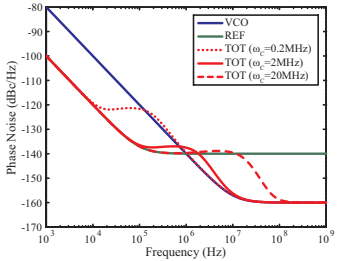
- Since the charge pump is an active circuit, we compute the noise transfer from the CP to the output (LPF)

$$NTF_2 = \frac{\Phi_{out}}{\Phi_{N,CP}} = \frac{H(s)\frac{K_{VCO}}{s}}{1 + \frac{K_{PD} I_{CP} K_{VCO} H(s)}{Ns}} = \frac{K_{VCO} H(s)}{s + \frac{K_{PD} I_{CP} K_{VCO} H(s)}{N}}$$

- The total output noise is given by

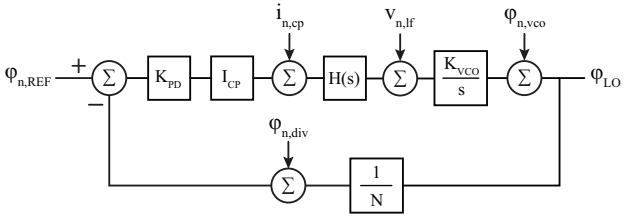
$$N_{out}(s) = N_{ref}(s)|STF(s)|^2 + N_{VCO}(s)|NTF_1(s)|^2 + N_{CP}|NTF_2(s)|^2$$

Phase Noise Spectrum



- The charge pump should be designed to minimize the in-band noise since its transfer function is low-pass. Recall that any mismatch between the up and down transistors also creates a reference spur, which means the devices should be sized and biased carefully.
- The total phase noise profile can be characterized into three regions: (1) Reference noise dominates in the PLL bandwidth, (2) the transition band, and (3) outside the loop bandwidth, where the free-running VCO dominates.

Loop Dynamics



- The transfer function from the input (reference) to the output is given by

$$G(s) = \frac{\phi_{LO}}{\phi_{n,ref}} = \frac{K_{PD} I_{cp} H(s) \frac{K_{VCO}}{s}}{1 + K_{PD} I_{cp} H(s) \frac{K_{VCO}}{s} \frac{1}{N}}$$

- where $H(s) \approx \frac{1}{sC_2}(1 + s/\omega_z)$.

Loop Dynamics (cont)

- The transfer function is therefore

$$G(s) = \frac{K_{PD} I_{cp} \frac{1}{sC_2}(1 + s/\omega_z)\frac{K_{VCO}}{s}}{1 + K_{PD} I_{cp} \frac{1}{sC_2}(1 + s/\omega_z)\frac{K_{VCO}}{s}\frac{1}{N}}$$

$$= \frac{K_{PD}\frac{I_{cp}}{C_2}(1 + s/\omega_z)K_{VCO}}{s^2 + K_{PD}\frac{I_{cp}}{C_2}K_{VCO}\frac{1}{N}(1 + s/\omega_z)}$$

- Focusing on the denominator, we can put it into standard second order from

$$D(s) = s^2 + (s/\omega_z)K_{PD}\frac{I_{cp}}{C_2}K_{VCO}\frac{1}{N} + K_{PD}\frac{I_{cp}}{C_2}K_{VCO}\frac{1}{N}$$

$$= s^2 + \frac{s\omega_0}{Q} + \omega_0^2$$

Loop Natural Frequency and Quality Factor

- By equation the above two equations, we have

$$\omega_0 = \sqrt{K_{PD}\frac{I_{cp}}{C_2}K_{VCO}\frac{1}{N}}$$

- The amount of ringing in the loop depends on the Q value. The Q is given by

$$\frac{\omega_0}{Q} = \frac{\omega_0^2}{\omega_z}$$

- or

$$Q = \frac{\omega_z}{\omega_0}$$

- The location of the zero controls the stability of the loop

Location of Poles

- The poles are found easily since it's a second order transfer function

$$s_{1,2} = \frac{\frac{-\omega_0}{Q} \pm \sqrt{\left(\frac{\omega_0}{Q}\right)^2 - 4\omega_0^2}}{2}$$

- To realize an undamped system (real poles), the $Q < 1/2$. Otherwise there will be jitter peaking in the transfer function.

"Critically Damped" System

- If we take $Q = 1/2$, we have two poles at

$$s_{1,2} = \frac{-\omega_0}{2Q} = -\omega_0$$

- The location of the zero is $\omega_z = Q\omega_0 = 0.5\omega_0$. The overall transfer function is given by

$$G(s) = G(0)\frac{1 + 2s/\omega_0}{(1 + s/\omega_0)^2}$$

- Due to the zero, the system still overshoots slightly and the loop bandwidth is given by $\omega_{-3dB} \approx 2.5\omega_0$.

Underdamped System

- To ensure a damped response, one may choose $Q \ll 1$, say $Q = 0.1$, which implies a very low frequency zero, $\omega_z = Q\omega_0$. This requires a large capacitor!
- A useful approximation for a low Q system is the following

$$s^2 + \frac{s\omega_0}{Q} + \omega_0^2 \approx (s + \frac{\omega_0}{Q})(s + Q\omega_0)$$

- The utility of this approximation is that the second pole is at the zero frequency $\omega_z = Q\omega_0$, which cancels the zero in the transfer function

$$G(s) = \frac{K_{VCO}K_{PD}\frac{I_{cp}}{C_2}(1 + s/\omega_z)}{(s + \frac{\omega_0}{Q})(s + \omega_z)}$$

$$G(s) = \frac{K_{VCO}K_{PD}\frac{I_{cp}}{\omega_z C_2}(1 + s/\omega_z)}{(s + \frac{\omega_0}{Q})(1 + s/\omega_z)}$$

Underdamped System (cont)

- The overall transfer function simplifies and acts like a single pole system

$$G(s) = \frac{K_{VCO} K_{PD} \frac{I_{cp}}{\omega_z C_2}}{(s + \frac{\omega_0}{Q})}$$

- The pole is given by

$$\omega_{-3dB} = \frac{\omega_0}{Q} = \frac{1}{Q} \sqrt{K_{PD} \frac{I_{cp}}{C_2} K_{VCO} \frac{1}{N}}$$

- Keep in mind that this is an approximation and in reality the pole/zero don't cancel exactly. Also we neglected the higher order pole of the lead/lag filter. There are more poles in the system as well ... simulate to be sure !

Choice of Loop Bandwidth

- Even though we modeled the PLL as a continuous time system, in reality most implementations are a discrete time system. This is due to the fact that the PDF compares edges of the reference to the divided clock, and only generates an error signal once per reference edge.
- One implication of the discrete time system is that the bandwidth must be smaller than the reference frequency, typically 1/10'th of the reference is a popular choice.
- XTAL oscillators are available up to a few hundred megahertz. In an Integer-N architecture, the reference frequency is set to the channel spacing, which means the loop dynamics are controlled by the reference frequency. Accurate synthesizers are therefore slow.
- A fractional-N synthesizer in theory decouples the choice of reference frequency from the resolution of the PLL, but in practice fractional spurs force low bandwidths. Realization of a high bandwidth fractional-N PLL is an active research topic.

Simulation Tools

- These equations are a good starting point in the design of a PLL. The next step is a system level simulation in matlab or an analysis with the complete transfer function.
- Next, you should remind yourself that our linear model is an approximation.
- A simulation framework that can model the actual dynamics, including the non-linearity, is very important. Full SPICE level simulation is too slow (hours to days) for design, but is a must for verification.
- Verilog-A is a great choice to model the PLL, and even include some of the blocks at the transistor level.

CppSim

- A great free tool that runs very fast (C++ based platform) and includes support for verilog components is available and highly recommended: `cppsim.org`