EECS 142 Laboratory #2

High Frequency Passive Components

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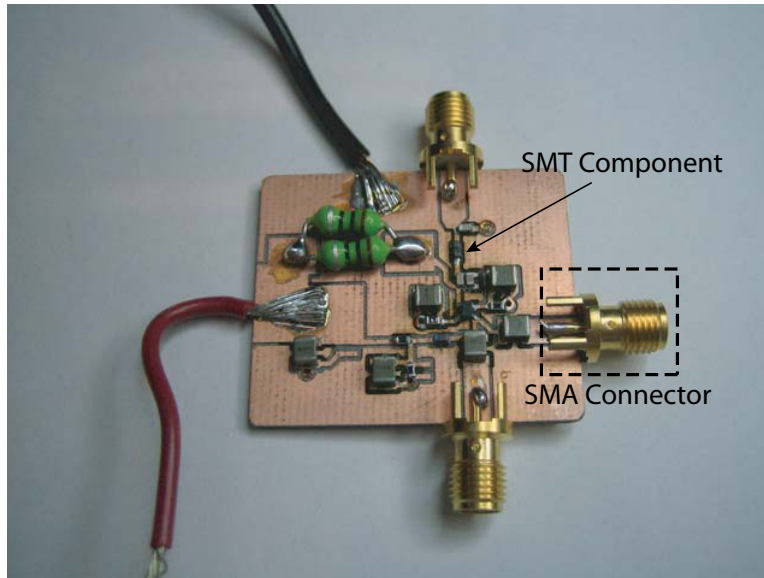February 7, 2025

Figure 1: An RF mixer PCB fabricated by a 142 student.

1 Introduction

Passive components play an important role in RF and microwave circuits. For instance, inductors are commonly employed to tune out the capacitance of transistors by forming resonant circuits. Inductors and capacitors together are used to build filters and impedance matching circuits. In communication circuits filtering and matching are important functions for attenuating unwanted signals while maximizing the gain of desired frequencies. Unfortunately there are no ideal inductors, capacitors, or resistors, and the unwanted characteristics of these components are called parasitics. In this laboratory you will learn about the high frequency parasitics associated with passive components. These parasitics add loss and limit the upper frequency range over which the components function properly.

2 PCB Manufacturing

All circuits will be fabricated using a simple two-layer printed circuit board (PCB). The PCB consists of a dielectric material, usually FR4 ($\epsilon_r = 4.4$), with a thickness of 62 mils[1], and two layers of Cu metal layer. The metal layers have a thickness of 34 μm. Normally you would pattern the metal layers to produce your circuit but in the interest of time, the boards have been prefabricated to take on a standard form. The backside of the board is a solid ground plane. Connections to ground must travel through a "via" to reach the backside.

A typical board is shown in Fig. 1. The input and output of the board have footprints for SMA connectors which allow you to connect SMA cables[2]. The input and output microstrip

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[1]1 mil = .001 inch = 25.4 μm

[2]SMA stands for SubMiniature version A, a connector for coaxial cables with 50Ω impedance and good performance up to 18GHz

transmission lines are interrupted periodically which allows you to place components in series or in shunt. Landing pads with vias to ground also appear periodically to allow shunt components to be soldered to ground.

To solder components onto the board, use standard 0603 components[3] in series or in shunt. Use a sharp solder needle and a microscope to do the soldering. If you are new to soldering surface-mount components, you should consult the following web page: `http://www.geocities.com` A PDF copy of this web-page is also stored on the class website. A short on-line video is available if you are soldering surface-mount components for the first time.
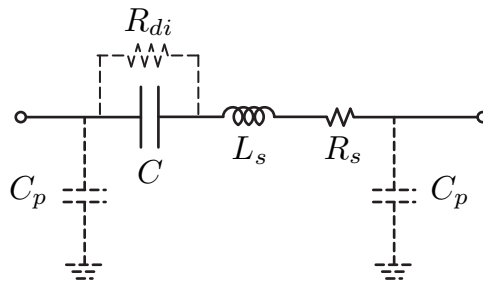
3 Lumped Passive Components

Figure 2: The lumped equivalent circuit model for a real soldered capacitor.

Up to now you have probably simulated your circuits with ideal passive components (inductors, capacitors, resistors), but real circuit components are far from ideal. Consider, for instance, a capacitor, which has an equivalent circuit model shown in Fig. 2. The model has many parasitic components which only become relevant at high frequencies. A plot of the impedance of the capacitor, shown in Fig. 3, shows that in addition to the ideal behavior, the most notable difference is the self-resonance that occurs for any real capacitor. The self-resonance is inevitable for any real capacitor due to the fact that as AC currents flow through a capacitor, a magnetic field is also generated by the capacitor, which leads to inductance in the structure. This inductance is exacerbated by the leads of the capacitor, which often dominate the inductance. The inductive parasitics are lumped into a single inductor L_s in series with the capacitor. The finite conductivity of the plates and the leads also results in some series loss, modeled by R_s (sometimes labeled *ESR*, or effective series resistance). Unless a capacitor is fabricated in a vacuum, the dielectric material that separates the plates also has loss (and resonance), which is usually modeled by a large shunt resistance R_{di}. Furthermore, when a capacitor is soldered onto a PCB, there is parasitic capacitance from the solder pads to the ground plane, resulting in the capacitors C_p in the equivalent model.

In a like manner, every inductor also has parasitics, as shown in the equivalent circuit model (Fig. 4), which limit operating frequency range. The series resistance R_x is due to

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[3]Components are classified according to their footprint size in mils, or in this case 0.060 inches by 0.030 inches.
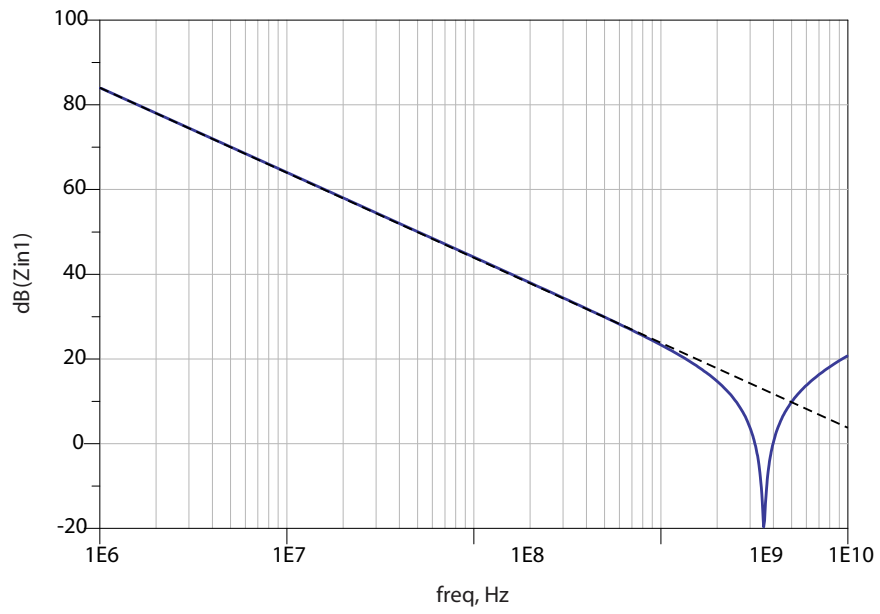
Figure 3: The magnitude of the impedance of a real capacitor (the dashed line shows the ideal behavior).
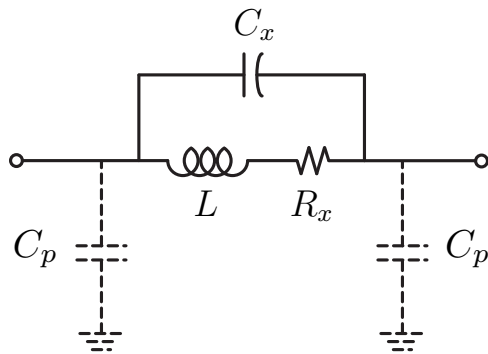

Figure 4: The lumped equivalent circuit model for a real soldered inductor.

the winding resistance and the capacitance C_x models the distributed turn-to-turn capacitance of the structure in a lumped element. The element self resonates at a frequency of approximately $1/\sqrt{LC_x}$ and has a quality factor $Q = \omega L/R_x$. When the inductor is soldered onto the PCB, there is an additional capacitance to ground modeled by C_p, which lowers the self-resonant frequency to $1/\sqrt{L(C_x + C_p/2)}$.

4   Board Parasitics

In addition to the component parasitics, you will find that there are significant parasitics associated with the PCB. When you solder a component in series with a lead, the placement of the component relative to the ground plane will affect the inductance and capacitance of the component. Likewise, when you solder a component to ground, the effect of the via path will affect the inductance. Traces between components can be modeled as LC circuits at low frequencies if the length of the trace is much shorter than the wavelength ($\ell \ll \lambda$). For example, ideally a short circuit should have zero impedance but as the measurements will show, there is a finite amount of inductance and resistance below the self-resonant frequency. When a component is soldered to ground, there is additional inductance and resistance associated with the via to the ground plane. It is important to realize that the ground plane itself contributes resistance, especially at higher frequencies when the current flow is non-uniform and flows in the proximity of the transmission lines. As explained in more detail in the next section, the "inductance" of the components is strongly related to the "return current", or the path of the current flow under the component. If the ground path beneath the component is interrupted, forcing the current to flow away from the component, the parasitic inductance increases considerably.

4.1   Component Specifications

Inductors and capacitors are often described in terms of the (1) inductance/capacitance at a particular frequency, (2) Quality factor and (3) self-resonant frequency (SRF). The inductance/capacitance varies due to the non-ideal behavior of the component. For instance, the intrinsic inductance may vary with frequency due to non-uniform current flow (current crowding) at high frequencies. More prominently, though, the inductance/capacitance varies due to the complex parasitics associated with the component. Instead of specifying the equivalent circuit model, many manufacturers simply specify these two or three numbers. If the components are used well below their self-resonant frequency, these three numbers may be sufficient to characterize the structure.

The quality factor (Q) is very important in RF circuits, since it ultimately limits the performance of amplifiers, filters, and other circuits. At frequencies well below resonance, the Q factor is given by

$$Q = \frac{|X_{L|C}|}{R_x}$$

where $X_{L|C}$ is the reactance of the component at a given frequency and R_x is the effective series resistance (ESR) of the component. In fact, instead of Q, the ESR may be given. It's important to note that Q is a function of frequency.
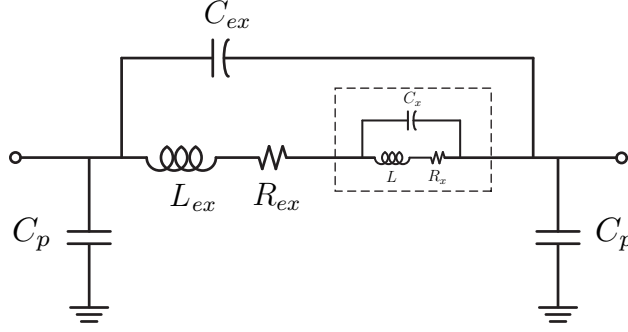
Figure 5: The lumped equivalent circuit model for an inductor includes *extrinsic* and *intrinsic* parasitic components.

The self-resonance is determined by the parasitics in the structure, and when a manufacturer of a component specifies this value, it's difficult to know what they mean! For instance, for a capacitor the series inductance is a strong function of how the component is used and the leads of the capacitor will determine the resonance frequency. One can only guess how the component was characterized. For instance, if a 0603 capacitor is measured as a two-port circuit using transmission line leads, then inductance is a strong function of the characteristic impedance of the line Z_0 (see below). It is therefore advisable to measure the self-resonance frequency of the component for the application at hand using the actual structure/leads employed in the design.

4.2   The Origin of Component Parasitics

As we discussed, the parasitics of a non-ideal inductor shown in Fig. 4 includes series loss R_x, a "winding" capacitance C_x, and parasitic capacitance C_p. These parasitics arise from two sources: (1) Intrinsic parasitics related to the way the inductor is physically constructed and (2) Extrinsic parasitics resulting from the way the component is soldered on the PCB substrate. In the case of integrated circuit (IC) inductors, the same parasitics arise, but the extrinsic parasitics are related to the Si substrate as opposed to the PCB substrate. In Fig. 5 we divide the equivalent circuit into the intrinsic and extrinsic portion.

The intrinsic losses can be understood by examining a typical solenoidal air-core inductor used for RF applications (Fig. 6). Since the wire has resistance, the inductor winding must include a series resistance, a component of R_s in the equivalent circuit model. Likewise, since the windings of the inductor come in close proximity, at very high frequencies signals can skip the loop and travel directly from winding to winding through the intrinsic capacitance between the windings. This is especially true at high frequencies when the potential difference between the windings increases ($V_{diff} \propto \omega L_w$). The effect of the interwinding capacitance is modeled by the capacitor C_x in the equivalent circuit model. In reality the interwinding capacitance is distributed non-uniformly throughout the structure and a more sophisticated model, shown in Fig. 7, can be used to capture the complex impedance of the structure more accurately. In practice, though, this is not necessary as long as we employ the inductor well below its *self-resonant frequency* (SRF), ω_0. The SRF is defined as the frequency when the
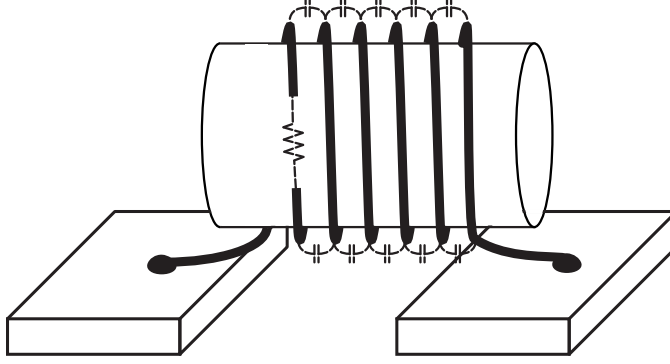
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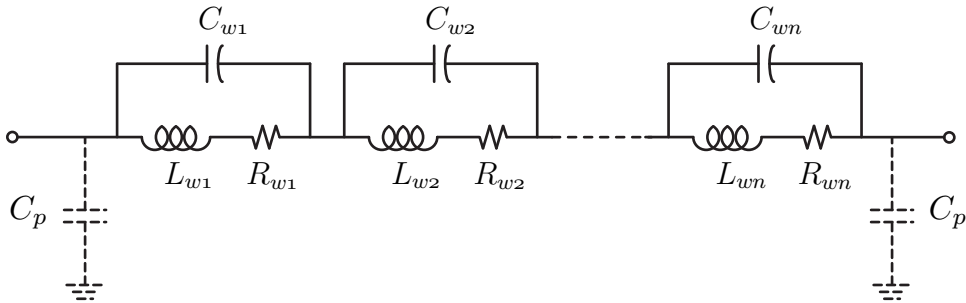Figure 6: A solenoidal "air-core" high frequency inductor geometry.

Figure 7: Distributed model for a solenoidal inductor.

imaginary portion of the inductor impedance $Z_L(\omega_0)$ reaches to zero, $\Im(Z_L(\omega_0)) = 0$. Above this frequency the inductor begins to behave like a capacitor, as more energy is stored in the fields of electric field rather than the magnetic fields. This occurs because the signal is bypassing the windings in favor of the capacitive coupling mechanism described earlier.

When an inductor is used in any real circuit, it must be connected to other components through leads, as shown in Fig. 8. Here we see that pads on the PCB trace are used to solder the leads of the inductor to the PCB substrate. If we define the interface points to the inductor at A and B, we clearly can see that capacitors C_s are needed to model the pad capacitance to the substrate, since the back-side of the substrate is usually a ground plane. Even though the leads A and B are relatively far away, a small electrical fringing field can couple these points as shown in Fig. 9. The presence of the ground plane greatly reduces this coupling capacitor C_f, but as components are reduced in physical size or if the substrate thickness is made larger, this coupling increases.

While these pad capacitors are easy to understand, the concept of lead inductance is much more difficult to explain. Recall that the inductance of any structure is defined for a *closed* loop. Reference points A and B are physically removed, so the inductance between points A and B must include a "return path" for the current. Imagine connecting voltage sources at points A and B as shown in Fig. 10. Now we can see that current flows in a loop by flowing through the ground plane between points A and B. This loop stores magnetic energy and thus has a inductance L_{lead}, which we lump into the leads of the inductor in the
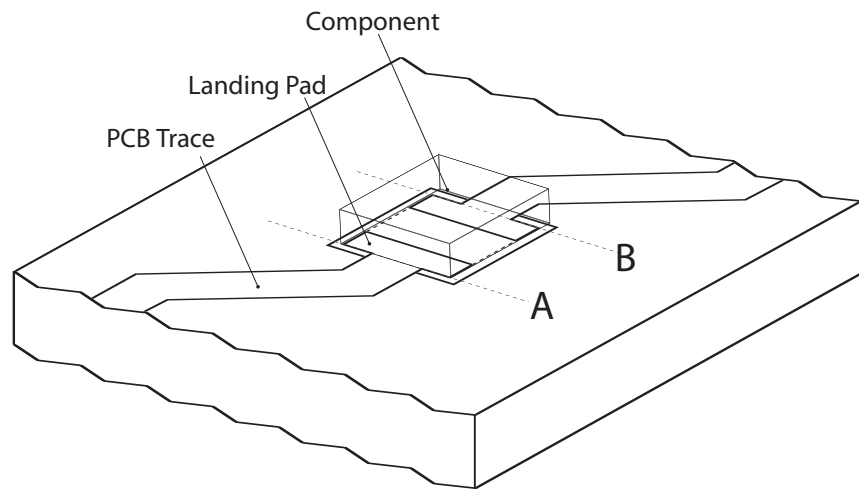
Component

Landing Pad

PCB Trace

B

A

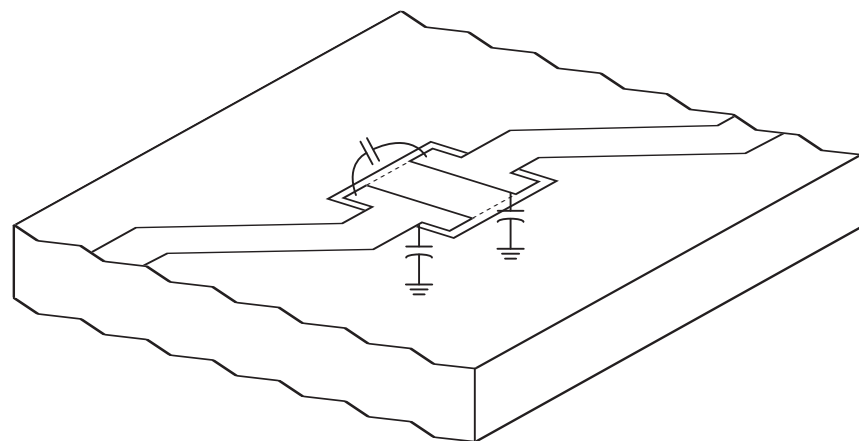Figure 8: The layout of an inductor on a PCB substrate includes landing pads and leads.

Figure 9: The capacitance between the landing pads includes a coupling capaictor due to the fringing fields between the leads of a component.
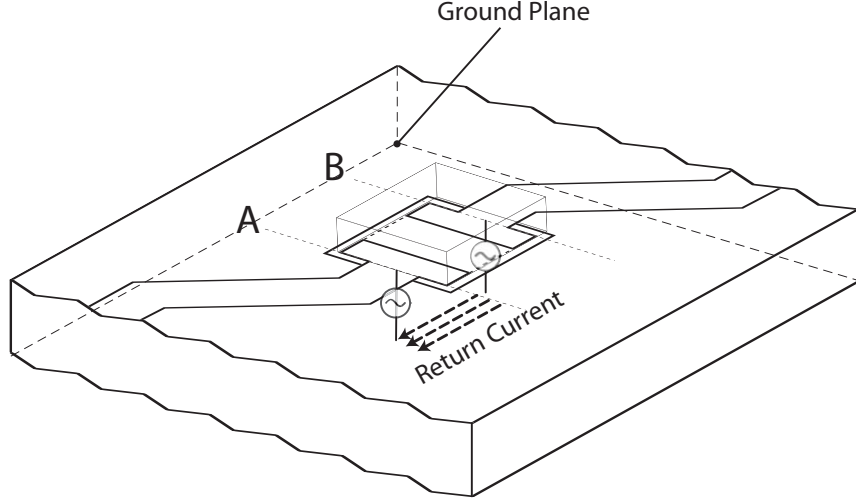
Figure 10: The return current in a PCB inductor flows through the ground plane.

equivalent circuit model. It is important to realize that to first order this lead inductance is independent of the inductance of the component inductor since the current flows through the same path regardless of the value of inductance L_w. In fact, if we short out the path between A and B, we still experience the lead inductance L_{lead}. We therefore augment the equivalent circuit model to account for this extra *extrinsic* inductance in the component, which is a function of the layout of the component rather than the component itself. Since traces on the PCB also incur additional loss, an extra resistance R_{lead} has been added to the model as well.

For integrated circuits the same considerations apply with a couple of small minor adjustments. A typical integrated inductor is made in spiral form, as shown in Fig. 11. Interwinding resistance and coupling capacitance occur as well, but the substrate is usually quite thick compared to the dimensions of the spiral. Typically the substrate is $700\mu m$ thick. The back of the substrate is not always an ideal ground plane (sometimes a non-conductive glue is used to attach the die to the package) and the return current signal path is actually on the surface of the substrate through metal layers. Since these surface leads can be made very close to the inductor, the lead inductance can be reduced significantly. In Fig. 12, the leads are routed in such a manner as the close the loop, effectively producing a one-port structure. The most important complication for integrated inductors, though, arises from the capacitive coupling through a doped Si substrate (conductivity varies but a good typical value for modern process is about 10 $\Omega - $cm), which is modeled by including a series resistance R_{sub} in the equivalent circuit model shown in Fig. 13. It is important to note that depending on the thickness and conductivity of the substrate, the coupling between the leads of the inductor through the substrate changes significantly. An extra resistance $R_{s,2}$ models the signal coupling through the substrate. The extra substrate capacitors model the displacement current flow in Si.

It is now easy to see that all the (extrinsic and intricsic) inductance can be lumped into a single inductor L_x, while all the resistance is lumped into R_x. The simpler model shown
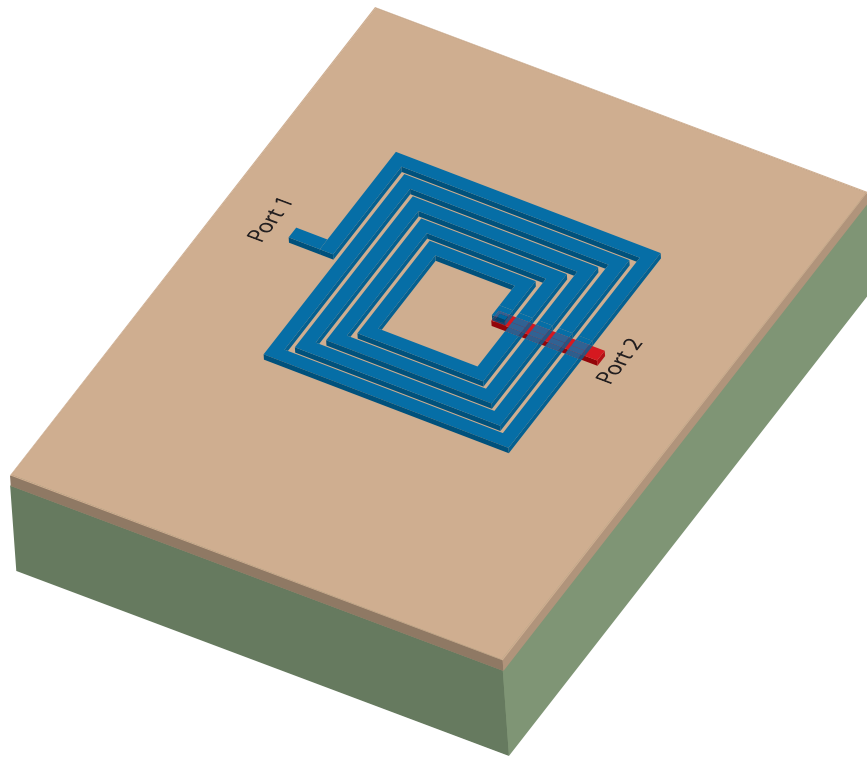
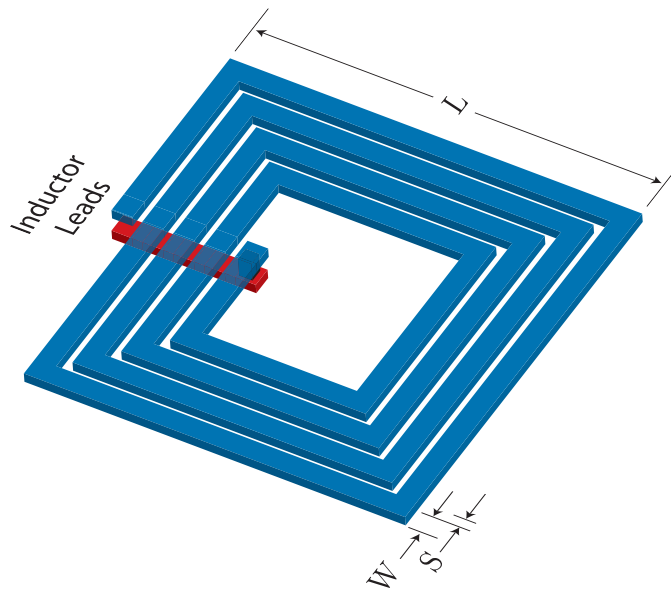Figure 11: The layout of an on-chip spiral inductor (two-port structure).

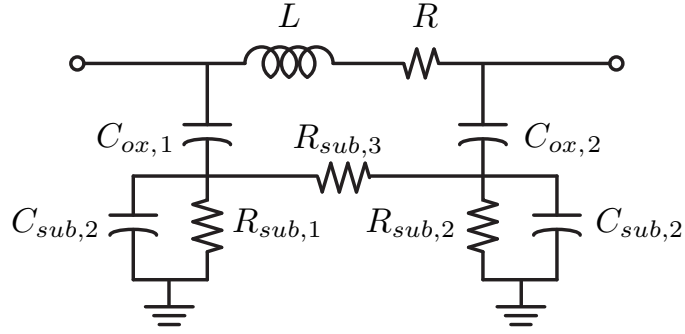Figure 12: The layout of an on-chip spiral inductor (one-port structure).

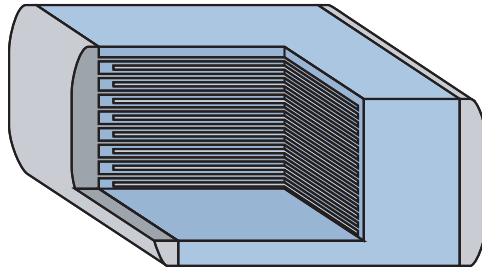Figure 13: The model for an on-chip inductor with a lossy substrate.

Figure 14: The physical layout of a surface-mount capacitor. (Source: Wikipedia)

in Fig. 4 is thus adequate for capturing the high frequency behavior of the component if it is employed well below the self-resonant frequency. Near or above the SRF, the component is dominated by distributed behavior and a simple lumped circuit cannot capture the behavior.

It is now clear that other components can be similarly divided into intrinsic and extrinsic parasitics. For instance, a large capacitor is physically manufactured by sandwiching several plates and stacking or rolling the plates to realize a large capacitance in a small volume (Fig. 14). For RF applications, many capacitors are made by using a flat parallel plate structure called a metal-insulator-metal (MIM) capacitor. A very thin insulator is used to maximize the capacitance between the plates. In IC process, lateral or flux capacitors use
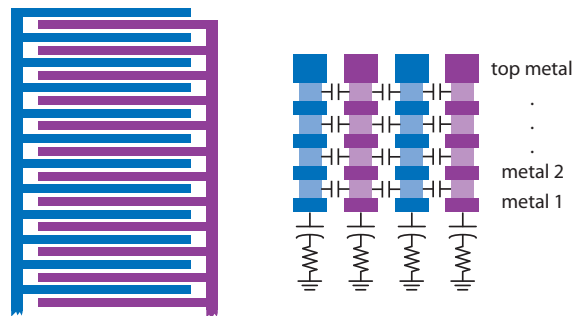

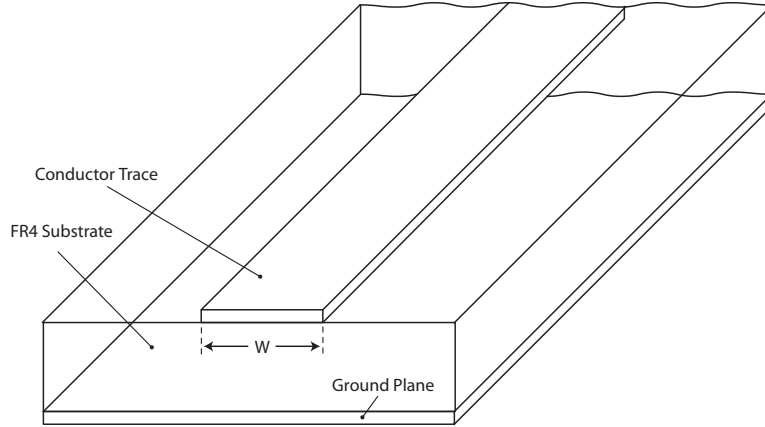Figure 15: A MIM "finger" capacitor layout.

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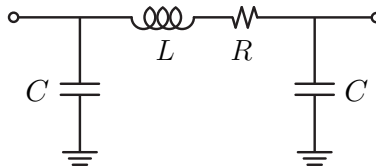Figure 16: A microstrip transmission line formed on a PCB substrate.

Figure 17: An equivalent circuit for a short section of transmission line.

small interdigitated fingers to realize a high capacitance between the leads of the capacitor (Fig. 15). Due the materials employed in the construction of the capacitor, we model the lead series resistance as R_s. The inductance of the capacitor is due to the magnetic energy storage in the structure when we connect a voltage source between the leads and measure the AC current flow into the structure. At high frequencies we find that the reactive portion increases and crosses zero at the self-resonant frequency. This behavior is modeled by L_s. The value of L_s is very dependent on how we connect the leads. If the component is placed on a PCB substrate, then the lead inductance is defined by the return current loop formed by the ground plane as shown in Fig. 10. As before, we account for the lead capacitance by adding C_p to the model.

4.3   Calculation of Component Parasitics

It is useful to estimate the parasitics of a component by using some simple assumptions. A very common layout technique in RF PCB circuits is the microstrip configuration shown in Fig. 16. Here the leads of the component are connected through "landing" pads (large enough for the component to fit), which may be larger than other traces used in the circuit. If we assume that the current flows along the width of the landing pad, and assuming there is a ground plane underneath the structure, we can model the component as a transmission line of length ℓ and characteristic impedance Z_0. This impedance can be calculated using standard tables or approximate equations (online tools are also available) once the the width and height of the line are specified.

From transmission line theory, the equivalent circuit for a short section of transmission line $\ell \ll \lambda$ is given by Fig. 17, where λ is the quasi-TE mode propagation wavelength in the PCB. If the dielectric constant of the PCB is much larger than air, then the speed propagates mostly in the medium with a velocity $v = c/\sqrt{\epsilon_r}$. More accurate values of v can be obtained from approximate equations or tables. The component values are calculated as follows

$$\omega L \approx Z_0 \beta \ell = Z_0 2\pi \frac{\ell}{\lambda}$$

$$\omega C \approx \frac{1}{2} Y_0 \beta \ell = Y_0 \pi \frac{\ell}{\lambda}$$

At 1 GHz the wavelength in free-space is 30 cm, and in the PCB it's 15 cm. An 0603 component is only 60 mils, or about 1.6 mm, which is only 11% of the wavelength. Therefore our lumped circuit model for the transmission line is reasonably accurate. Assuming $Z_0 = 50\Omega$, then the inductance is approximately given by $L_{TL} = 0.5$ nH. If the landing pads doubles the length of the structure, the parasitic inductance is about 1 nH. The parasitic capacitance is $C_{TL} = 11$ fF.

If the length approaches a significant fraction of wavelength, then a more accurate model can be employed. The Y parameters of the transmission line is given by

$$Y_{11} = Y_{22} = Y_o \coth(\gamma \ell)$$

$$Y_{12} = Y_{21} = -Y_0 \operatorname{csch}(\gamma \ell)$$

where $\gamma = \alpha + j\beta$ is the complex propagation constant (including loss). The complex hyperbolic functions can be calculated by

$$\coth(\gamma \ell) = \frac{\cosh(\alpha \ell)\cos(\beta \ell) + j\sinh(\alpha \ell)\sin(\beta \ell)}{\sinh(\alpha \ell)\cos(\beta \ell) + j\cosh(\alpha \ell)\sin(\beta \ell)}$$

$$\operatorname{csch}(\gamma \ell) = \frac{1}{\sinh(\gamma \ell)} = \frac{1}{\sinh(\alpha \ell)\cos(\beta \ell) + j\cosh(\alpha \ell)\sin(\beta \ell)}$$

5 The Network Analyzer

In this class, you'll make extensive use of a network analyzer. A typical Network Analyzer is shown in Fig. 18. This instrument is also called a VNA, or Vector Network Analyzer, to emphasize the complex nature of the measurements (as opposed to scalar). Simply stated, a network analyzer measures the N-port response of circuit over a specified frequency range. Most network analyzers are designed to measure two-port devices, since most filters, amplifiers, and other RF building blocks are two-ports. If only 1 port is used, then the network analyzer can measure the 1-port response, or the impedance of the device under test.

Network analyzers incorporate directional couplers to decompose the voltages in each port into "incident" and "reflected" waves. The ratio between these waves is directly related to the scattering or S-parameters of the device. Inherently, therefore, the network analyzer is measuring the S-parameters of the device under test. The S- parameters are easily converted into other parameter sets, such as impedance (Z) or admittance ($Y = Z^{-1}$) parameters.

Figure 18: A Network Analyzer (Agilent E5071C ENA RF Network Analyzer).

The measurements made by a network analyzer can be saved and exported as an SNP file format, where N is the number of ports used in the measurement. Typically you will be saving S2P files. The S2P file is an ASCII file format that is easy to read and import into other programs. Most CAD tools such as ADS and SpectreRF can read these files.

In this lab you will be estimating the parasitics of 0603 components by using the "port extension" feature of the Agilent network analyzer. The reference plane for the measurement can be moved from the SMA connectors to the point where the device is connected. To do this you will need to measure an "open" and "short" as shown in Fig. 19 (include the loss) and the network analyzer will automatically calculate the phase delay and loss associated with the input and output transmission lines. Using this configuration, you can measure the parasitics of a component in series or in shunt using the test boards shown in Fig. 20. For instance, you can measure the two-port parameters of a zero-ohm resistor when in series or shunt with the signal path.

The shunt components should be measured separately to include the effect of the via ground. Using the parasitics of a zero-ohm resistor allows you to to estimate the effect of the component parasitics due to the board layout. Alternatively, you can also measure the actual performance of the lumped components (inductors, capacitors) and model the component loss and resonance with an appropriate equivalent circuit.

Before performing measurements using a VNA, you need to calibrate the instrument. This is needed since the internal directional couplers are non-ideal. Calibration also allows you to move the reference plane of the measurement to the tips of the cables. Manual calibration involves connecting a set of standards to the VNA (opens, shorts, thrus, loads, etc.) step by step. An E-Cal kit has all the standards built-in and the VNA will automatically perform the calibration in one step. To get consistent and accurate results, use the torque wrench to connect the cables to the VNA and the board.

6 Prelab

If you do not have experience soldering, begin by watching the soldering tutorial video. Watch this video before and after soldering for best results. There is also a video tutorial on using the network analyzer.

1. Calculate the AC impedance of a lumped inductor modeled by Fig. 4. Plot the impedance with component values: $L = 5$ nH, $R_x = 1.15\Omega$, $C_p = 400$ fF, $C_x = 10$ fF.

    (a) Compare the impedance to an ideal inductor by overlaying their plots on a log scale. Also plot the effective inductance of the structure ($\Im(Z_{ind})/\omega$) as a function of frequency.

    (b) Over what frequency range does the inductor behavior appear close to ideal behavior?

    (c) What is the self-resonant frequency (SRF) of the inductor? You can calculate the SRF using the simplified equivalent LC circuit.

    (d) What is the effective inductance near resonance? After the self-resonance frequency, how would you describe the inductor behavior?

    (e) Over what range of frequency is the inductor a high Q component?

    (f) (Optional) Plot the S_{11} and S_{12} of the inductor on a Smith Chart from DC to 10 GHz. Vary the component parasitics and observe the behavior on the Smith Chart. Make sure you qualitatively understand the plots.

2. Suppose that the inductor model in the previous section is actually an air-core inductor made of 5 windings. Simulate a distributed model of the inductor by assuming that the L and C_p are uniformly distributed from turn-to-turn. Compare the frequency dependent impedance of the distributed model with the simple model. Over what frequency range is the simpler model adequate?

3. Calculate the AC impedance of a lumped capacitor modeled by Fig. 2a. Plot the impedance with component values: $C = 5$ pF, $R_x = 0.25\Omega$, $L_s = 0.75$ nH, $C_p = 20$ fF.

    (a) Compare the impedance to an ideal capacitor by overlaying their plots on a log scale.

    (b) Over what frequency range does the capacitor behavior appear close to ideal behavior? Plot the effective capacitance seen from terminal to termianl and compare to the low frequency value. Up to what frequency can you employ this capacitor if you cannot tolerate a deviation by more than 10%.

    (c) What is the self-resonant frequency of the capacitor? What is the effective value of capacitance very close to resonance?

    (d) Over what range of frequency is the capacitor a high Q component?

    (e) (Optional) Plot the S_{11} and S_{12} of the capacitor on a Smith Chart from DC to 10 GHz. Vary the component parasitics and observe the behavior on the Smith Chart. Make sure you qualitatively understand the plots.

Figure 19: (a) Open and (b) short structures used for the automatic port extension feature of the network analyzer.
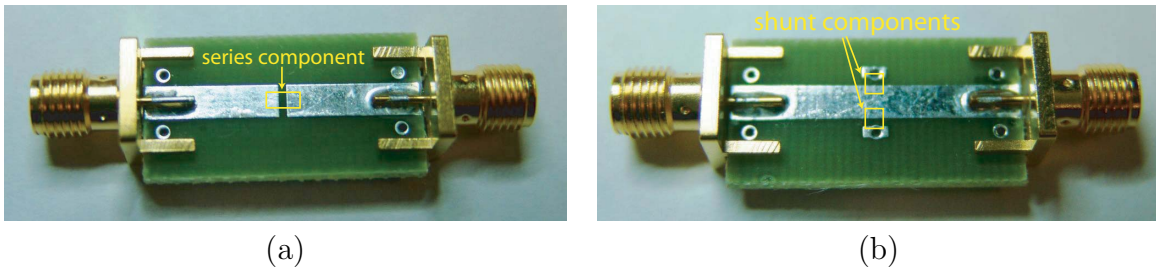

Figure 20: Structures used to estimate the board level parasitics. (a) An "open" structure allows a component to be soldered in series and characterized. (b) Shunt components can be soldered to ground to characterize components soldered in this configuration. In each case a zero ohm resistor can be used to estimate the series/shunt inductance.

7   Experimental Work

7.1   Procedure

1. Make sure the Network Analyzer is calibrated correctly. You can perform the calibration with the E-Cal Kit or simply recall the calibrated setting from memory. The GSI can assist you with this step.

2. Solder the SMA leads to a the "open" and "short" PCB (Fig. 19) and use the port extension feature to move the reference plane to the device under test (DUT).

3. Measure and save the scattering parameters of a "thru" structure (the board with soldered SMAs is available from the GSI). Name the output file 'thru.s2p'. Since the size of the "thru" transmission line matches the size of the component, you can use this measurement to estimate the parasitics of the component on the PCB substrate. You can use a pre-soldered "thru" board to solder SMA leads to the "shunt component" board (Fig. 20b), which you will use later.

4. Measure and save (S2P) the scattering parameters of the "shunt short" structure ('shuntshort.s2p'). Since this structure is symmetric, you only need to measure it as a 1-port but it is interesting to measure the transmission properties to note that

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the shunt short does not perfectly reflect the incoming signal. This structure can be used to estimate the parasitics of a component soldered to ground (and it includes the extra via to ground parasitics).

5. Next measure the two-port S-parameters of a zero ohm resistor connected in series (Fig. 20a) and name the file 'zero_ohm_series.s2p'. Note that an ideal zero ohm resistor would produce no reflection ($S_{11} = S_{22} = 0$) and perfect transmission ($S_{12} = S_{21} = 1$). Any deviation from this ideal performance can be attributed to the parasitics of this component. Save the S2P file for this measurement.

6. Now measure the two-port S-parameters of a zero ohm resistor to ground soldered in shunt ('zero_ohm_shunt.s2p'), as shown in Fig. 20b. Only solder one component to ground (you can place up to two components on the board). Note that an ideal zero ohm resistor to ground would produce a perfect reflection ($S_{11} = S_{22} = 1$) and zero transmission ($S_{12} = S_{21} = 0$). Any deviation from this ideal performance can be attributed to the parasitics of this component. Save the S2P file for this measurement.

7. To avoid wasting a board (and to match the port extension)[4], de-solder the zero ohm resistor and replace it with an inductor with $L < 10$ nH. Measure the inductor in series and shunt. Save both S2P files as 'ind_series.s2p' and 'ind_shunt.s2p'.

8. Using the Network Analyzer, measure the magnitude and phase response of the impedance of the 1-port structure (component soldered to ground). Adjust the resolution to clearly capture the component response on a log scale. Estimate the inductance and resistance of a "shunt short" directly.

9. Repeat the last two steps with a capacitor component with $C < 10$ pF. To avoid wasting a board (and to match the port extension), re-use the same board by de-soldering the inductor. Name the files 'cap_series.s2p' and 'cap_shunt.s2p'.

10. Using the highest frequency VNA in the lab, measure one of your components up to 8.5 GHz. Name the file 'cap_series_hf.s2p' and 'cap_shunt_hf.s2p' (or 'ind').

8 Post Laboratory

1. Using the measurements on the "thru" structure, calculate the equivalent circuit for the short section of transmission line. You can do this by converting the S parameters to Y parameters and then forming a Π circuit. You can refine this model by matching the measured S parameters to the model results (use the optimizer in ADS or use optimization).

2. Compare the component values of the equivalent circuit to calculated component values based on transmission line theory.

3. Repeat the above steps for the "short to ground", zero-ohm shunt and series components. Estimate the extra inductance due to the via structure.

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[4]SMT components are very inexpensive (cents) whereas low volume custom PCBs are expensive!

4. Compare the measurements and models of the zero-ohm structures to the short structures. Explain any differences or similarities. Generate S-parameter plots (mag/phase/Smith) of measurements versus model.

5. Use the above steps to create models for the capacitor and inductor component. Generate S-parameter plots (mag/phase/Smith) to compare the measurements to the modeled components.

6. Create models of the shunt/seires inductor/capacitor directly from measurements from the zero-ohm resistor structures by using the manufactured component value and the extrinsic parasitics. How close is the *a priori* model compared to the *a posteriori* model? This is an important step since it avoids creating custom models for every component. Compare the results qualitatively and qualitatively using plots of S-parameters (mag/phase/Smith).

7. Using the high frequency measurements, compare the model to measurement results. Up to what frequency do you trust your model? Plot S-parameters (mag/phase/Smith).

8. Your final lab write up (PDF format) should be easy to read and summarize all of your pre-lab and post-lab results. Please do not paste several plots together and expect us to understand the order and logic behind your results. Include a coherent write-up, clearly drawn or computer generated schematics of your models and plot comparisons between model and measurements. Include all the measured S-parameters (mag/phase/and Smith Chart format) and compress the file and upload it to the class submission site (use ZIP or a gzip'ed tar ball)

9. How much time did you spend on this lab? Any feedback is appreciated.

9   References

Check online for sites that discuss SMT, PCB manufacturing, Network Analyzers, for instance in the *RFCafe* website. Another good source is Wikipedia, search the terms 'capacitor', 'inductor', and 'surface mount technology'. Documentation on the Network Analyzer is available in the lab and on the class website. Also refer to Agilent's online documentation.