Differential Amplifiers

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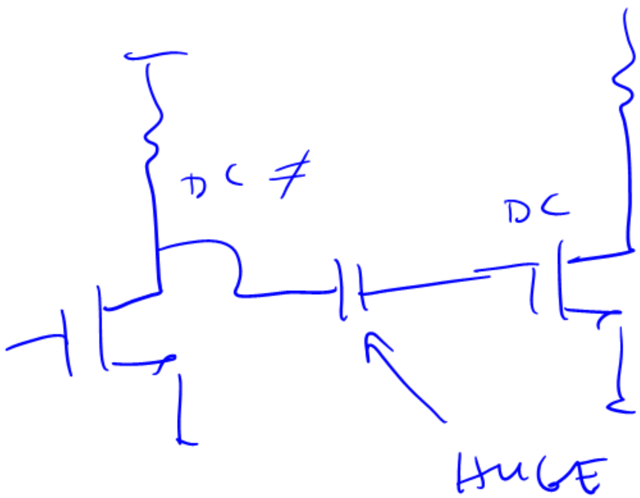
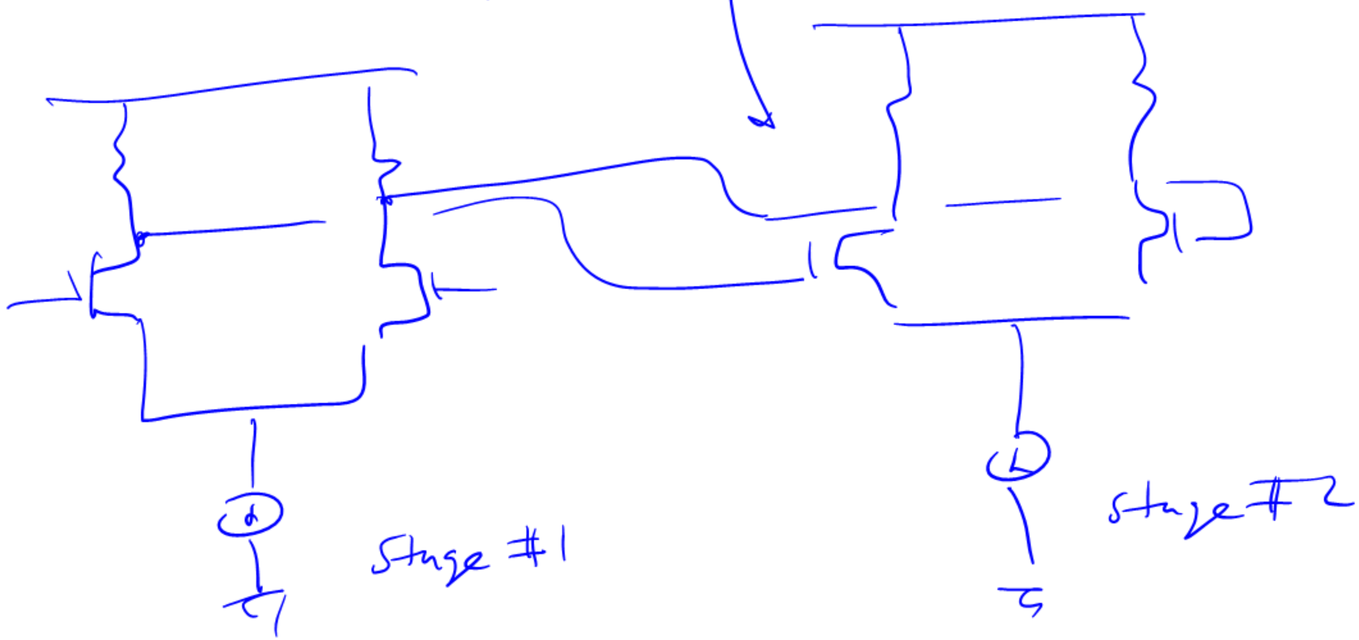
Why Differential?

- Differential circuits are much less sensitive to noises and interferences
- Differential configuration enables us to bias amplifiers and connect multiple stages without using coupling or bypass capacitors
- Differential amplifiers are widely used in IC's
  - Excellent matching of transistors, which is critical for differential circuits
  - Differential circuits require more transistors → not an issue for IC

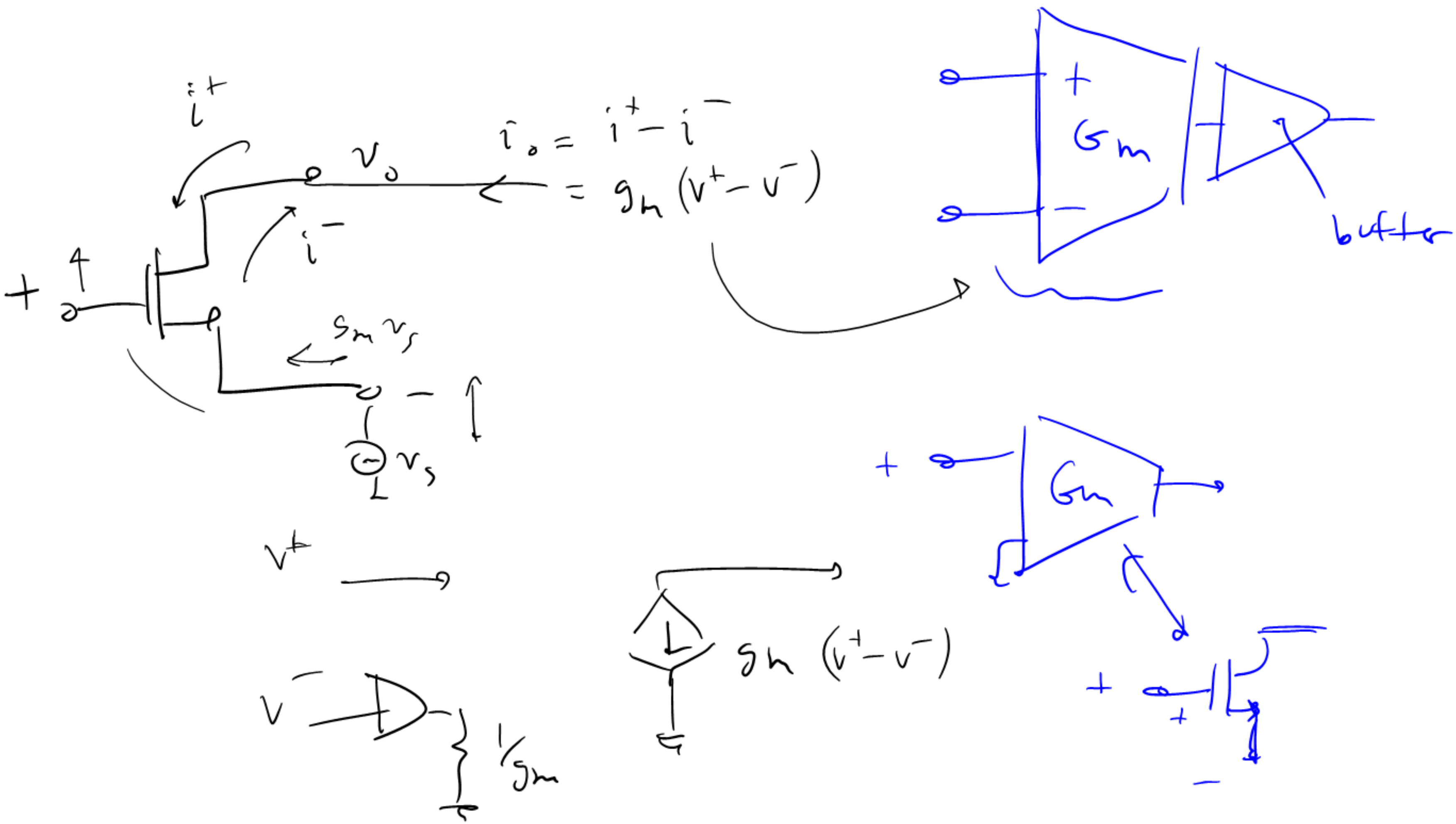


tolerates a large input CM range

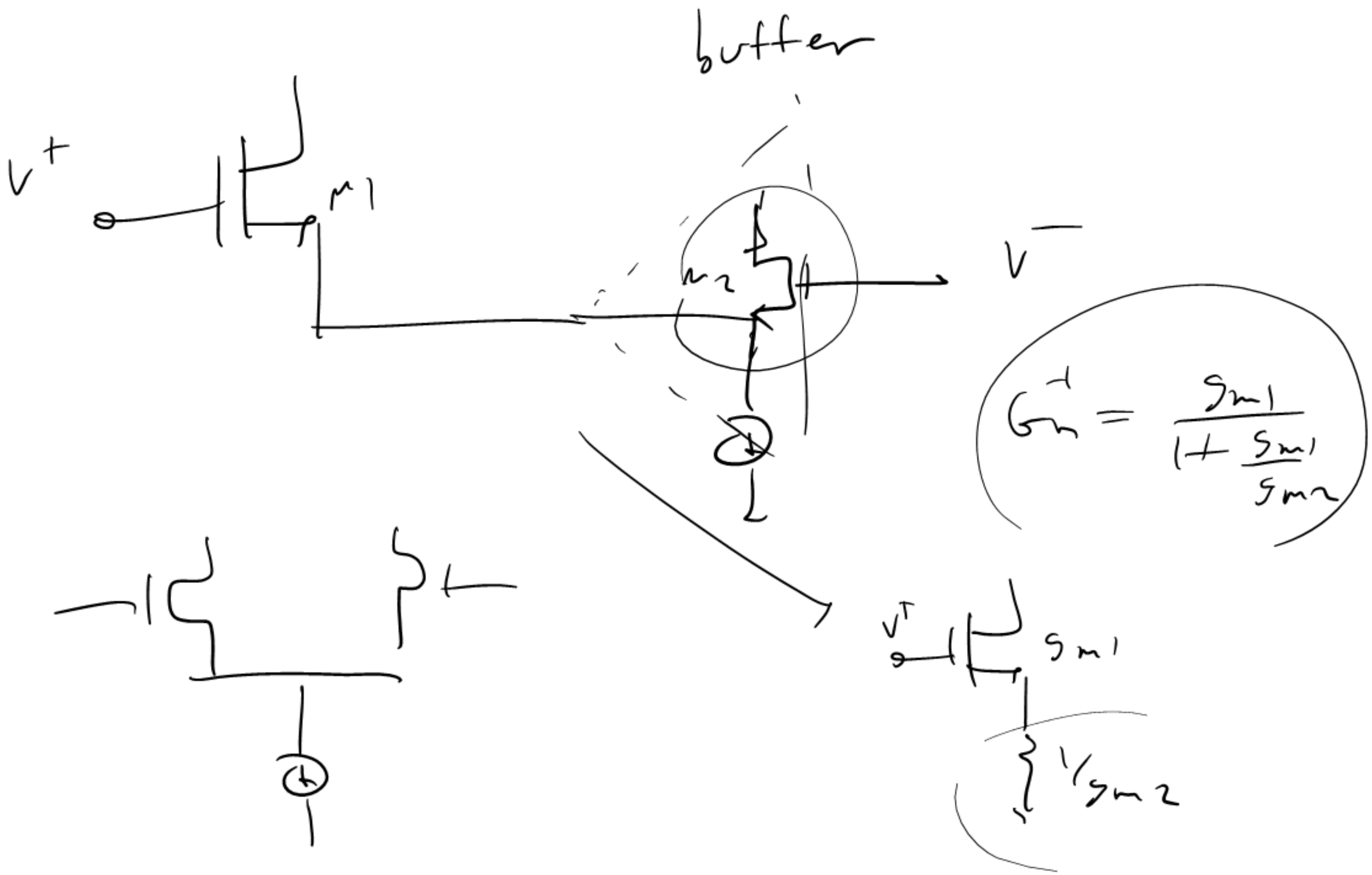


Goal: Differential Gm

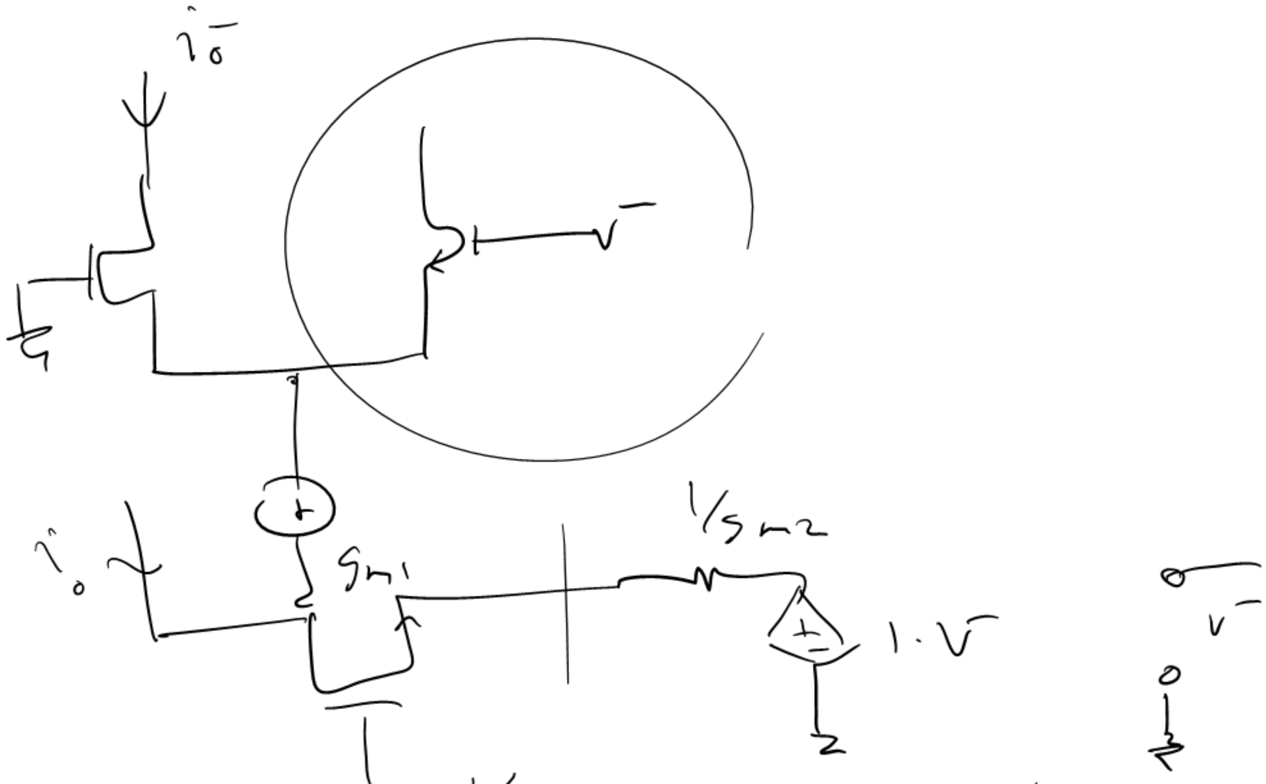
- What's wrong with this circuit?



Add a buffer to source side…



A symmetric pair is born…

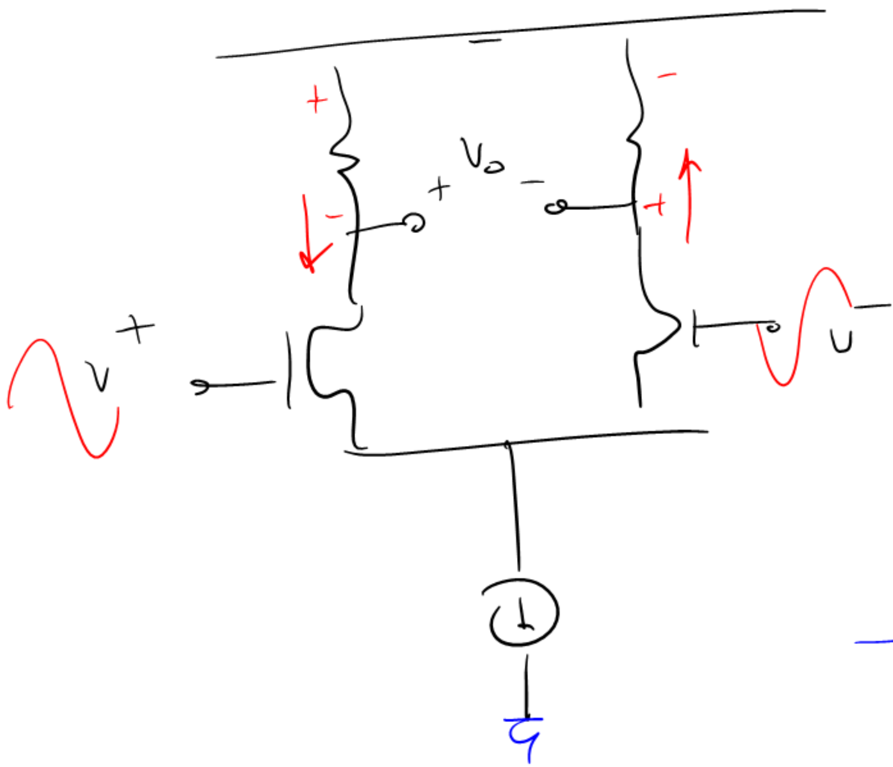


$$v_{gs} = -v^- \frac{1/g_{m1}}{1/g_{m1} + 1/g_{m2}} = -v^- \frac{1}{1 + \frac{g_{m1}}{g_{m2}}}$$

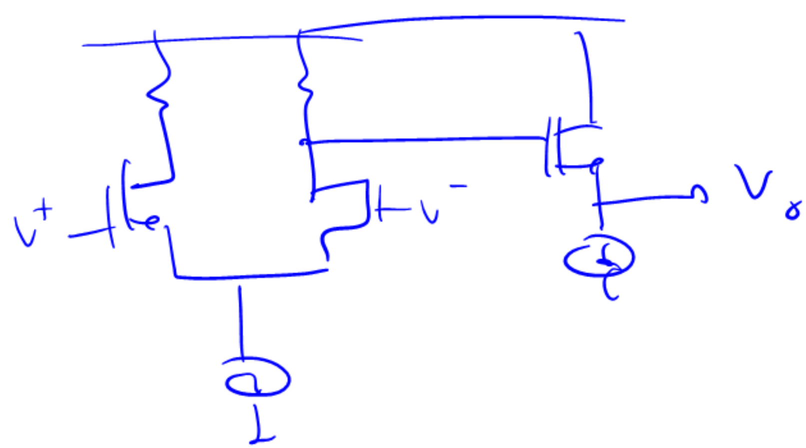
$$G_m^- = \frac{-g_{m1}}{1 + \frac{g_{m1}}{g_{m2}}}$$

MOS Differential-Pair

Basic Configuration

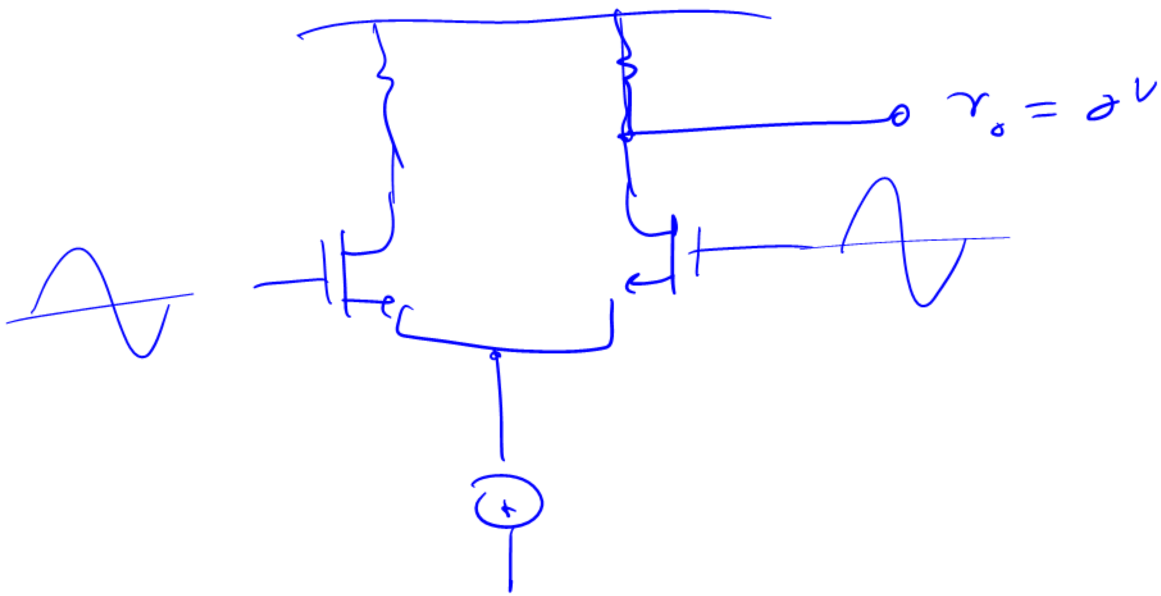


option : differential or single-ended output



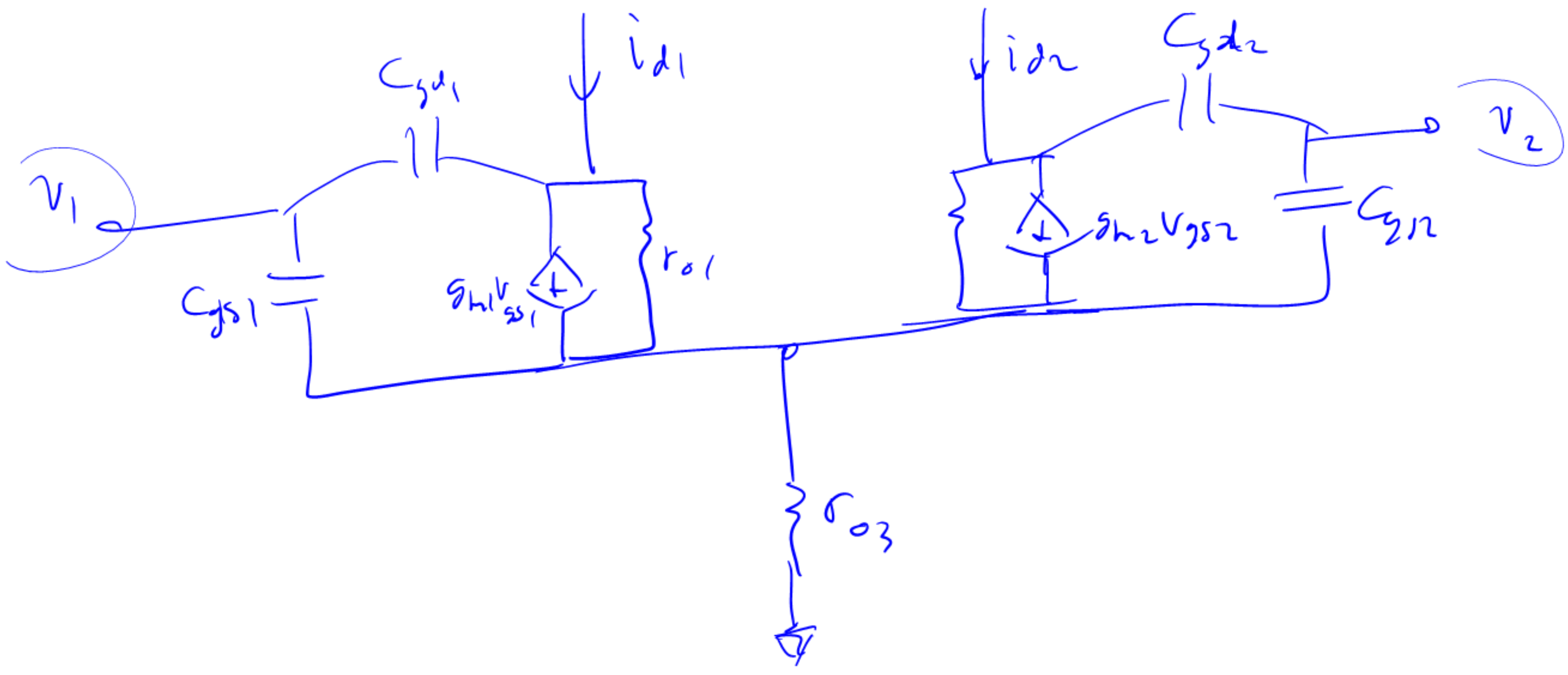
Common Mode Inputs

Differential Pair
Rejects Common-Mode Inputs



$$G_m(v^+ - v^-) = 0$$

Small Signal Operation



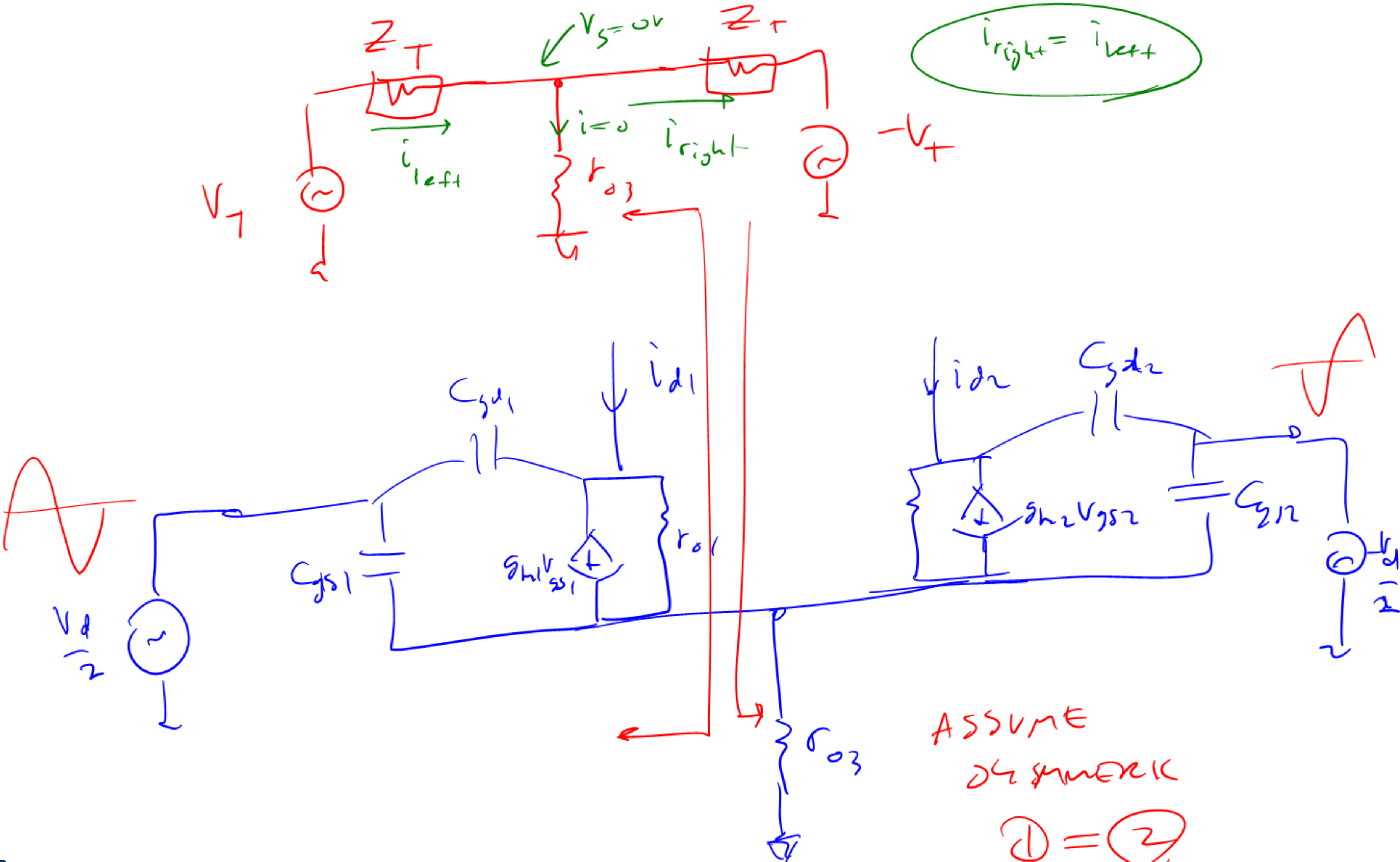
$$V_1 = \frac{V_d}{2} + V_c$$

$$V_2 = -\frac{V_d}{2} + V_c$$

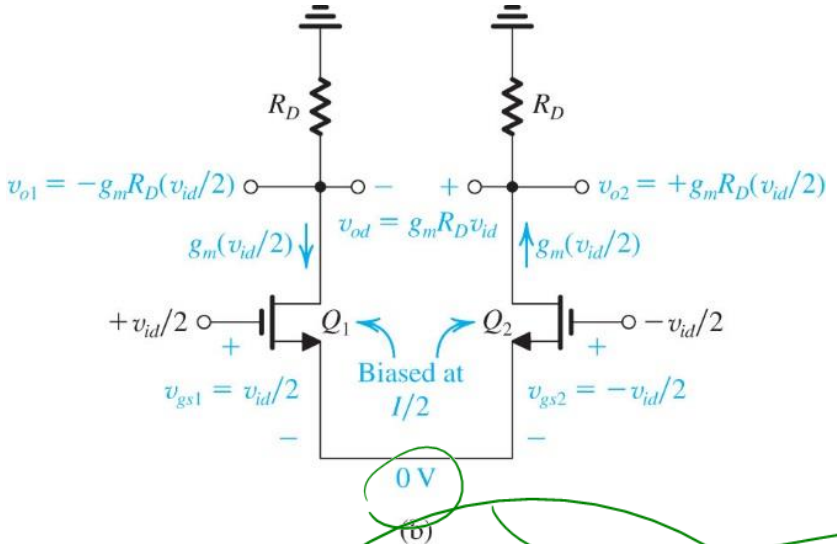
DM CM

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \longrightarrow \begin{pmatrix} V_d \\ V_c \end{pmatrix}$$

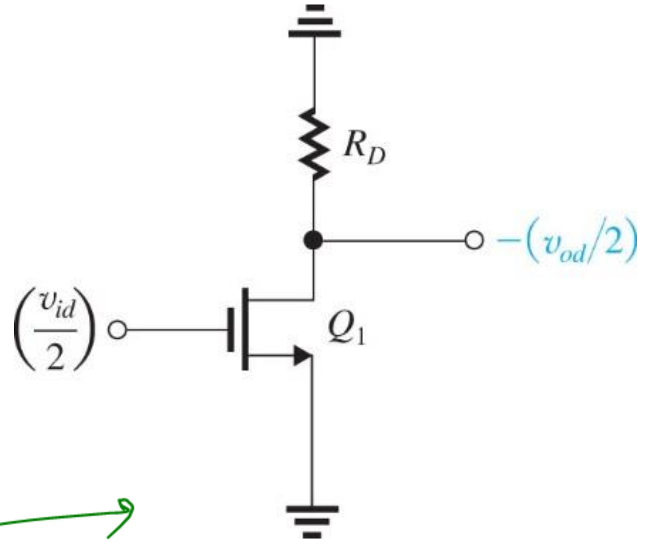
Differential Symmetry



Differential Half Circuit



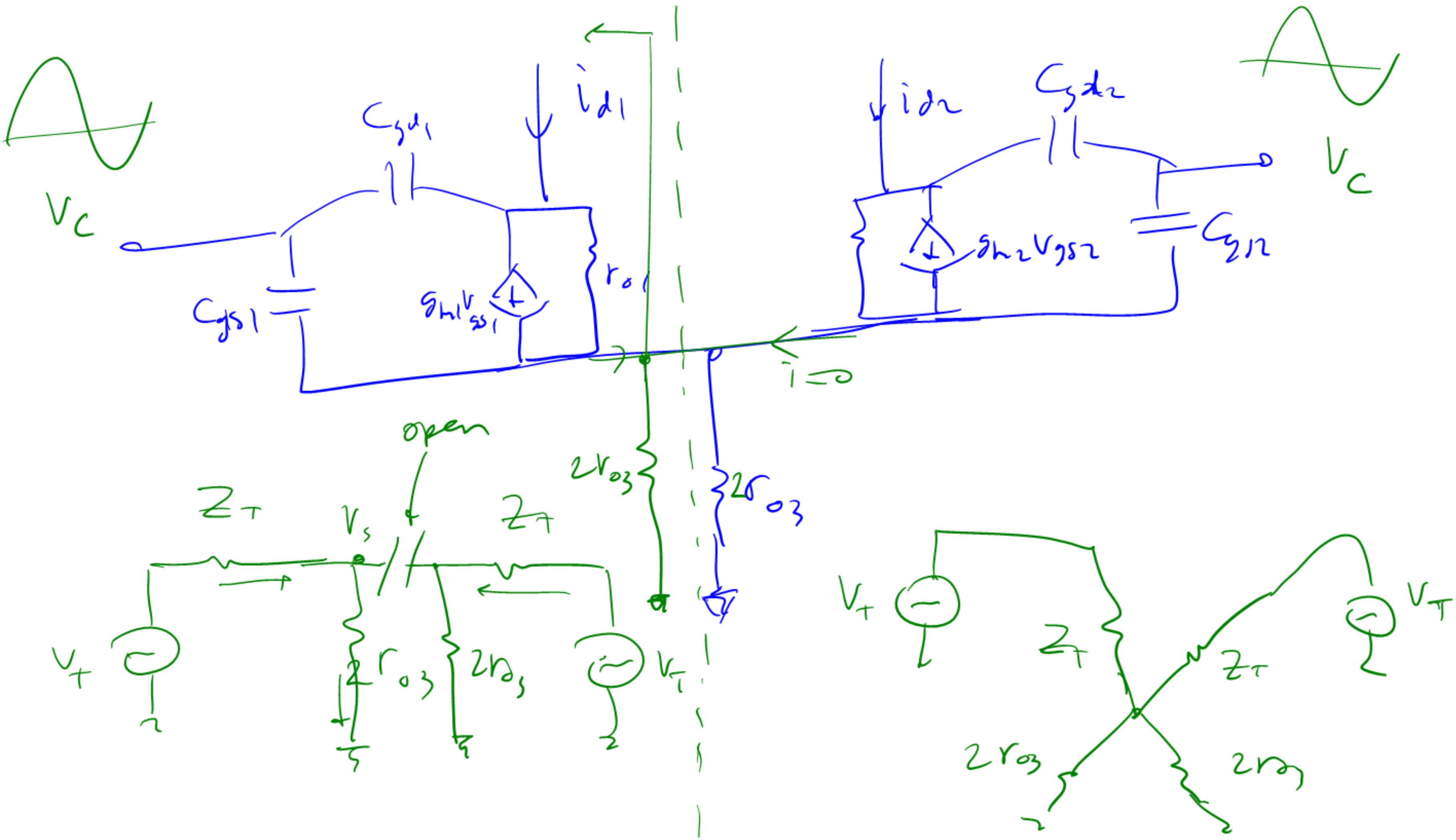
Virtual ground



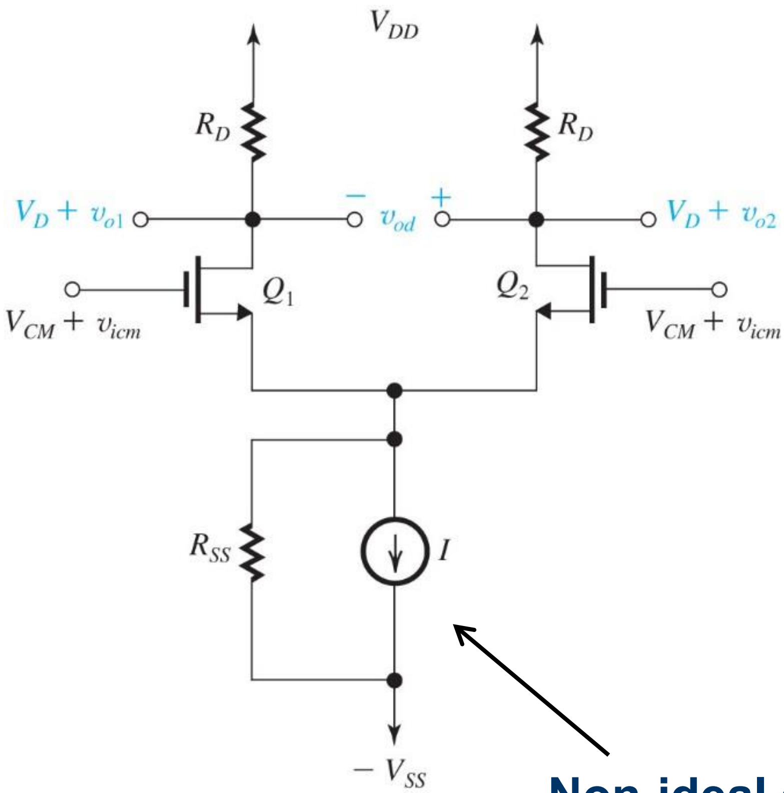
Q_1 biased at $\frac{I}{2}$

$$A_d = \frac{\frac{v_{od}}{2}}{\frac{v_{id}}{2}} = \frac{v_{od}}{v_{id}} = g_m \left(R_D \parallel r_o\right)$$

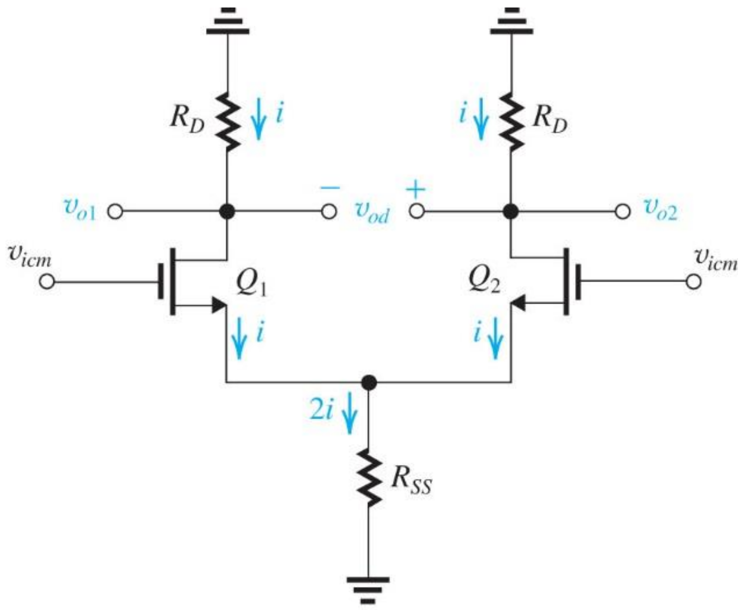
CM Symmetry


Vc
Cgd1
id1
ro1
gm1vgs1
Cgs1
id2
Cgd2
gm2vgs2
Cgs2
Vc
i=0
2ro3
2ro3
open
ZT
Vs
ZT
V+
2ro3
2ro3
VT
V+
ZT
ZT
VT
2ro3
2ro3

CM AC Equivalent Circuit



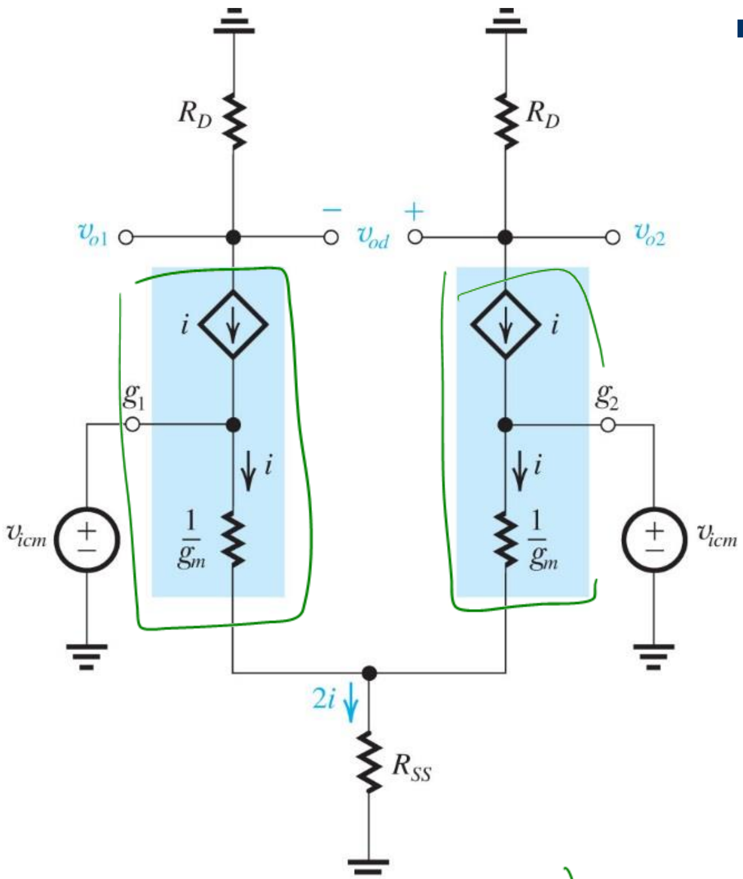
(a)

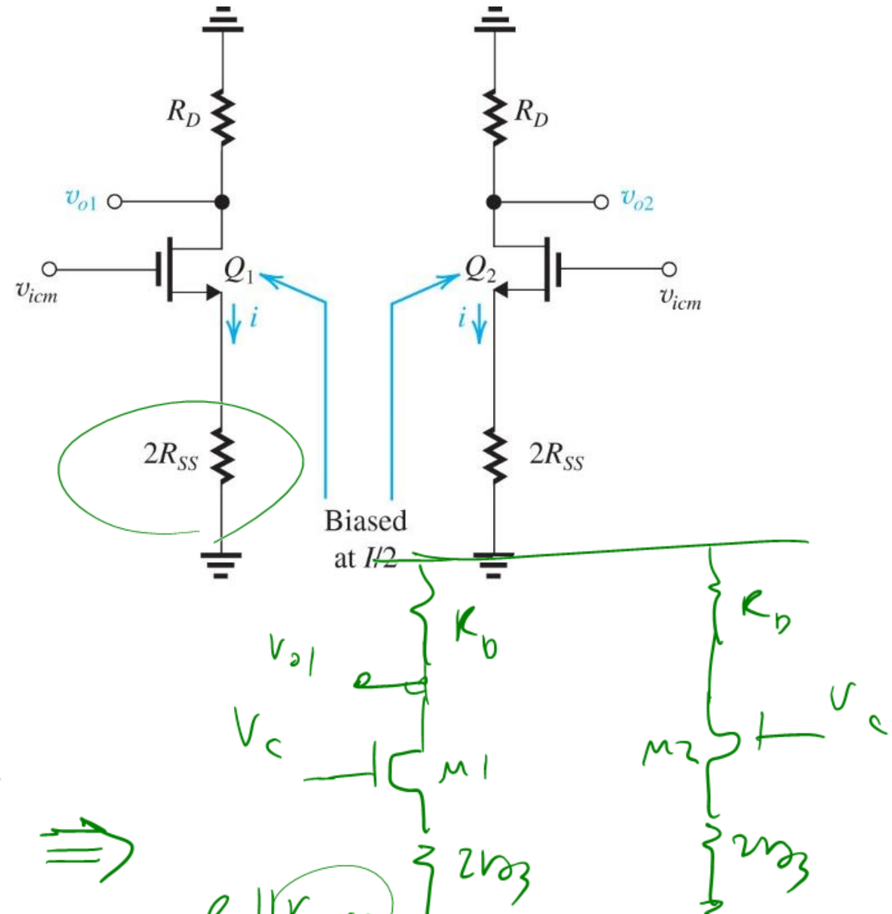


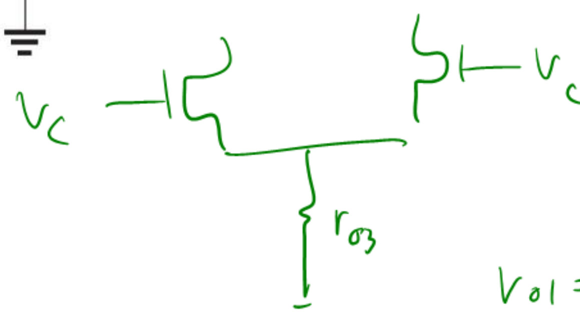
(b)

Non-ideal current source consists of an ideal current source shunted by a large resistance, R_{SS}

Common Mode "Half Circuit"

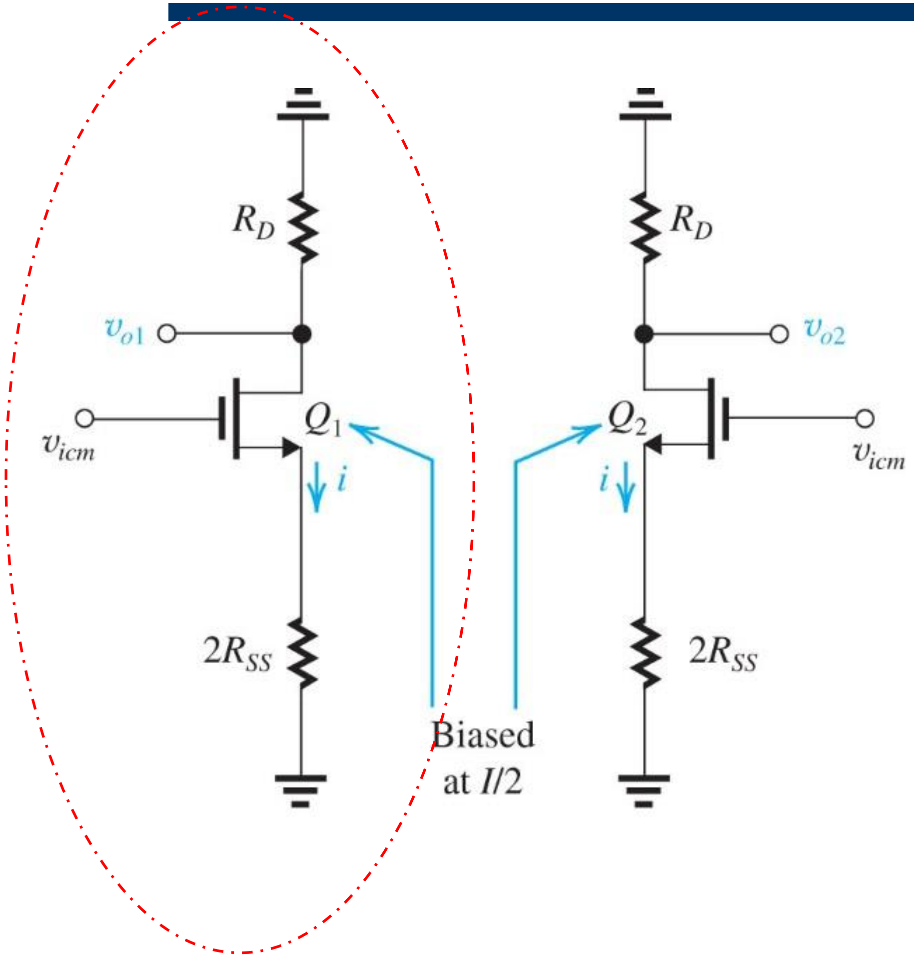






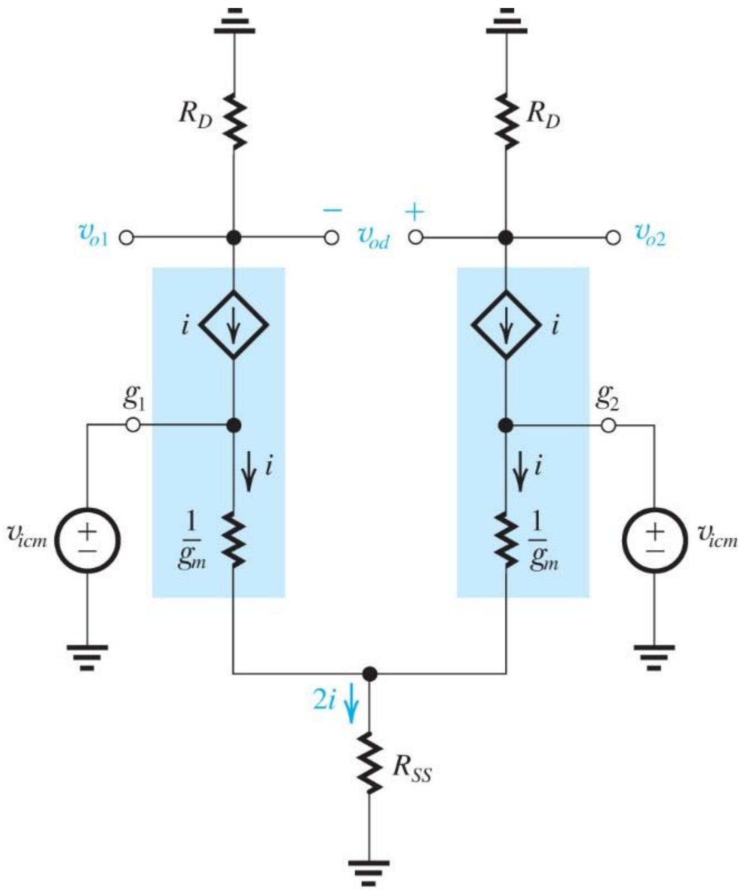
$$\frac{V_{o1}}{V_c} = \frac{-g_{m1} R_D \| r_{oeff}}{1 + g_{m1} \cdot 2r_{o3}}$$

Ideal CM Output Voltage



Common-Source with degeneration

Common Mode Gain with Mismatched R_D



However, any mismatch in the half circuits will produce finite output voltage, e.g.,

$$R_{D2} = R_D + \Delta R_D$$

$$v_{od} = v_{o2} - v_{o1} = \frac{-\Delta R_D}{2R_{SS}} v_{icm}$$

Common mode gain:

$$A_{cm} = \frac{v_{od}}{v_{icm}} = \frac{-\Delta R_D}{2R_{SS}} = \left(\frac{-R_D}{2R_{SS}}\right)\left(\frac{\Delta R_D}{R_D}\right)$$

Common Mode Rejection Ratio (CMRR):

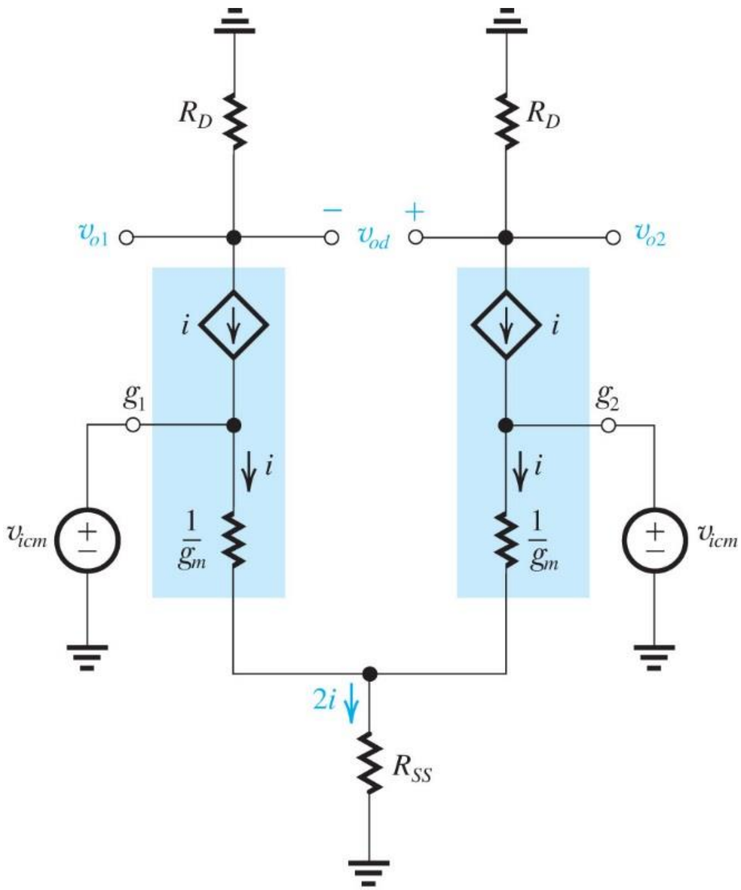
$$CMRR \equiv \frac{|A_d|}{|A_{cm}|}, \qquad \text{in dB: } CMRR(dB) \equiv 20\log\frac{|A_d|}{|A_{cm}|}$$

CMRR should be as large as possible.

For the above case,

$$\text{CMRR} = \frac{g_m R_D}{\dfrac{\Delta R_D}{2R_{SS}}} = \frac{2g_m R_{SS}}{\left(\dfrac{\Delta R_D}{R_D}\right)}$$

Common Mode Gain with Mismatch of g_m



Mismatch in g_m :

$$g_{m1} = g_m + \frac{1}{2}\Delta g_m; \qquad g_{m2} = g_m - \frac{1}{2}\Delta g_m$$

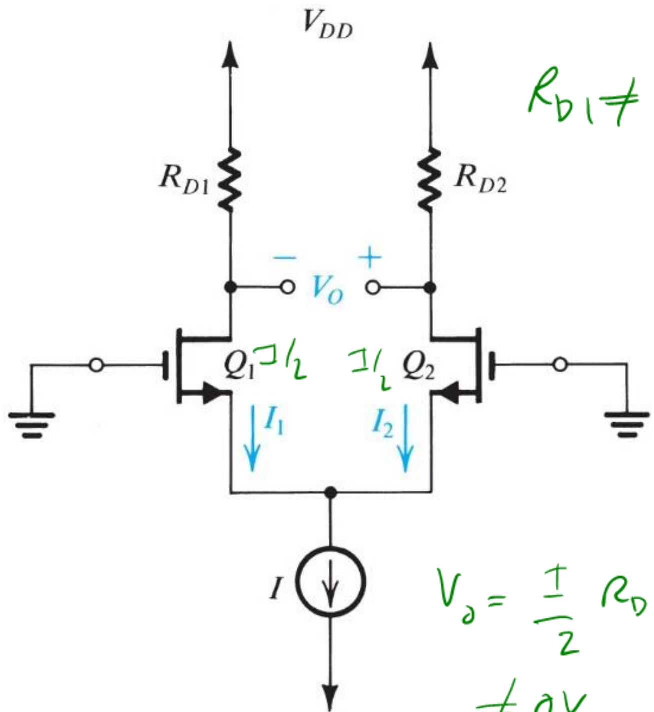
$$g_{m1} - g_{m2} = \Delta g_m$$

(Derivation skipped)

$$A_{cm} = \frac{v_{od}}{v_{icm}} = \frac{R_D}{2R_{SS}} \frac{\Delta g_m}{g_m}$$

$$\mathrm{CMRR} = \frac{g_m R_D}{\frac{R_D}{2R_{SS}} \frac{\Delta g_m}{g_m}} = \frac{2 g_m R_{SS}}{\left(\frac{\Delta g_m}{g_m}\right)}$$

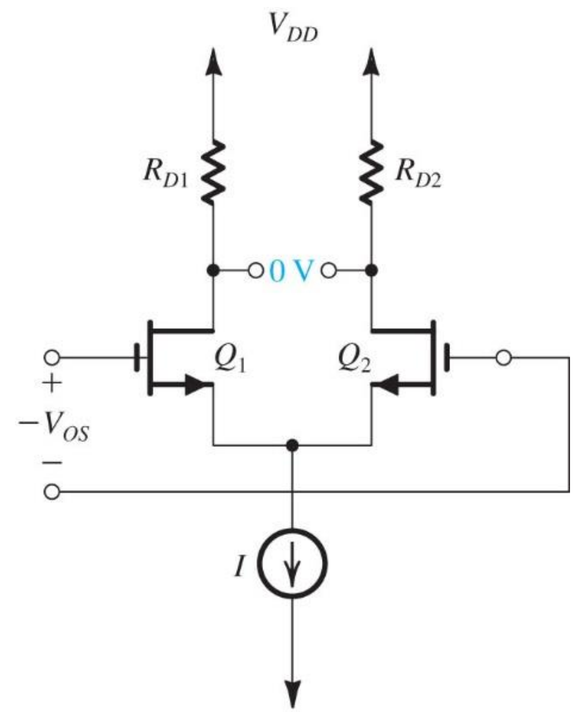
DC Offset



$R_{D1} \neq R_{D2}$

$V_o = \frac{I}{2} R_{D1} - \frac{I}{2} R_{D2}$

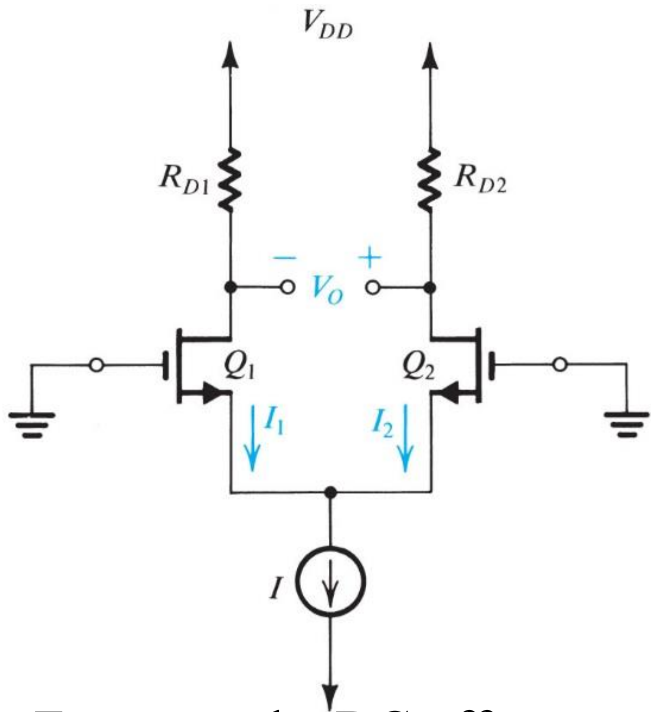
$\neq 0V$

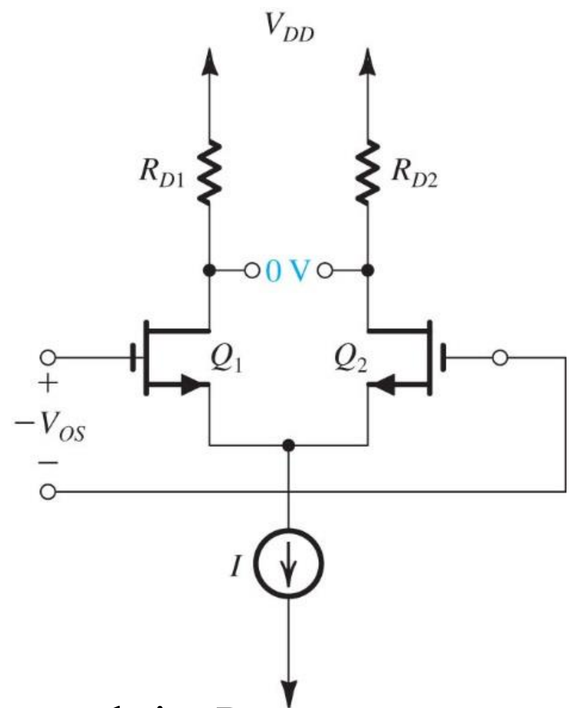


Due to mismatch in R_D, output voltage $V_O \neq 0$ even both inputs are grounded. To produce zero output, an input offset voltage

$V_{OS} = \dfrac{V_O}{A_d}$, where A_d is differential gain, needs to be applied.

DC Offset



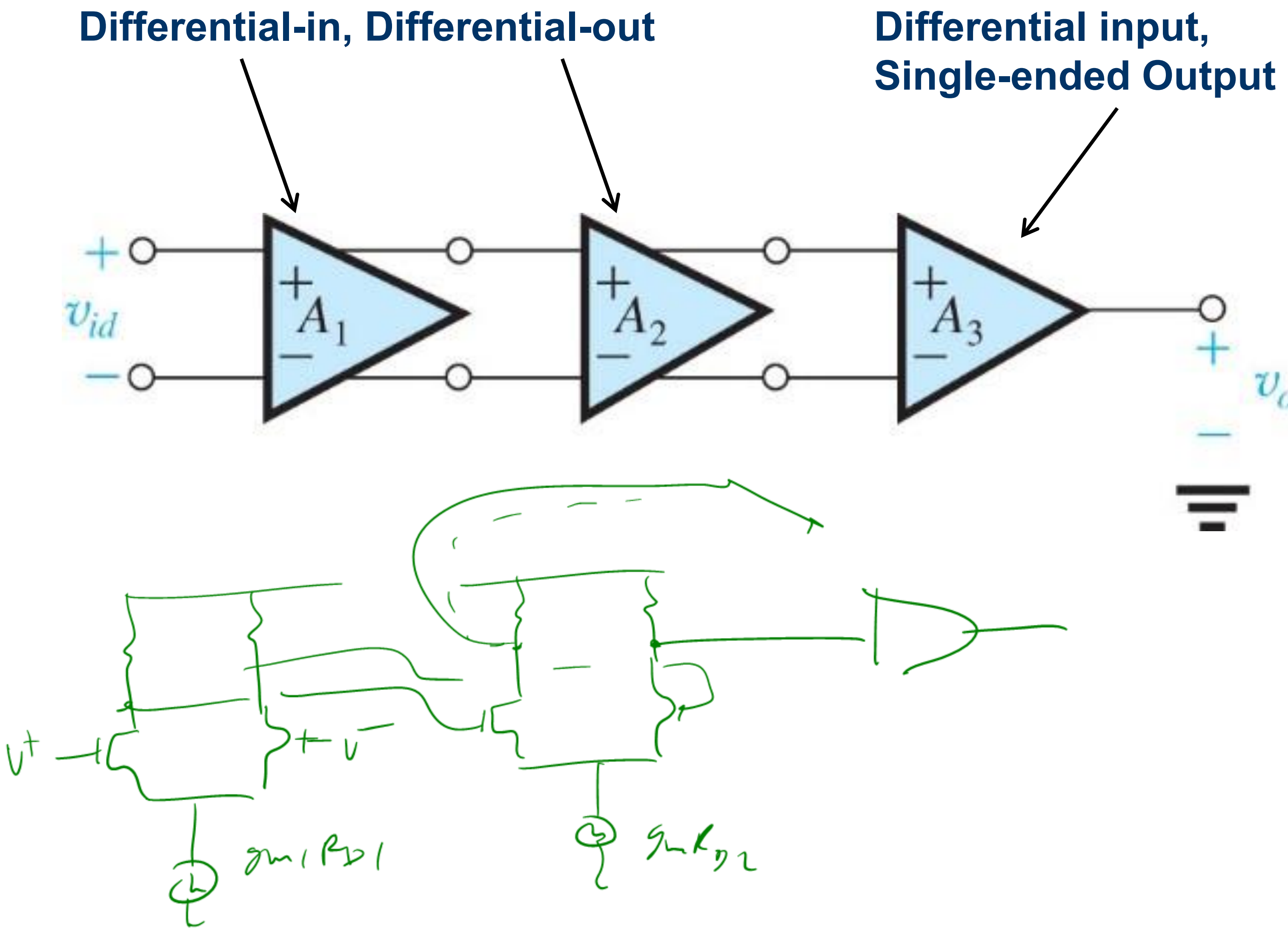


For example, DC offset caused by mismatch in R_D :

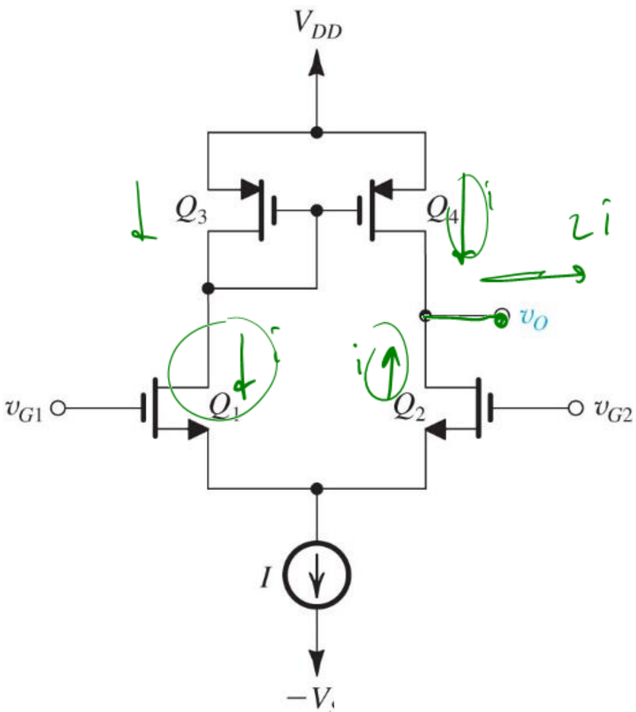
$$R_{D1} = R_D + \Delta R_D / 2; \quad R_{D2} = R_D - \Delta R_D / 2; \quad V_O = V_{D2} - V_{D1} = \frac{I}{2}\Delta R_D$$

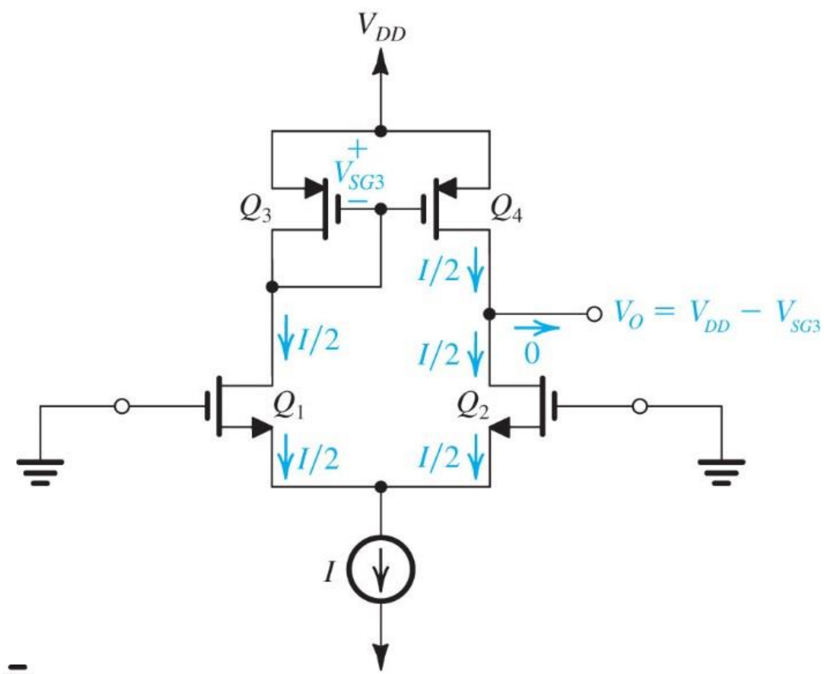
$$V_{OS} = \frac{V_O}{A_d} = \frac{I\Delta R_D / 2}{g_m R_D} = \frac{I\Delta R_D / 2}{2\left(\frac{I/2}{V_{OV}}\right)R_D} = \frac{V_{OV}}{2}\frac{\Delta R_D}{R_D}$$

Differential Input, Single-End Output

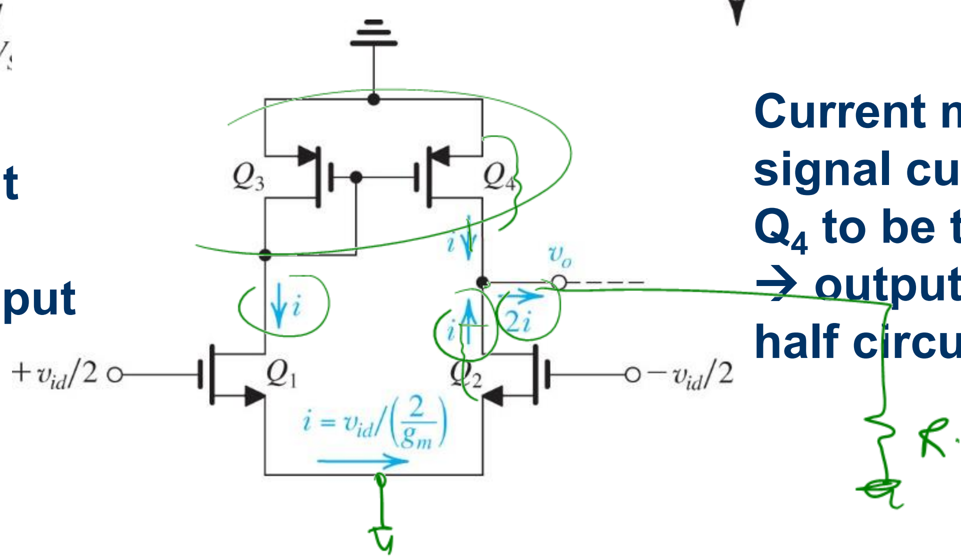


Current Mirror Load (1)



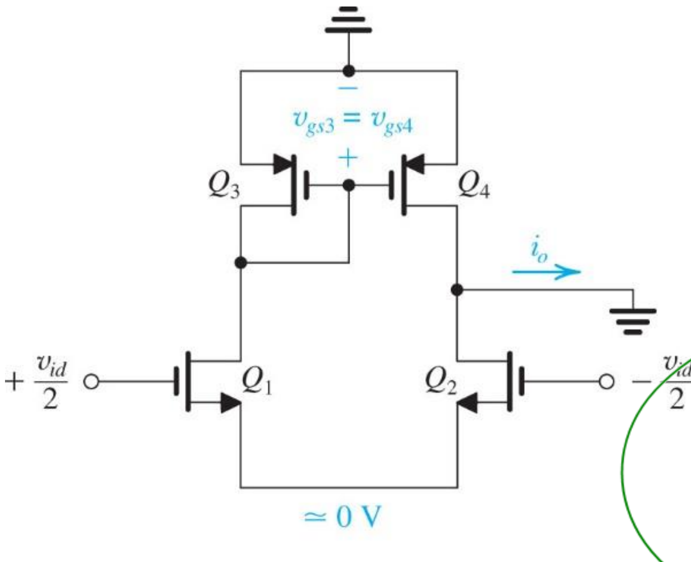


AC equivalent circuit for differential input

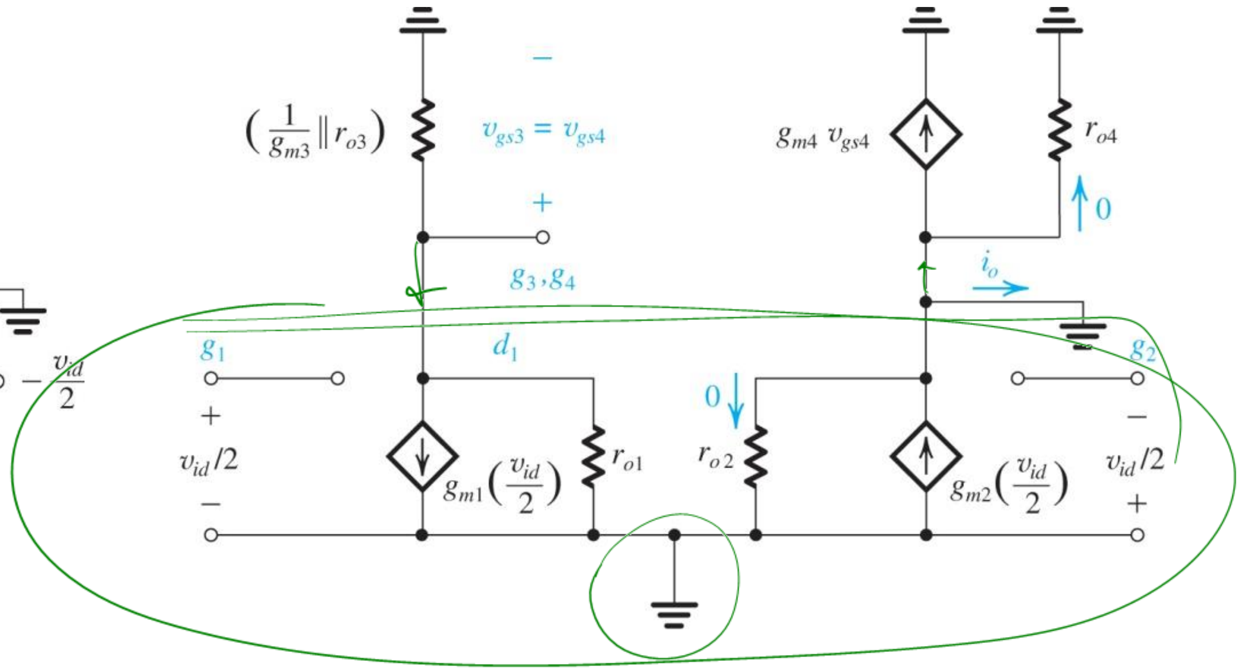


Current mirror forces small-signal currents through Q_3 and Q_4 to be the same
→ output currents = 2x that of half circuit

Current Mirror Load (2)



(a)



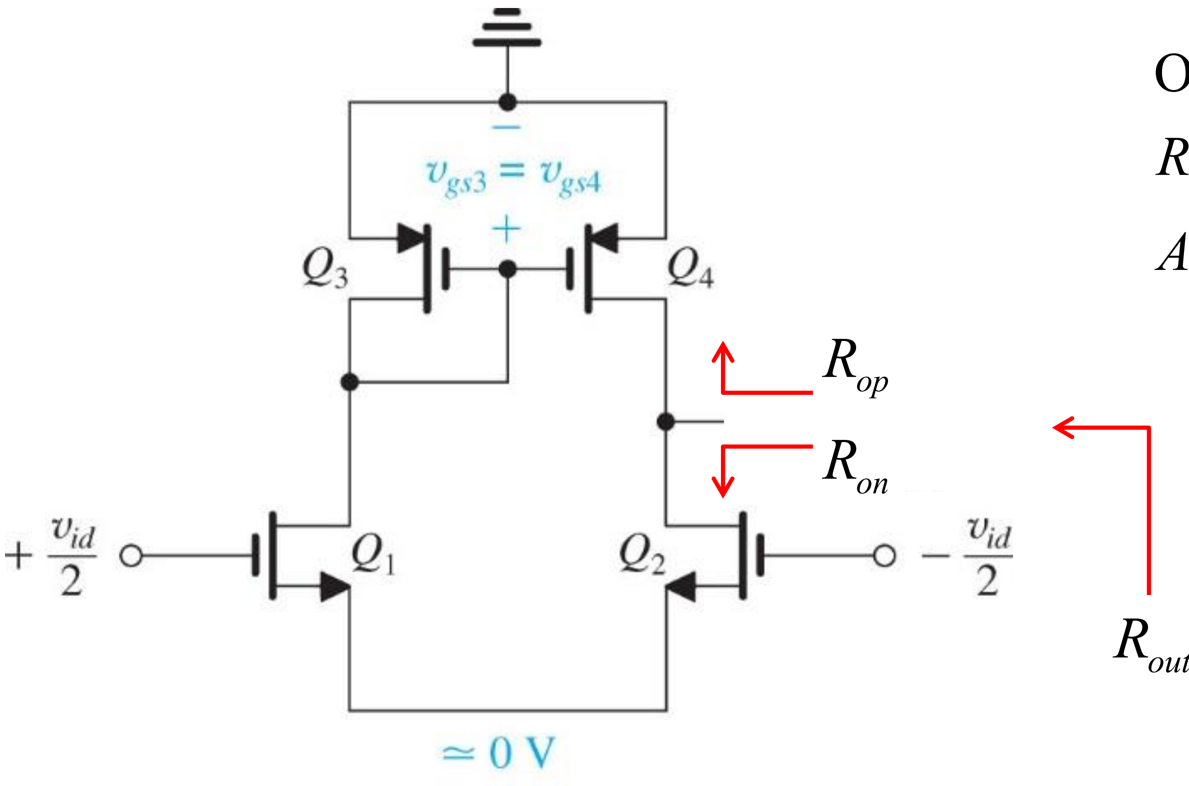
Short-circuit transconductance of differntial pair with current mirror load:

$$G_m = \frac{i_o}{v_{id}}; \quad i_o: \text{ output current with short-circuit load}$$

$$i_o = g_{m2}\left(\frac{v_{id}}{2}\right) - g_{m4} v_{gs4}; \quad v_{gs4} = v_{gs3} = -g_{m1}\left(\frac{v_{id}}{2}\right)\left(\frac{1}{g_{m3}} \| r_{o3} \| r_{o1}\right) \approx -\frac{g_{m1}}{g_{m3}}\frac{v_{id}}{2}$$

$$g_{m1} = g_{m2} = g_m; \quad g_{m3} = g_{m4} \quad \Rightarrow \quad i_o = g_m v_{id} \quad \Rightarrow \quad G_m = g_m$$

Current Mirror Load (3)



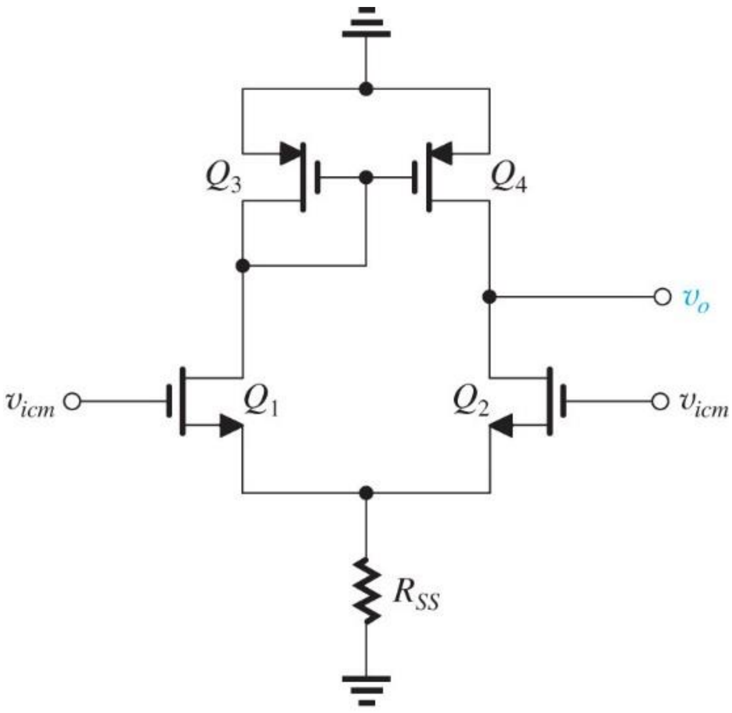
(a)

Output resistance,

$$R_{out} = R_{op} \parallel R_{on} = r_{o4} \parallel r_{o2}$$

$$A_d = G_m R_{out} = g_m \left(r_{o4} \parallel r_{o2} \right)$$

Common Mode Gain



(a)

Common mode gain (derivation skipped):

$$A_{cm} \approx -\frac{1}{2g_{m3}R_{SS}}$$

$$CMRR = \frac{|A_d|}{|A_{cm}|} = g_m\left(r_{o4} \parallel r_{o3}\right) \times 2g_{m3}R_{SS}$$

For $r_{o4} = r_{o3} = r_o$ and $g_m = g_{m3}$

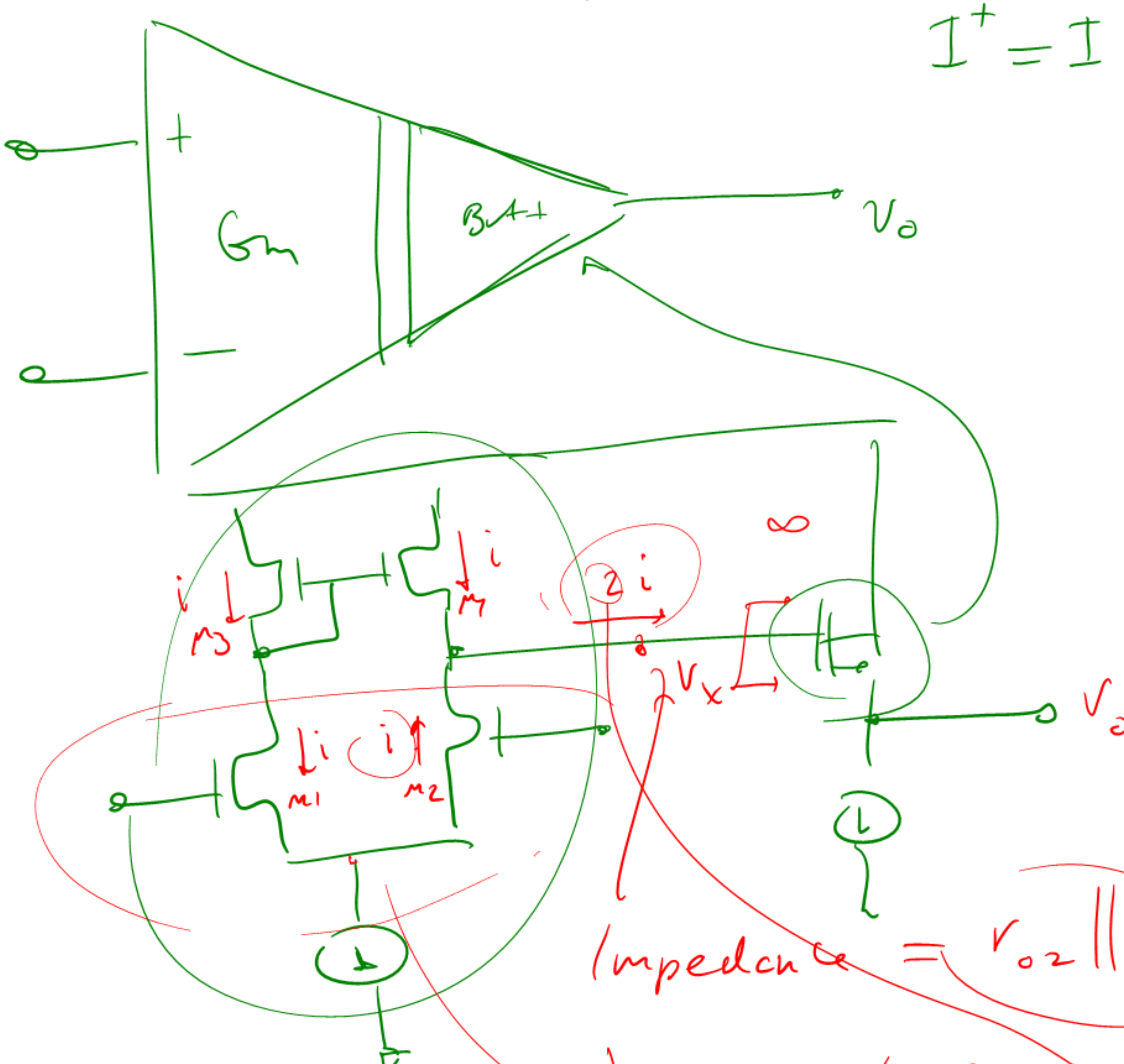
$$CMRR = \left(g_m r_o\right)\left(g_m R_{SS}\right)$$

Op-amp

$I^+ = I^- = 0A$

MOS Amp

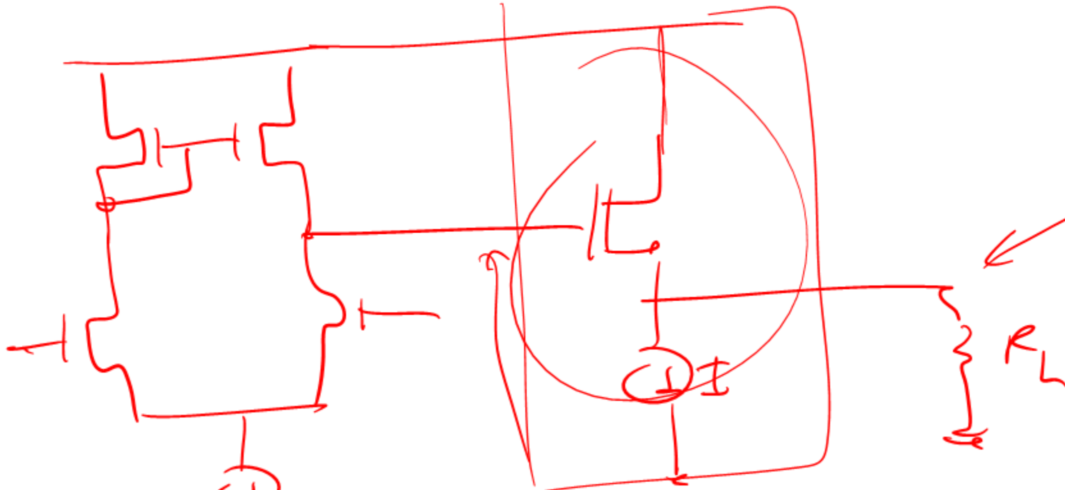
GATE CURRENT $I_G = 0A$



Impedance $= r_{o2} \| r_{o3}$

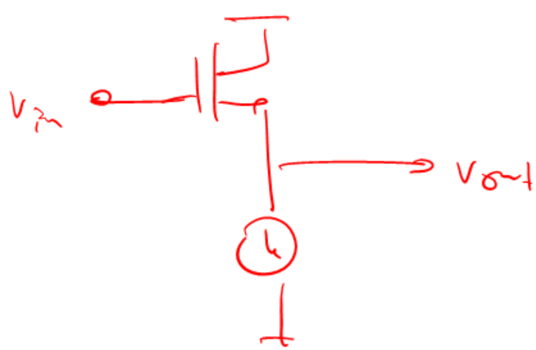
$$V_x = \underbrace{g_m \left(\frac{V_d}{2}\right)}_{i} \times 2 \times r_{o2} \| r_{o3}$$

$$\frac{V_x}{V_d} = g_{m1}(r_{o2} \| r_{o3})$$



$V_x = (g_m r_{o2} || r_{o3}) v_d$

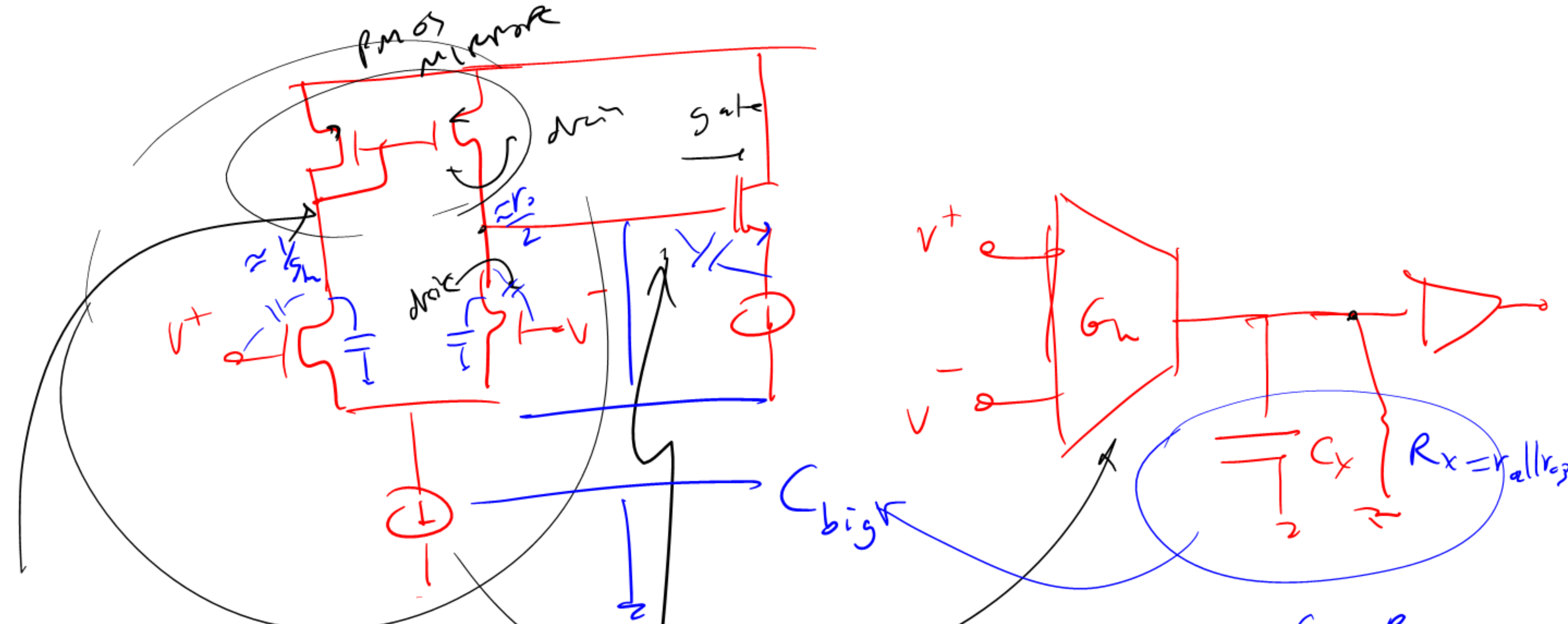
$\frac{V_o}{V_x} =$



1. draw small-signal ckt & analyze

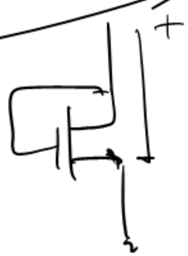
2. "memory"

3. 2-port equivalent



diode loaded node

low-Z node



hi Z node

$$A_o = G_m R_x$$

$$\omega_o = \frac{1}{C_x R_x}$$

$$A(j\omega) = \frac{A_o}{1 + j\frac{\omega}{\omega_o}}$$

$$GBW = \frac{G_m \cancel{R_x}}{\cancel{R_x} C_x}$$

$$\boxed{GBW = \frac{G_m}{C_x}}$$

"diode connected" transistor ≠  p-n junction