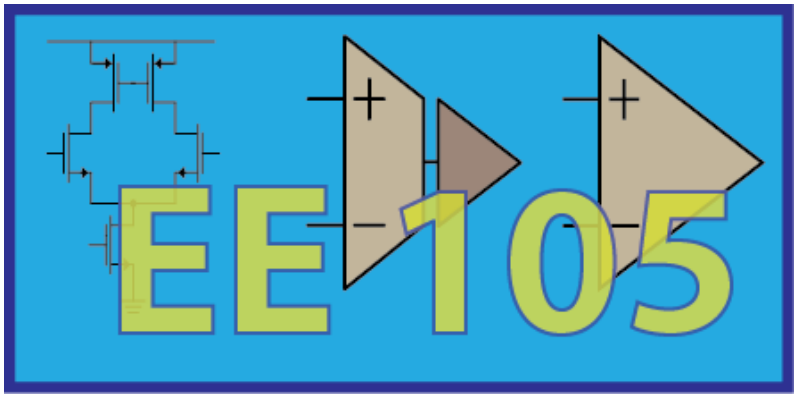

Differential Amplifiers

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Announcements

- HW11 due on Friday, last homework!
- Lab 6 due this week, last lab!
- Check web site for updates on RRR & finals week office hours and review sessions:
- http://rfic.eecs.berkeley.edu/105/lectures.html

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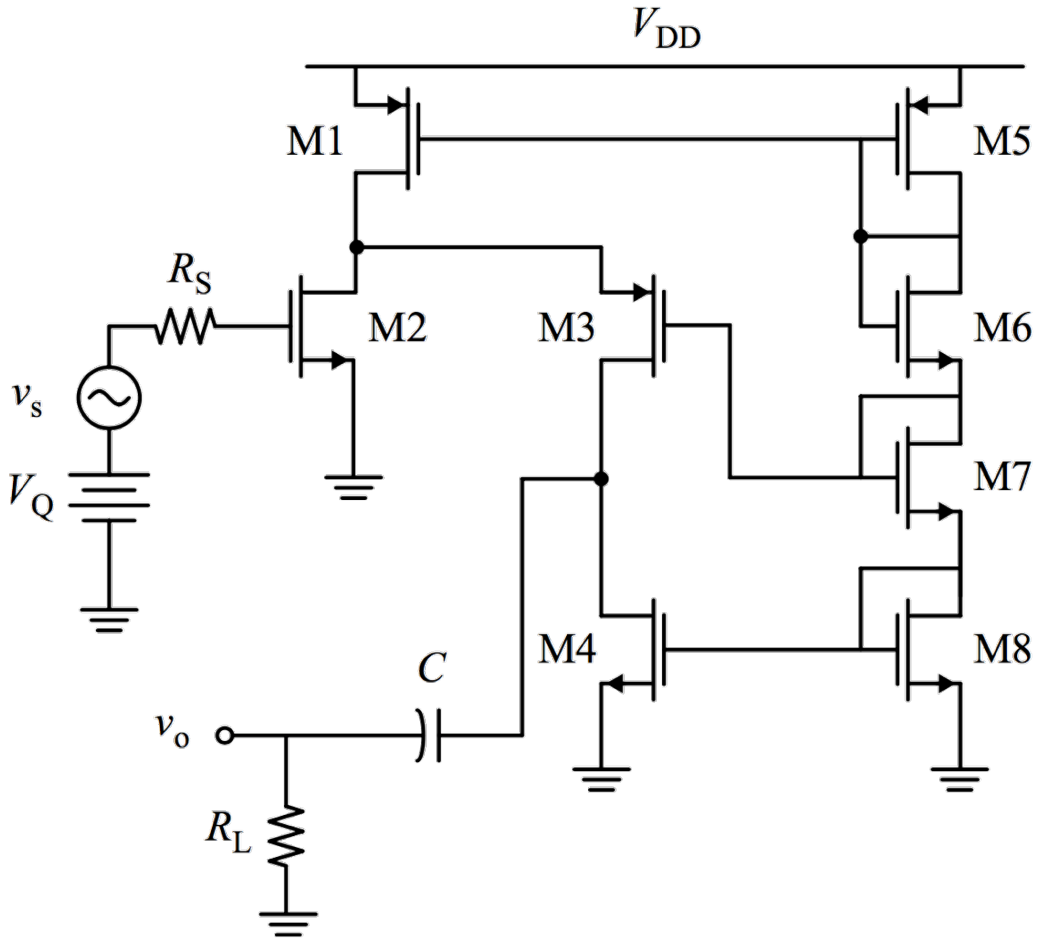
Multistage Analysis Example



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Cutting Through the Complexity

1. Identify the "signal path" between the input and output

2. Eliminate "background" transistors to reduce clutter
   ↳ biasing

3. For "background" transistors, understand their role (e.g. DC biasing)

4. For frequency response, identify "hi-Z" nodes.

$\tau = RC$ ← look for high R contributes to dom. pole / BW

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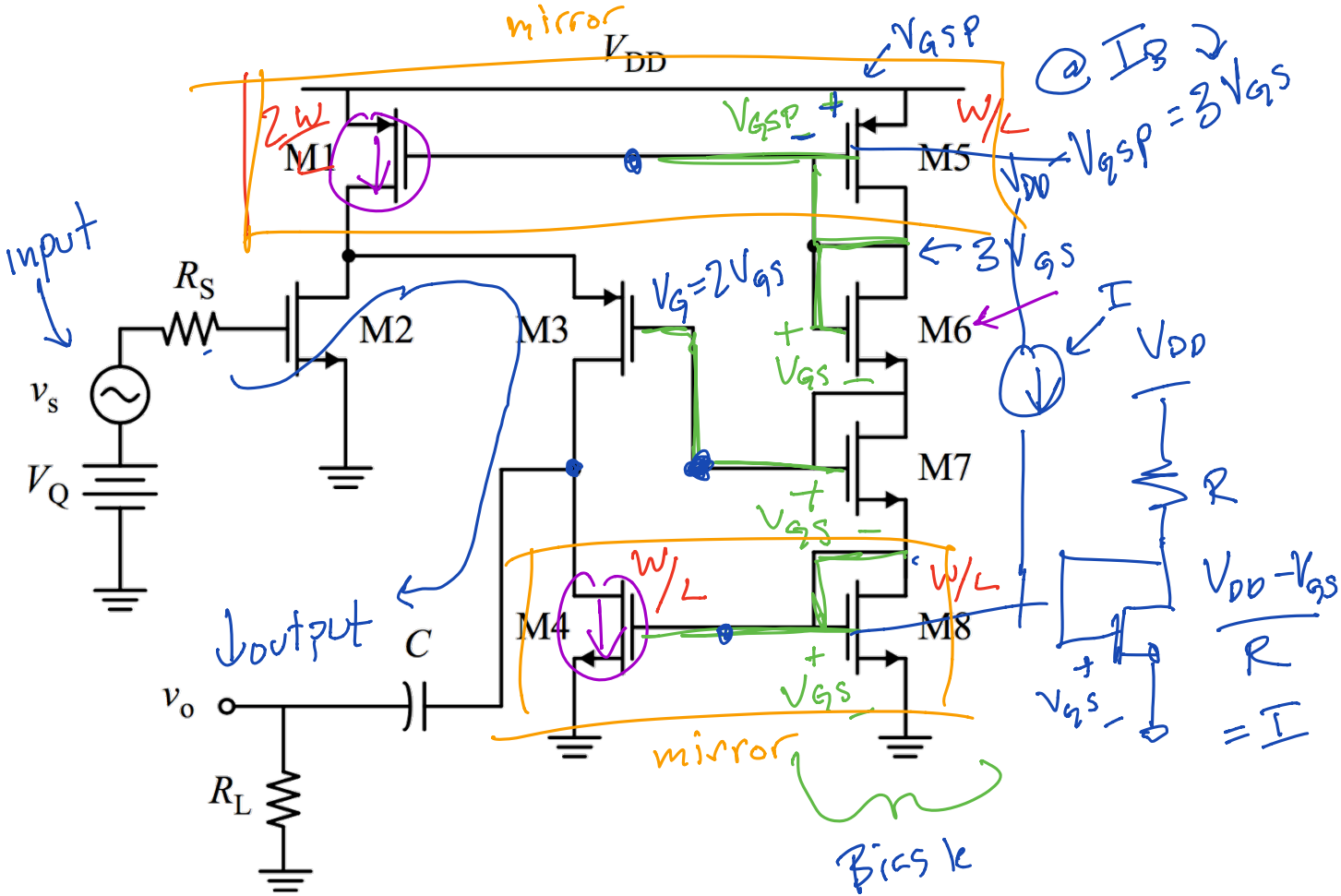
Eliminate Clutter



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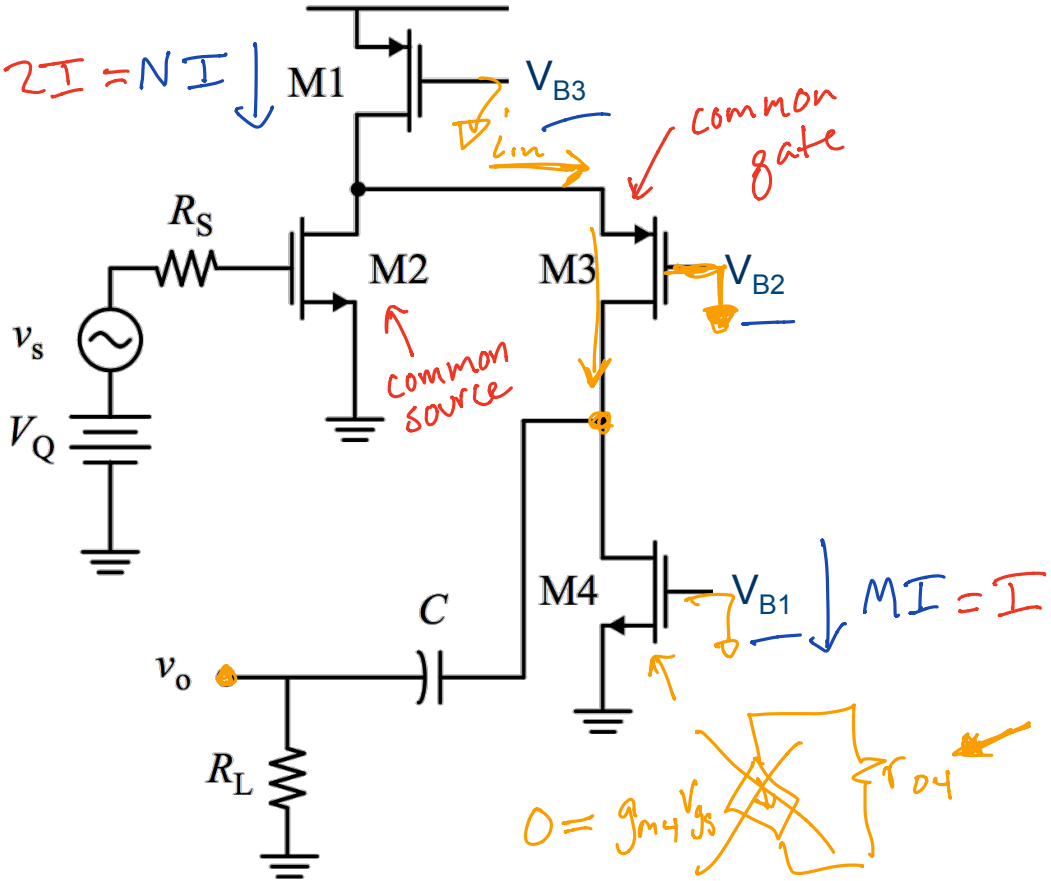
Identify Signal Path & Amplifier Stages



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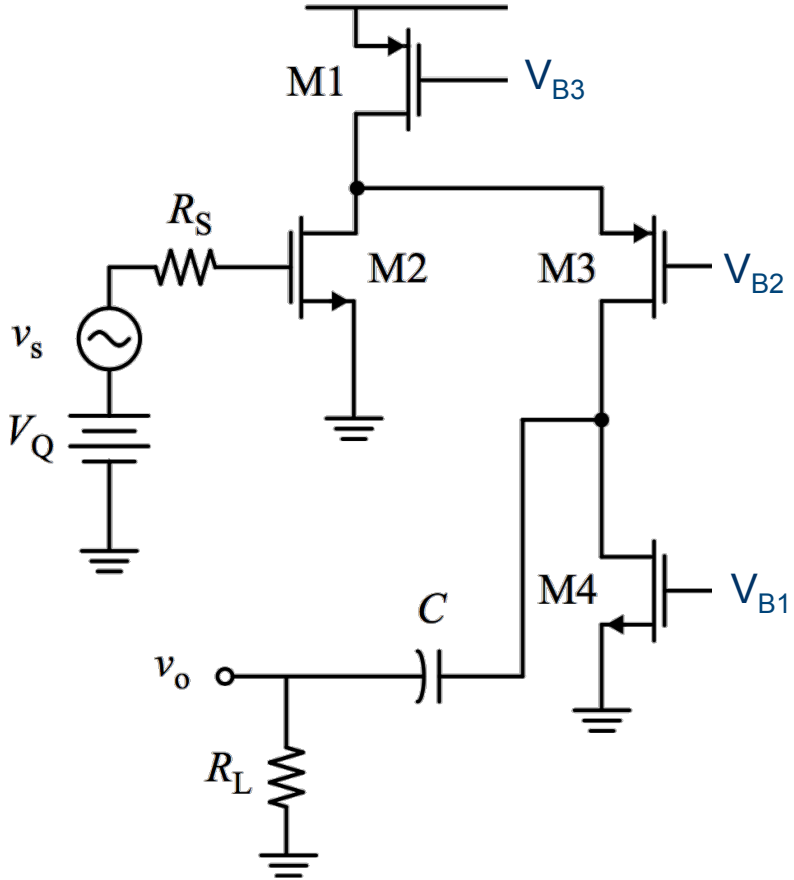
DC Biasing



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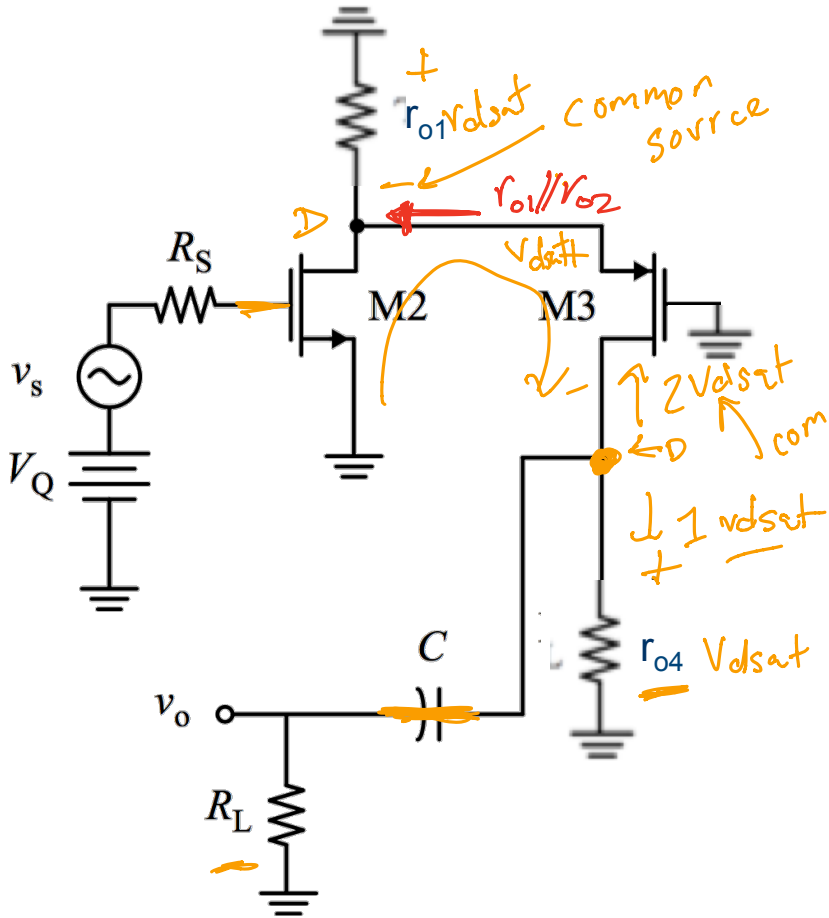
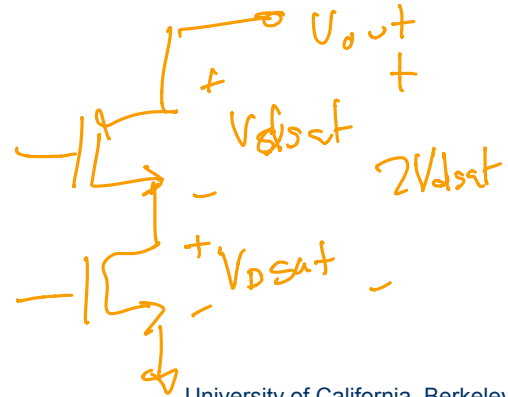
Small-Signal Models



Cascode disadv. = output swing

folded casc. = improved output swing



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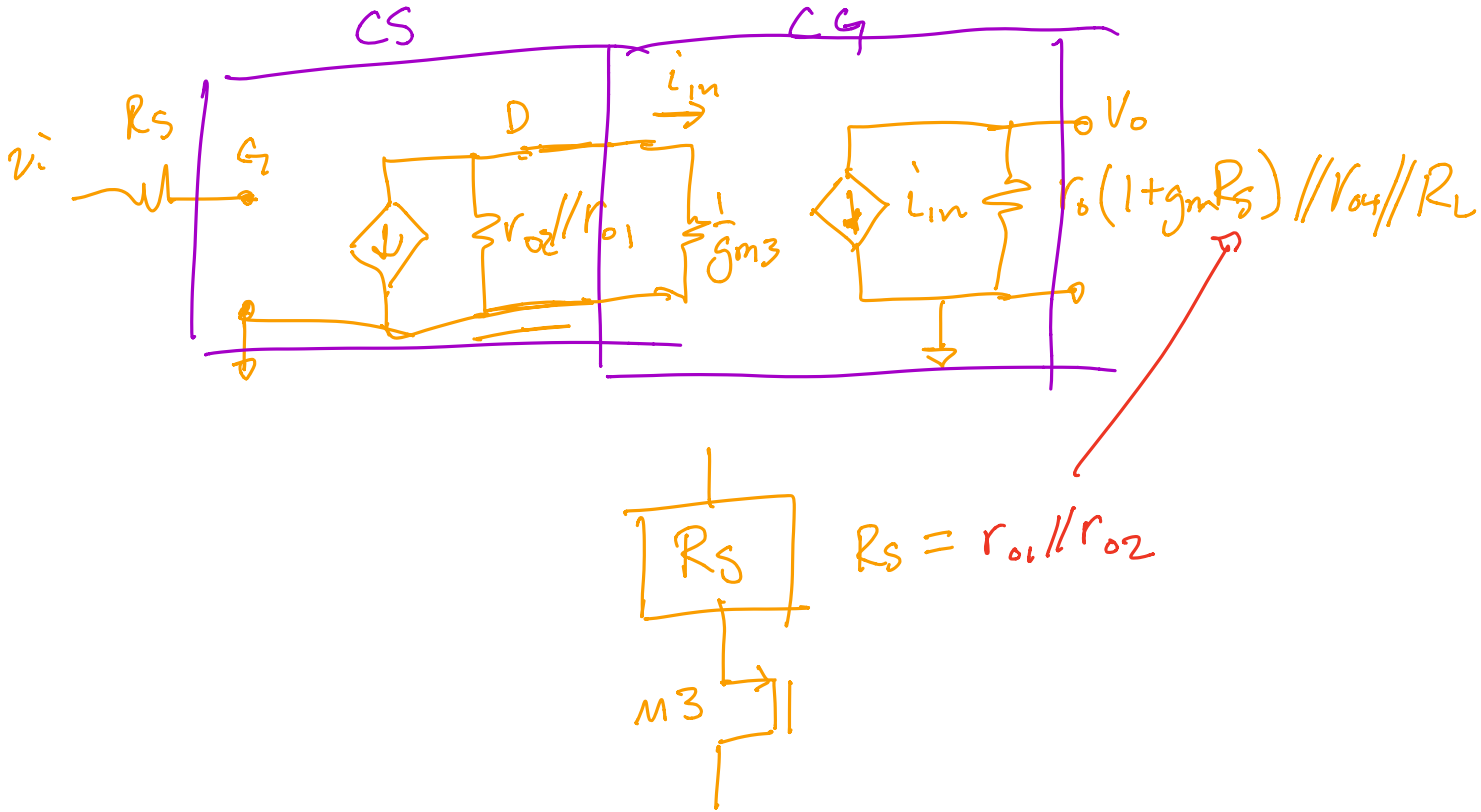
Two-Port Model



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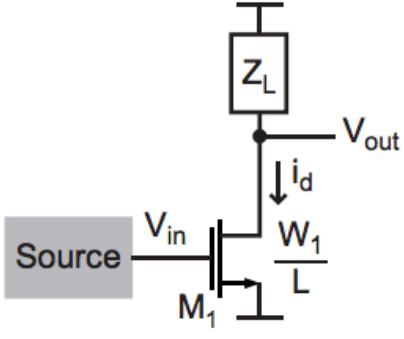
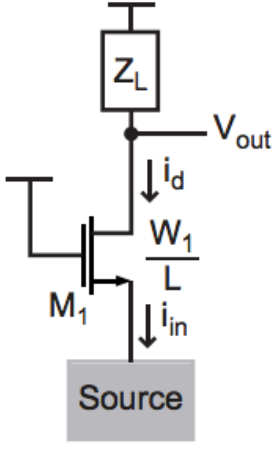
Basic Amplifier Types

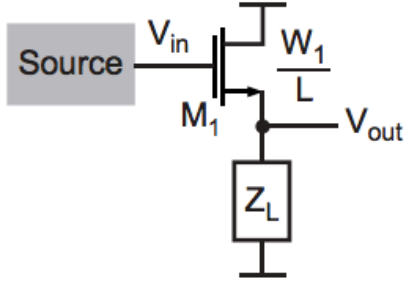
Common Source



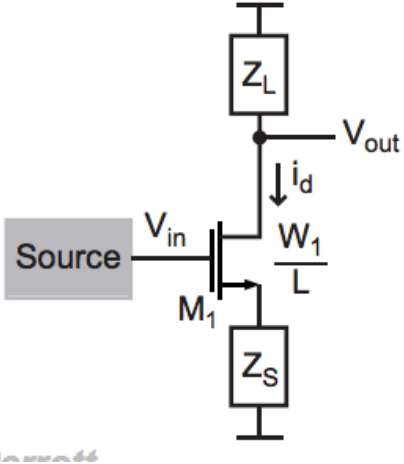
Common Gate



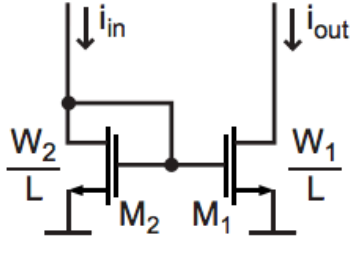
Source Follower



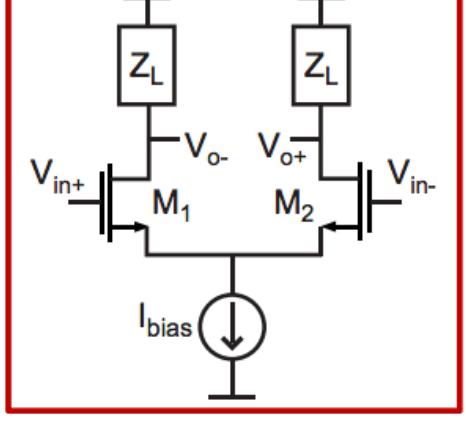
Common Source with Source Degeneration



Current Mirror



Differential Amplifier



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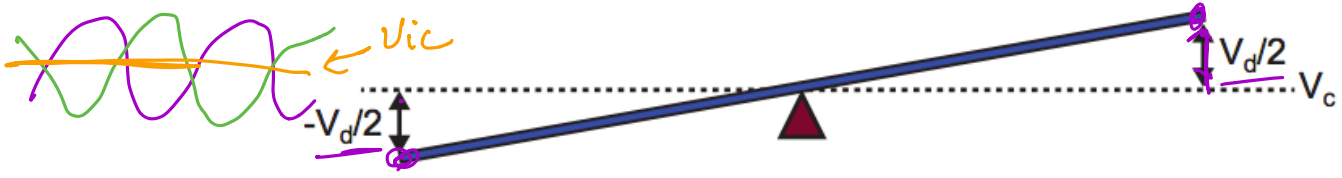
Differential & Common Mode Signals



- Consider positive and negative input terminal signals V_i^+ and V_i^-
- Define differential signal as: $V_{id} = V_{in}^+ - V_{in}^-$
- Define common mode signal as: $V_{ic} = (V_{in}^+ + V_{in}^-)/2$
- We can create arbitrary V_i^+ and V_i^- signals from differential and common mode components:

average value

$$V_{in}^+ = V_{ic} + \frac{1}{2}V_{id} \qquad V_{in}^- = V_{ic} - \frac{1}{2}V_{id}$$

- This also applies to differential output signals:

$$V_o^+ = V_{oc} + \frac{1}{2}V_{od} \qquad V_o^- = V_{oc} - \frac{1}{2}V_{od}$$

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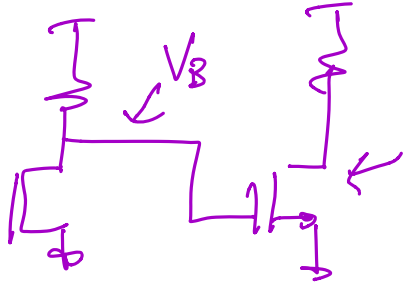
Why Differential?

- Differential circuits are much less sensitive to noises and interferences
- Differential configuration enables us to bias amplifiers and connect multiple stages without using coupling or bypass capacitors
- Differential amplifiers are widely used in IC's
  - Excellent matching of transistors, which is critical for differential circuits
  - Differential circuits require more transistors → not an issue for IC



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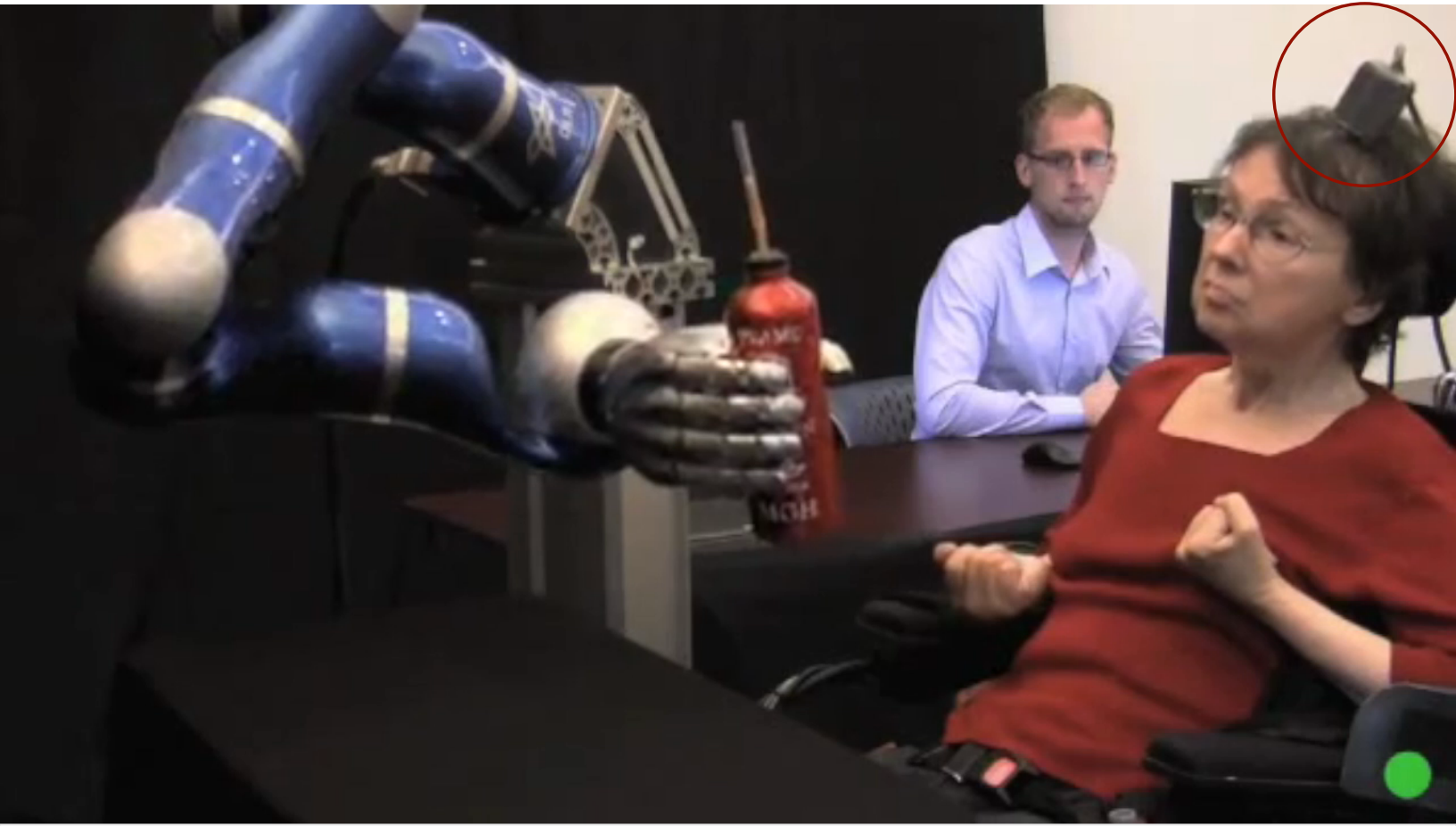
Brain-Machine Interfaces



Source: Hochberg et al., *Nature* '12

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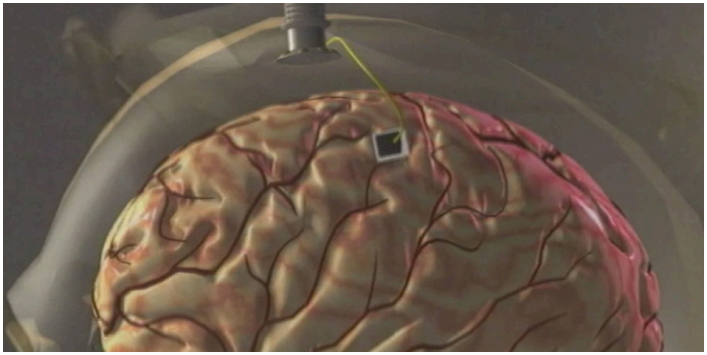
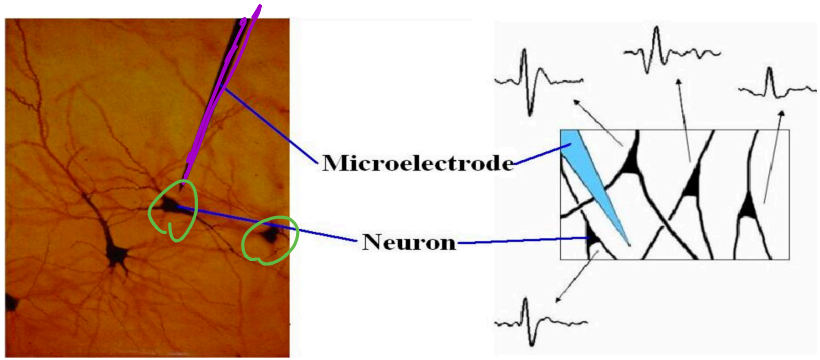
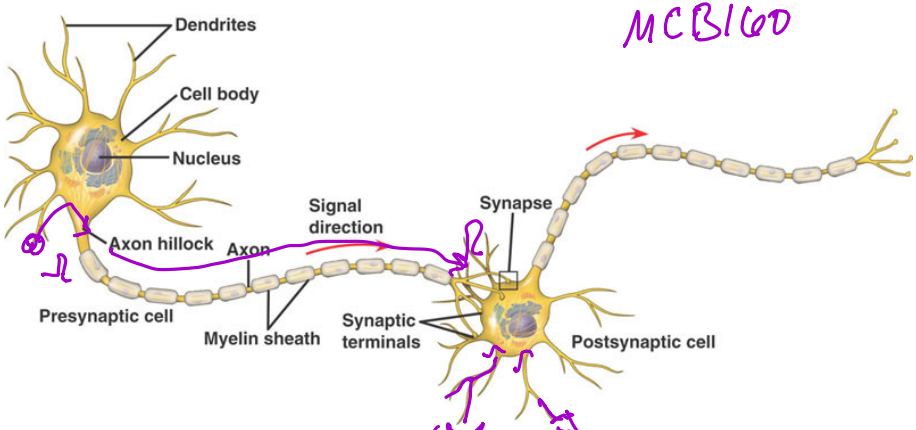
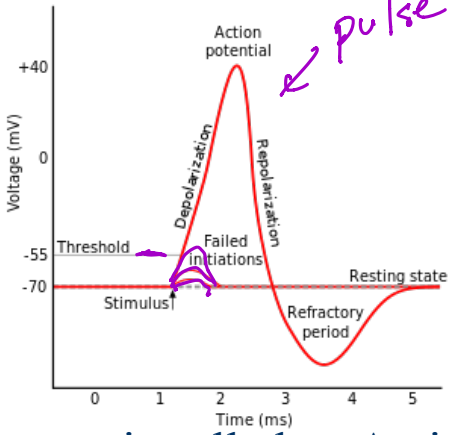
Neural Recording





- An array of electrodes is implanted in the motor cortex and senses extracellular signals that include firing from nearby neurons





- The propagation of signals from neuron to neuron is called an Action Potential, which is analogous to a digital "pulse"

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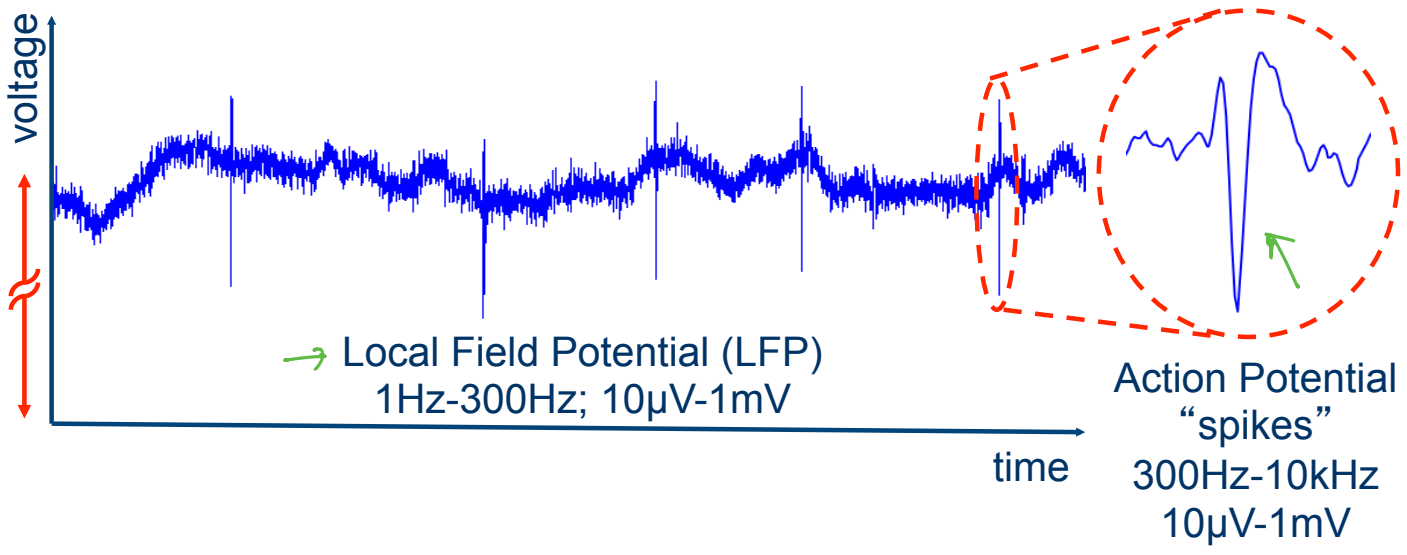
Extracellular Neuronal Signals



- The goal of a neural recording device is to record the small-amplitude neural signals and pick out the meaningful signals from the "noise".
- These signals are then decoded to create trajectories, movements, and speeds for controlling prostheses, computers, etc.

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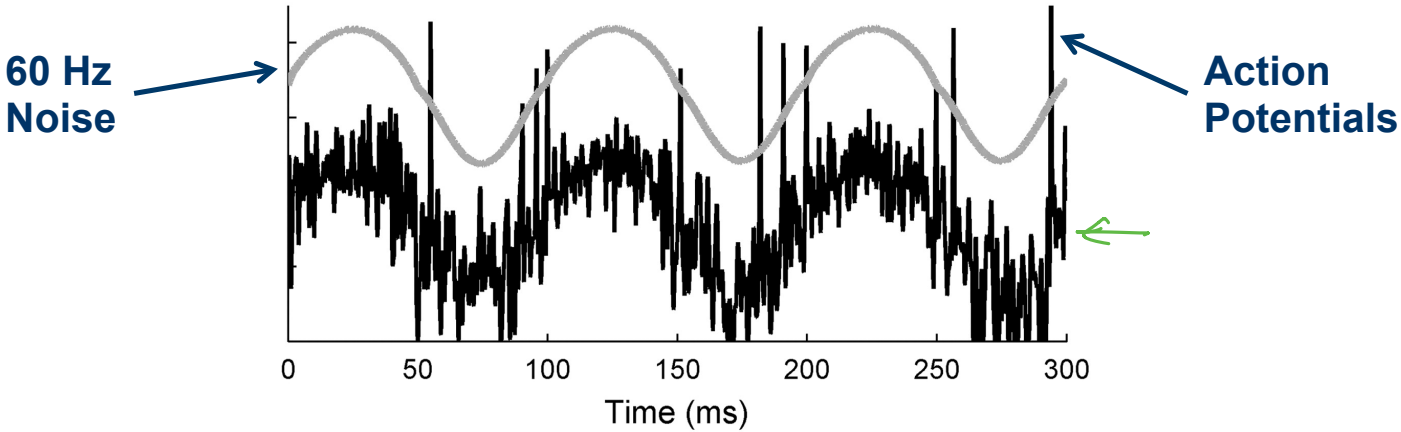
60Hz and Other Interferers



- In reality, the tiny signals recorded from the brain can get corrupted by numerous interferers.
- Ambient 60Hz noise couples into electrical signals in and on the body
- Motion can cause voltage artifacts from the movement of the electrodes relative to the neurons

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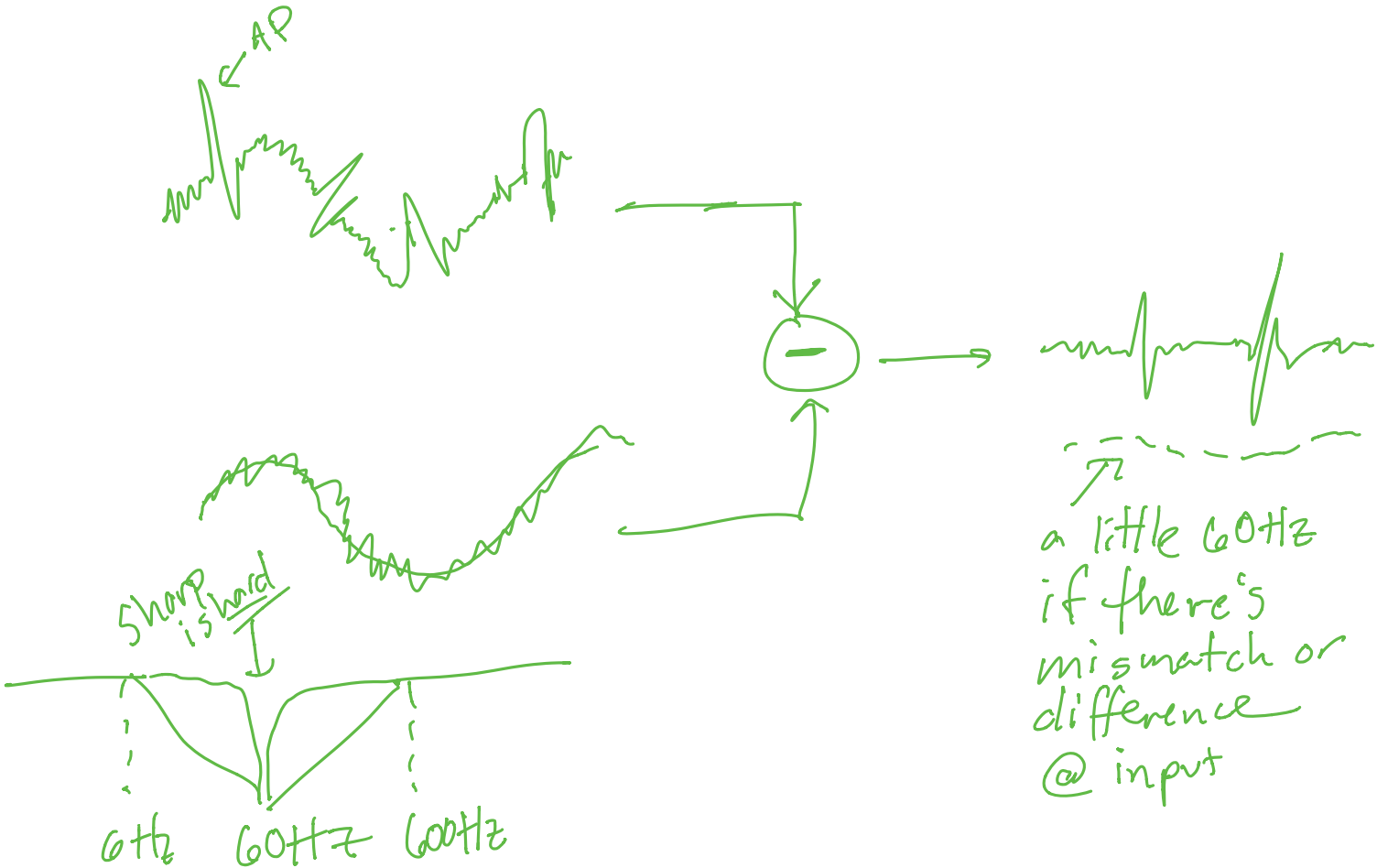
Key Idea: Differential Recording



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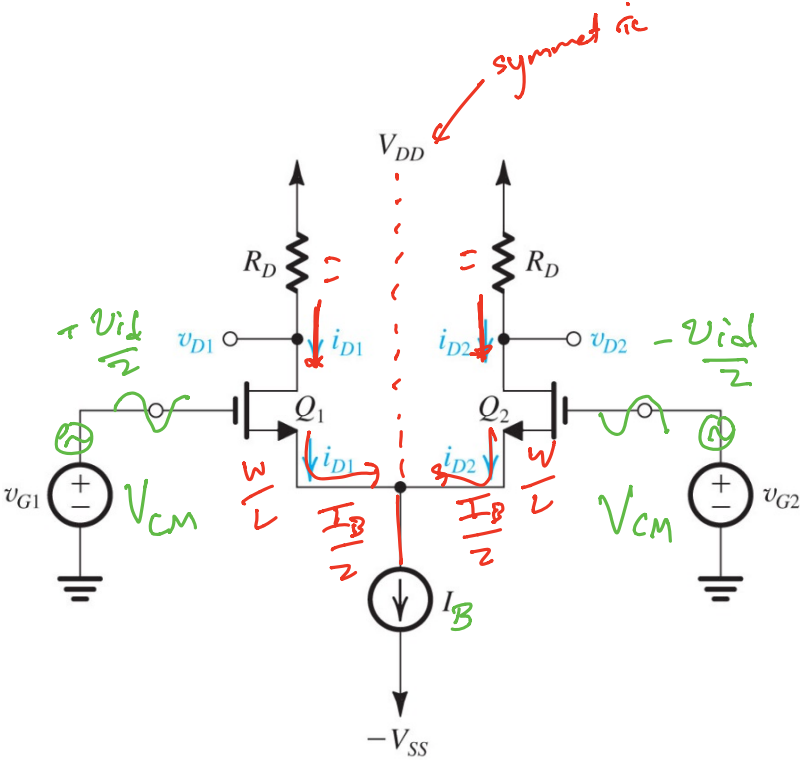
MOS Differential-Pair

Basic Configuration



Two matched MOS transistors

Common current bias

"Differential signls" applied to v_{G1} and v_{G2} (equal amplitude but opposite sign)

"Differential outputs" are produced at v_{D1} and v_{D2}

Note in differential configuration, V_{GS} is fixed for both Q_1 and Q_2

$$I_{D1} = I_{D2} = \frac{I}{2}$$

$$\frac{I}{2} = \frac{k_n}{2}\left(V_{GS} - V_{Tn}\right)^2$$

$$V_{GS} = V_{Tn} + \sqrt{\frac{I}{k_n}}$$

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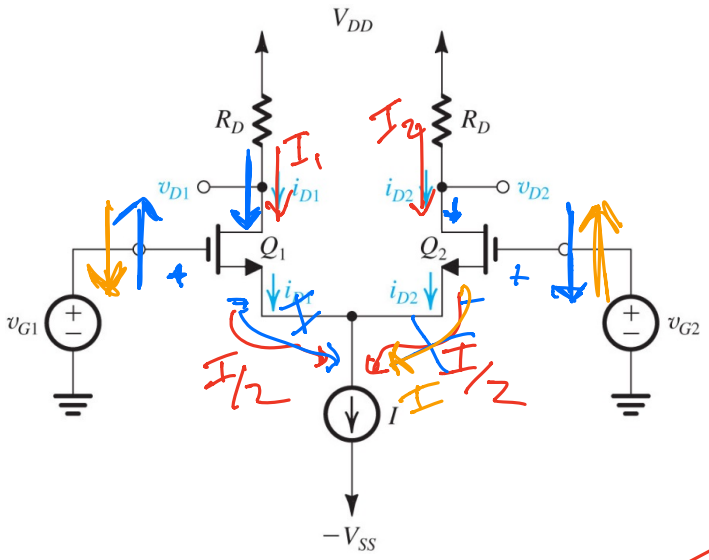
Large Signal Behavior of Diff Mode Operation



$$v_{id} = v_{in+} - v_{in-} = \left(V_{Tn} + \sqrt{\frac{I_1}{k_n}}\right) - \left(V_{Tn} + \sqrt{\frac{I_2}{k_n}}\right)$$

$$v_{id} = \sqrt{\frac{I_1}{k_n}} - \sqrt{\frac{I_2}{k_n}} = \sqrt{\frac{I/2 + \Delta i/2}{k_n}} - \sqrt{\frac{I/2 - \Delta i/2}{k_n}}$$

$$\Delta i = i_{D1} - i_{D2}$$

solve

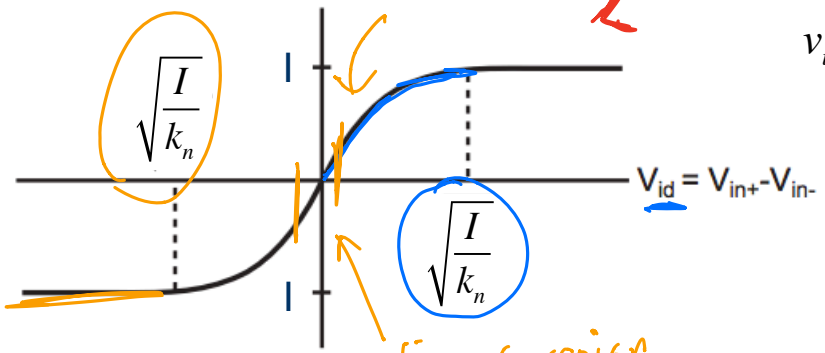
$$\Delta i = k_n v_{id} \sqrt{\frac{2I}{k_n} - v_{id}^2}$$

$$I_1 = \frac{I}{2} + \frac{\Delta i}{2}$$

$$I_2 = \frac{I}{2} - \frac{\Delta i}{2}$$

$$v_{id} \le \sqrt{\frac{I}{k_n}}$$

v_{id} small enough that Δi is linear



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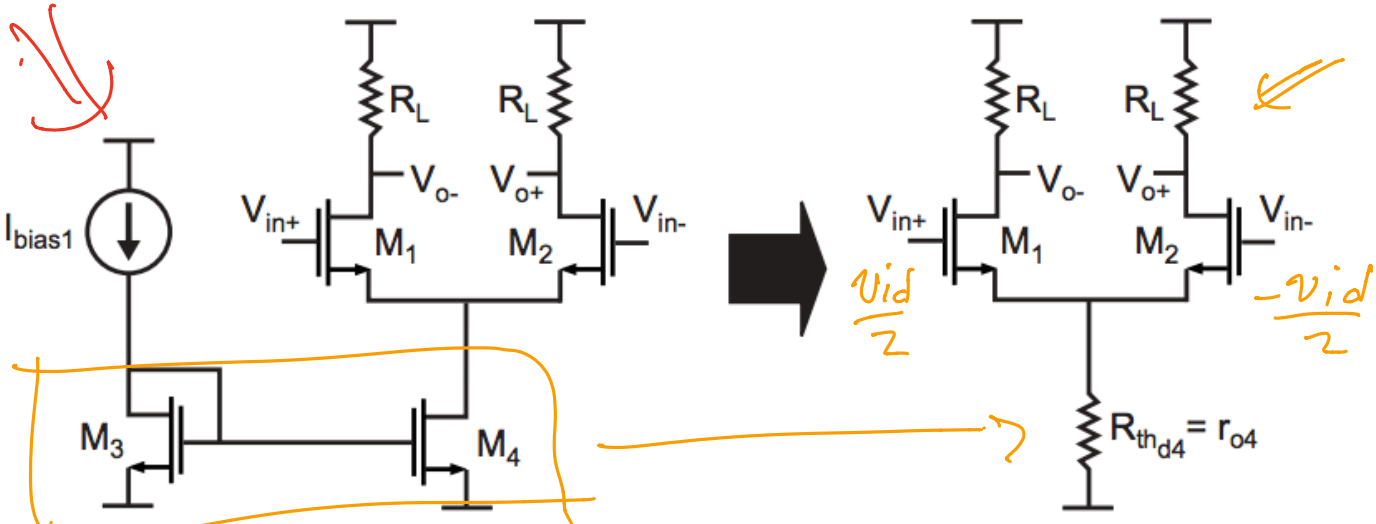
Small Signal Modeling: Step 1



- **Small signal analysis assumes linearity**
  - **Impact of M_4 on amplifier is to simply present its drain impedance to the diff pair transistors (M_1 and M_2)**
  - **Impact of V_{in+} and V_{in-} can be evaluated separately and then added (i.e., superposition)**
    - By symmetry, we need only determine impact of V_{in+}
      - Calculation of V_{in-} impact directly follows

Courtesy: M.H. Perrott

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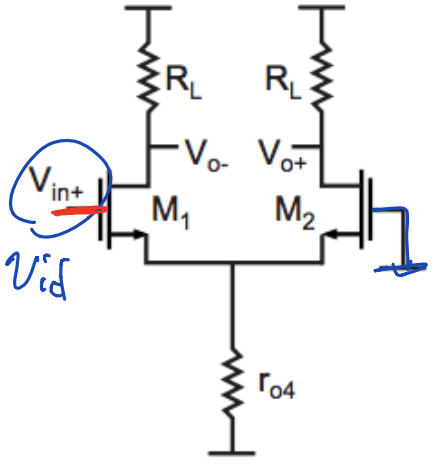
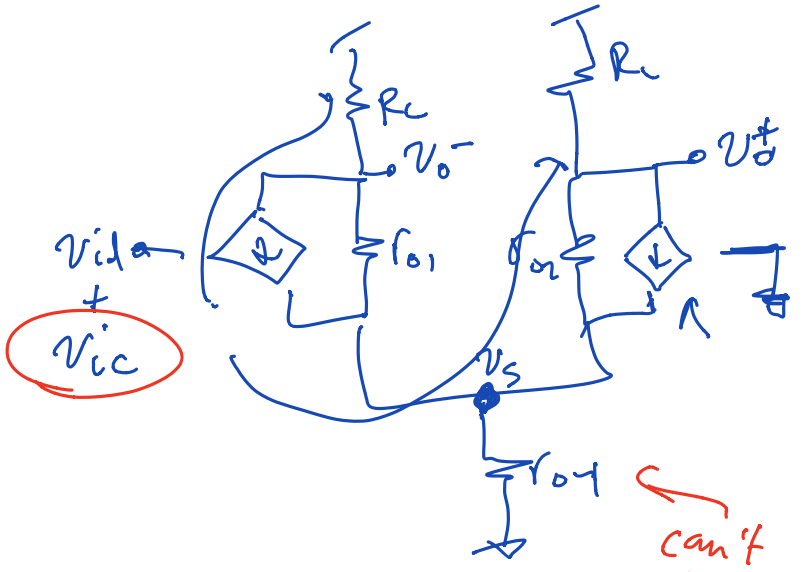
Method 1: Use Small Signal Model





Write KCL

v_o^-, v_o^+

$v_{id} = v_o^+ - v_o^-$

- Analysis follows easily, but there is a simpler way!

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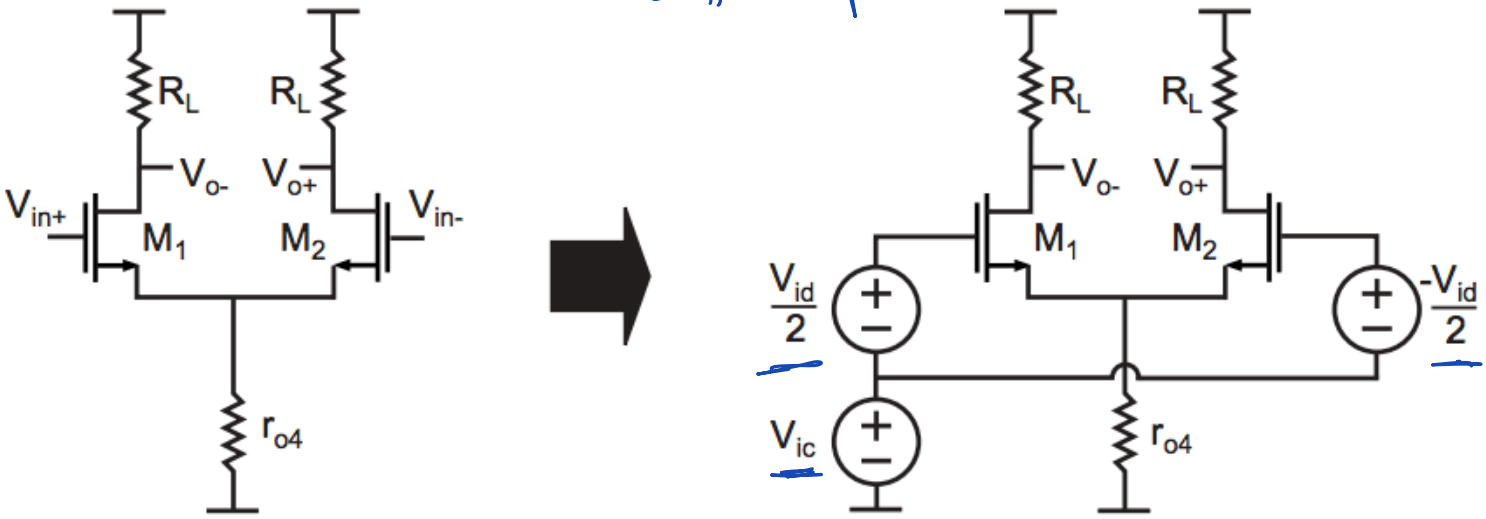
Method 2: Differential Amplifier Analysis

"diff amp"



- Partition input signals into common-mode and differential components
- By superposition, we can add the results to determine the overall impact of the input signals

Courtesy: M.H. Perrott

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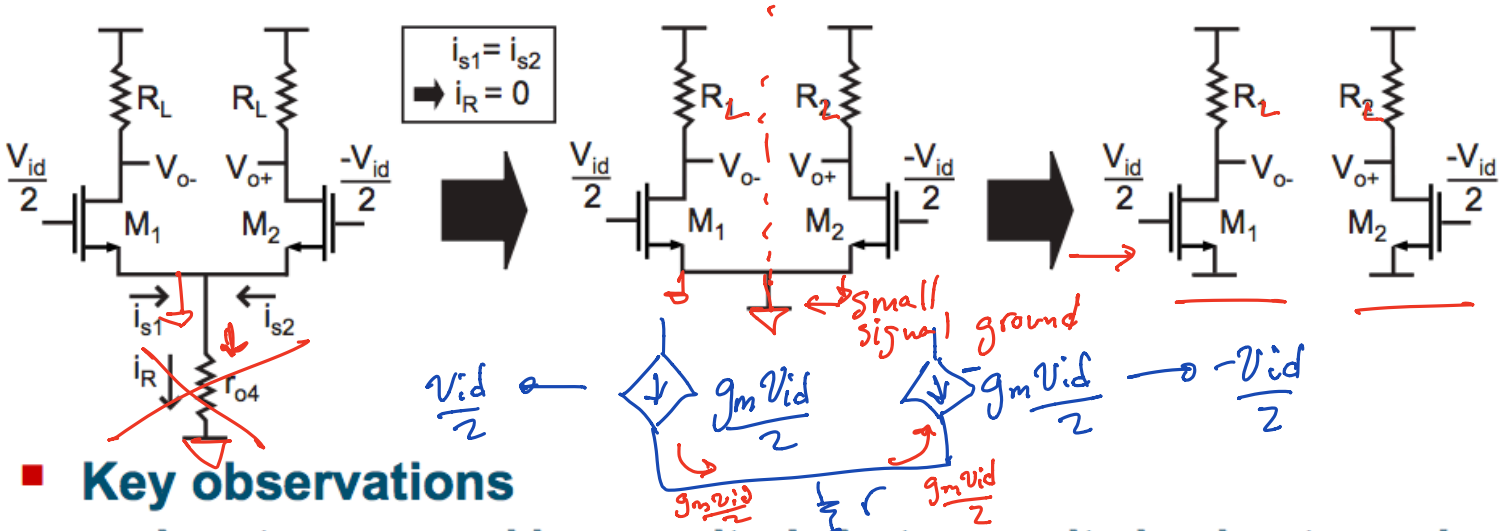
Differential Analysis



- **Key observations**
  - **Inputs are equal in magnitude but opposite in sign to each other**
  - **By linearity and symmetry, i_{s1} must equal $-i_{s2}$**
    - This implies i_R is zero, so that voltage drop across r_{o4} is zero
      - The sources of M_1 and M_2 are therefore at incremental ground and decoupled from each other!
- **Analysis can now be done on identical "half-circuits"**

Courtesy: M.H. Perrott

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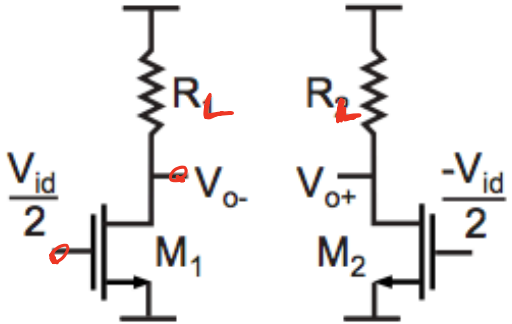
Find Differential Gain



$g_{m1} = g_{m2}$

$r_{o1} = r_{o2}$

$$\frac{v_o^-}{\frac{v_{id}}{2}} = -g_{m1}(r_{o1} \| R_L)$$

$$\frac{v_o^+}{\frac{-v_{id}}{2}} = -g_{m2}(r_{o2} \| R_L)$$

$$\frac{v_o^-}{\frac{v_{id}}{2}} = -g_m(r_o \| R_L)$$

$$\frac{v_o^+}{\frac{-v_{id}}{2}} = -g_m(r_o \| R_L)$$

$$\frac{v_{od}}{v_{id}} = \frac{v_o^+}{v_{id}} - \frac{v_o^-}{v_{id}} = -\frac{1}{2}g_m(r_o \| R_L) - \frac{1}{2}g_m(r_o \| R_L)$$

$$= -g_m(r_o \| R_L)$$

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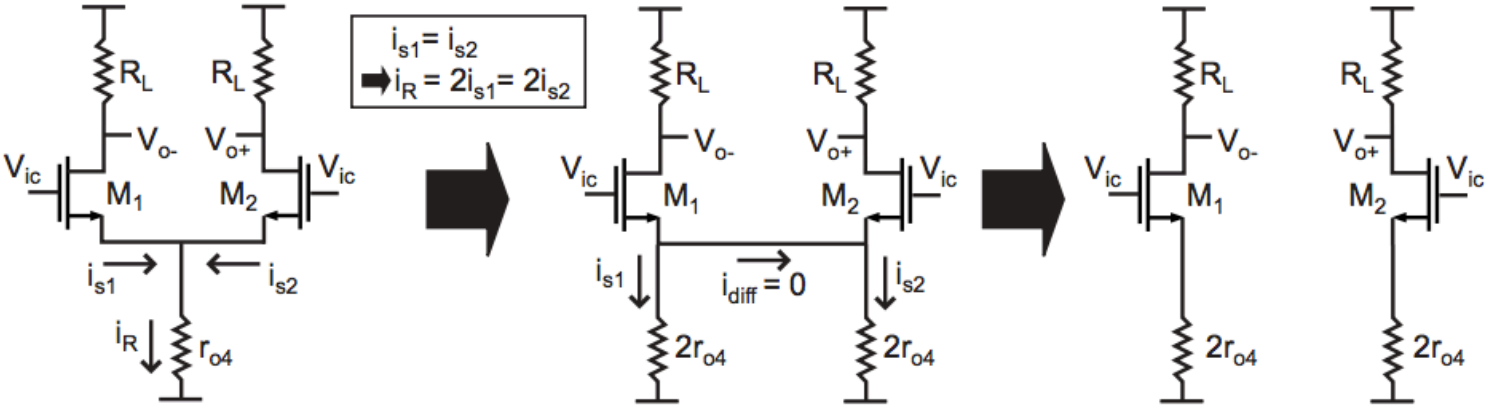
Common Mode Analysis



- **Key observations**
  - **Inputs are equal to each other**
  - **By linearity and symmetry, i_{s1} must equal i_{s2}**
    - This implies $i_R = 2i_{s1} = 2i_{s2}$
  - **We can view r_{o4} as two parallel resistors that have equal current running through them**
- **Analysis can also be done on two identical half-circuits**

Courtesy: M.H. Perrott

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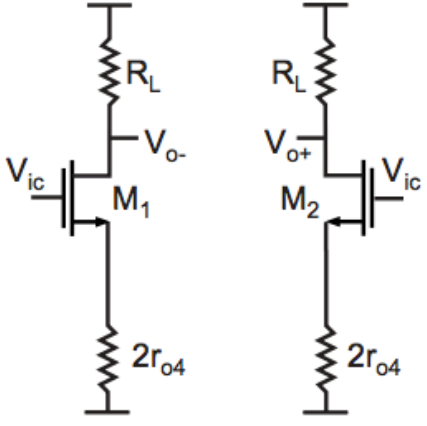
Common Mode Analysis



Common-Source with degeneration

$$\frac{v_{o-}}{v_{ic}} = \frac{v_{o+}}{v_{ic}} = \frac{-R_L}{1/g_m + 2r_{o4}} = \frac{-g_m R_L}{1 + 2g_m r_{o4}}$$

Since $2r_{o4} >> 1/g_m$,

$$\frac{v_{o-}}{v_{ic}} = \frac{v_{o+}}{v_{ic}} \approx \frac{-R_L}{2r_{o4}}$$

$$v_{od} = v_{o+} - v_{o-} = 0$$

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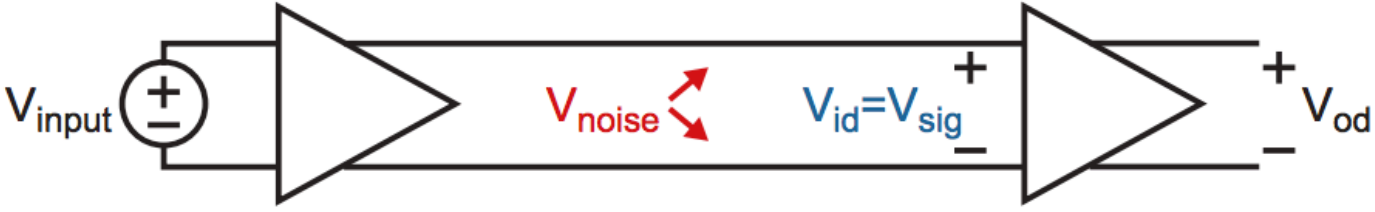
Useful Metric for Diff Amps: CMRR



- **Common Mode Rejection Ratio (CMRR)**
  - **Define: a_{vd}: differential gain, a_{vc}: common mode gain**

$$\text{CMRR} = \left(\frac{a_{vd}}{a_{vc}} \right)$$

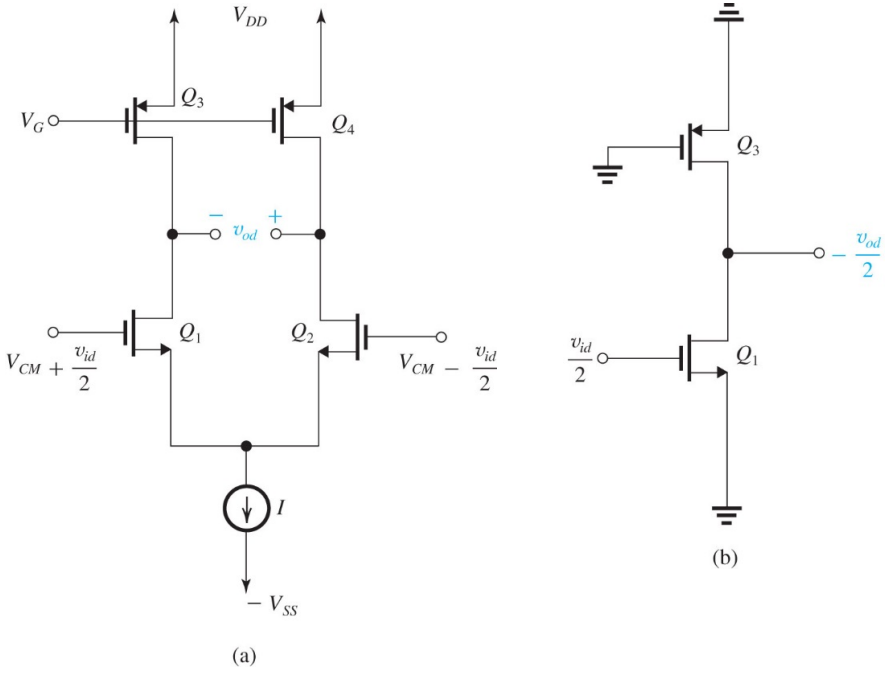
  - **CMRR corresponds to ratio of differential to common mode gain and is related to received signal-to-noise ratio**

$$V_{od} = a_{vd} V_{sig} + a_{vc} V_{noise}$$

$$\Rightarrow \frac{Signal}{Noise} = \left(\frac{a_{vd}}{a_{vc}} \right) \left(\frac{V_{sig}}{V_{noise}} \right) = \text{CMRR} \left(\frac{V_{sig}}{V_{noise}} \right)$$

Courtesy: M.H. Perrott

Current-Source Loads

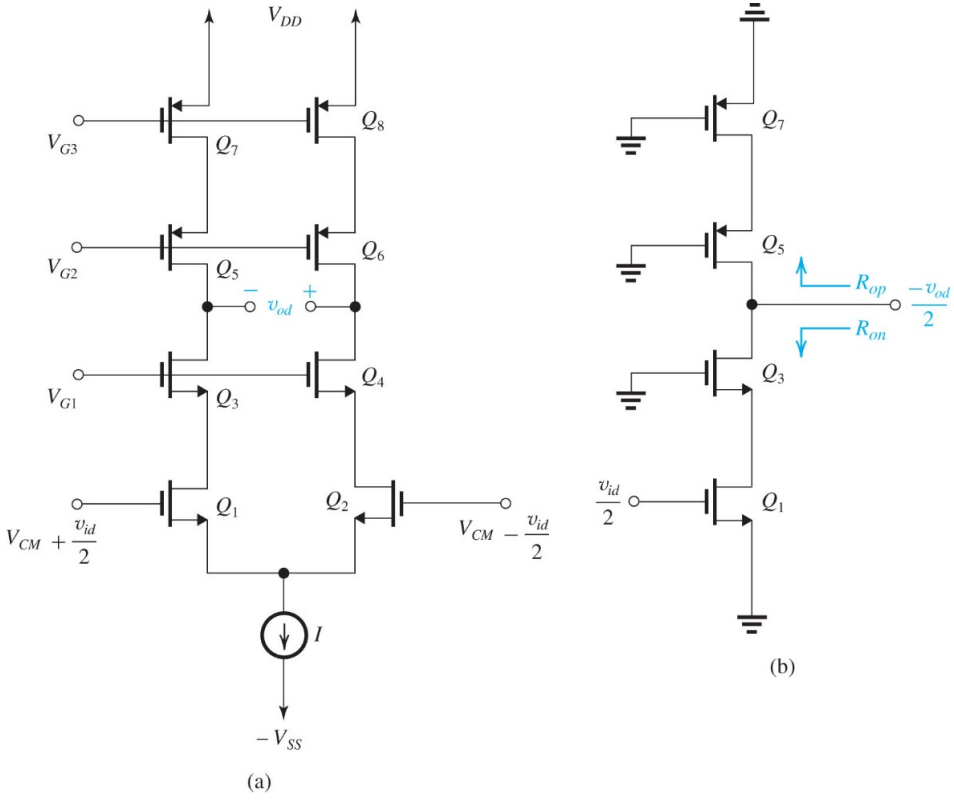


Q_3 and Q_4 are PMOS current sources

From half-circuit:

$$A_d = \frac{v_{od}}{v_{id}} = -g_{m1}\left(r_{o1} \parallel r_{o3}\right)$$

Cascode Differential Amplifier



Cascode configurations for both amplifying transistors and current source loads.

From half-circuit

$$A_d = \frac{v_{od}}{v_{id}} = g_{m1}\left(R_{on} \parallel R_{op}\right)$$

$$R_{on} = \left(g_{m3} r_{o3}\right) r_{o1}$$

$$R_{op} = \left(g_{m5} r_{o5}\right) r_{o7}$$

If all transistors are identical,

$$R_{on} = R_{op} = g_m r_o^2$$

$$A_d = \frac{1}{2} g_m^2 r_o^2$$

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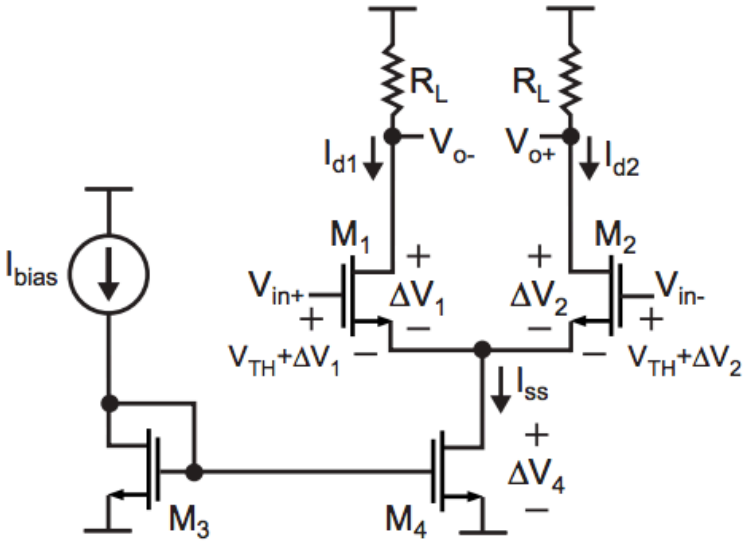
Prof. Rikky Muller

Common Mode Voltage Range



- **While keeping all devices in saturation:**
  - **What is the maximum common mode output range?**
    - Assume $V_{id} = 0$
  - **What is the maximum common mode input range?**
    - Assume $V_{od} = 0$

Courtesy: M.H. Perrott