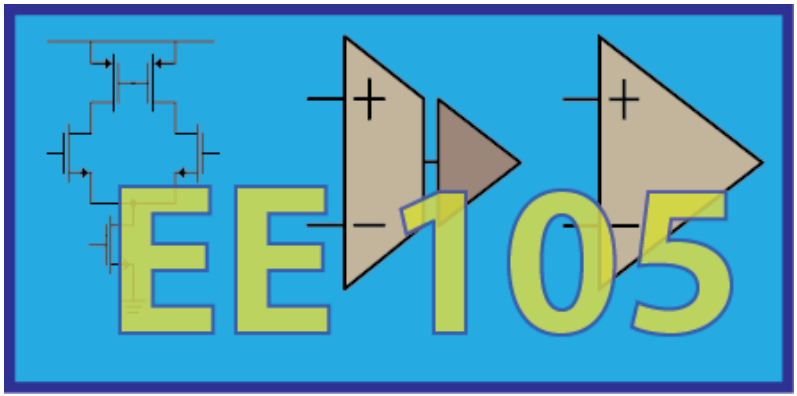

Multi-stage Amplifiers

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Announcements

- HW10 due on Friday
- Lab 5 due this week
- 2 weeks of lecture left!

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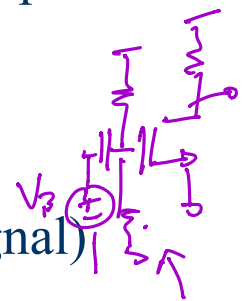
Multistage Amplifiers

Why cascade single-stage amplifier stages?

- More gain !
  - Gain/stage limited, especially in nanoscale devices
- Input/output resistance matching
  - Source/load impedance may be too high/low
- Improve Bandwidth
  - De-couple high impedance nodes from large capacitors
- Output stages to drive "external" loads
- DC coupling (no passive elements to block the signal)
  - Use amplifiers to naturally "level shift" signal



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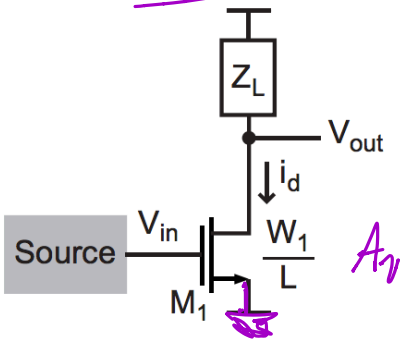
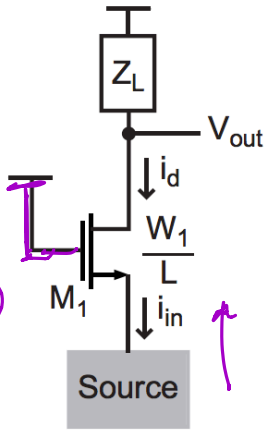
1-Stage Amplifier Types

Common Source

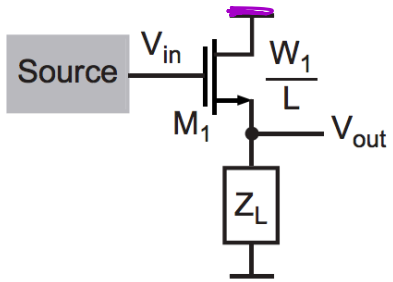


$A_V \sim -g_m (Z_L \| r_o)$

Common Gate

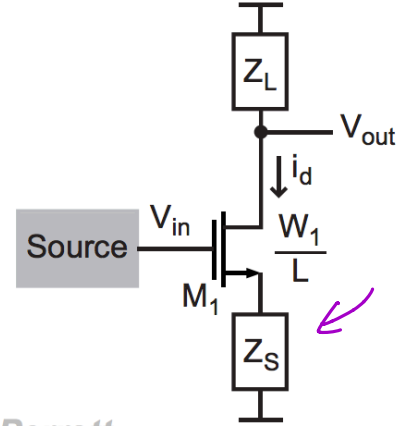


Source Follower → CD



$A_V \sim 1$

Common Source with Source Degeneration



Courtesy M.H. Perrott

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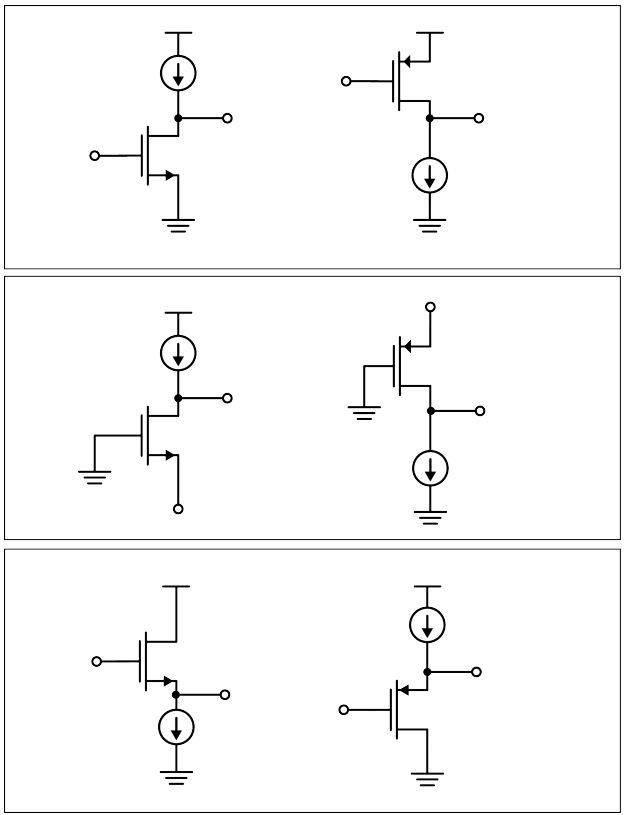
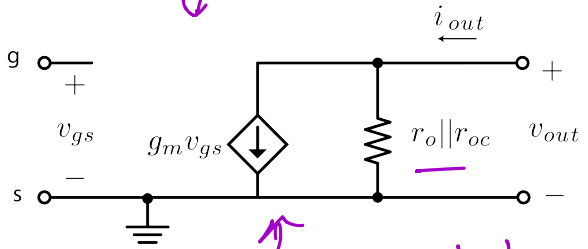
Transistor Amplifiers → Gm/V/I



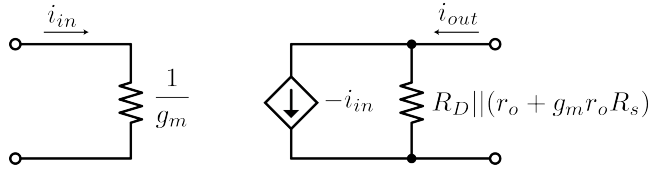
2-port models



CS

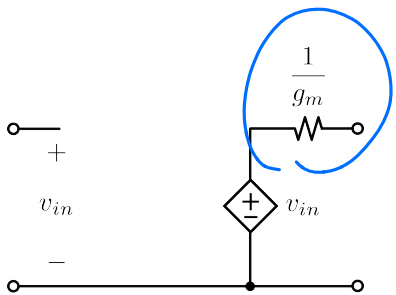
Gm Amplifier Common Source

CS model



CG

I-Buffer Common Gate



V-Buffer Source Follower

CD

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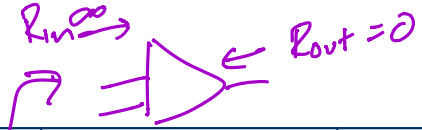
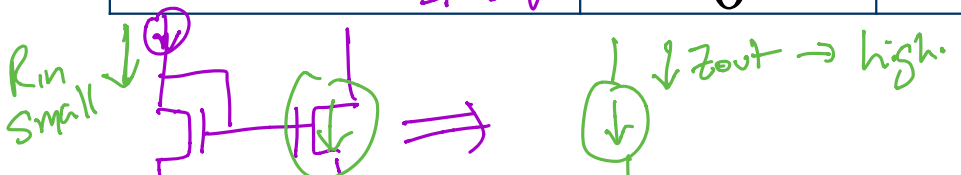
Impedance "Match"

- On-chip circuits often use "voltage/current" matching to minimize loading
- Keep in mind the input resistance and output resistance of each type of stage so that the loading does not create an undesired effect



Amp type	R_{in}	R_{out}
Voltage:	∞	0 ← ideal
Current:	0 ←	∞
Transconductance: V → I	∞ ↑	∞ ↑ opposite
Transresistance: I → V	0 ↓	0 ↓



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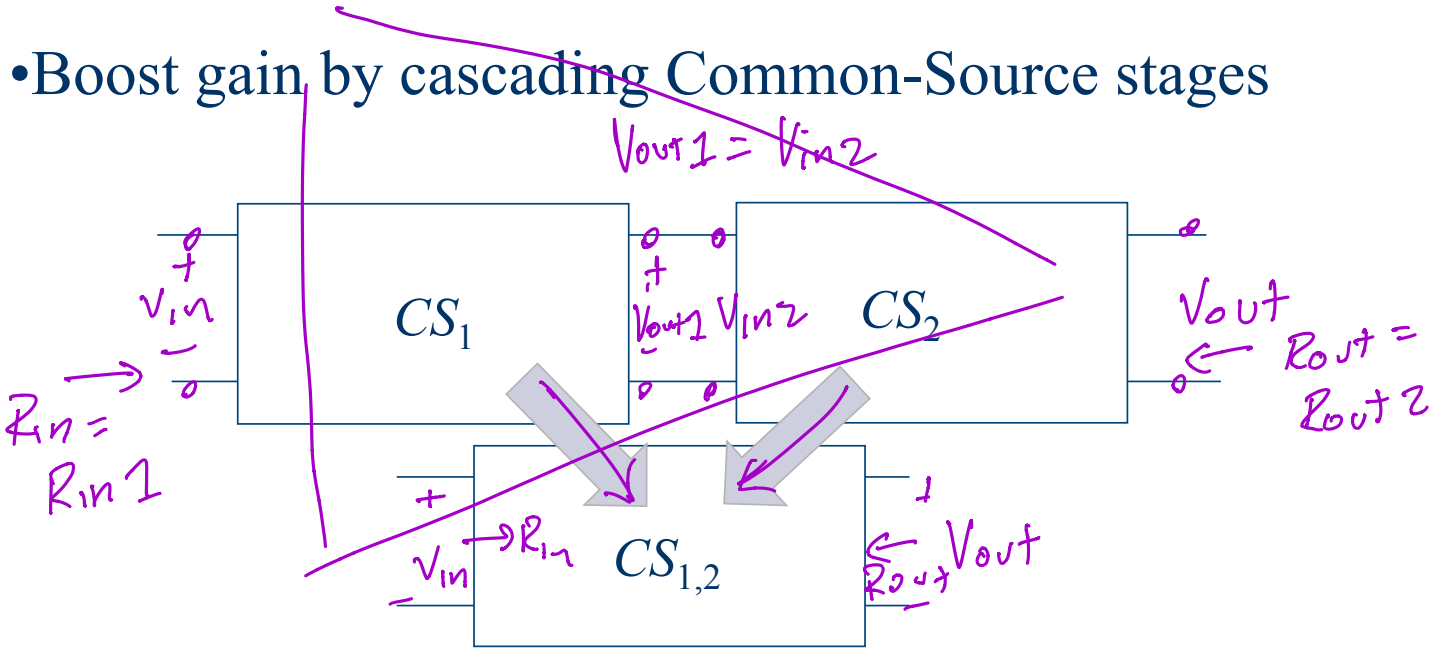
Two-Stage Voltage Amplifier

- Boost gain by cascading Common-Source stages



Can combine into a single 2-port model

Results of new 2-port: $R_{in} = R_{in1}$, $R_{out} = R_{out2}$

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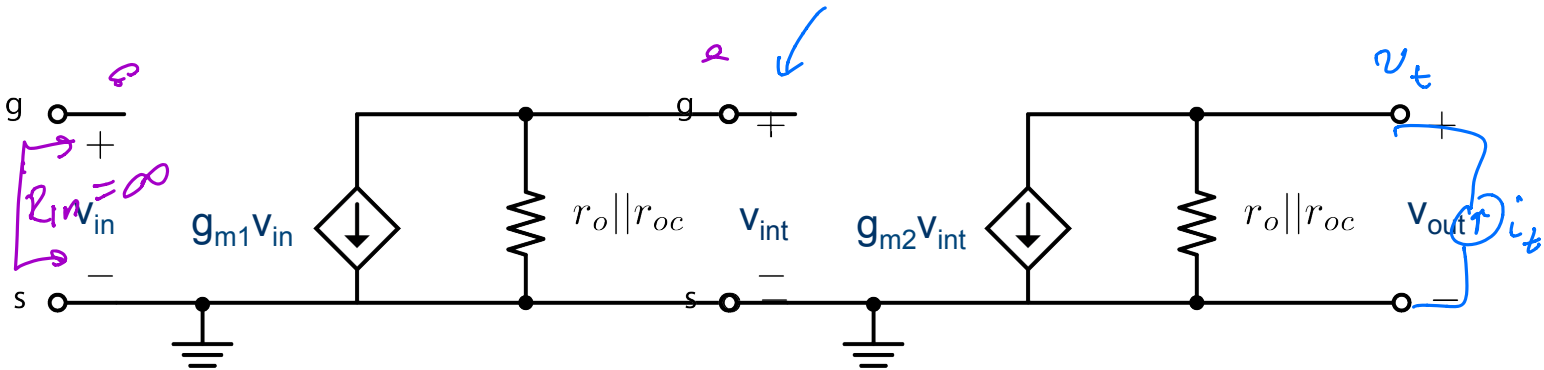
CS Cascade Analysis



Results of new 2-port:

$R_{in} = R_{in1} = \infty$

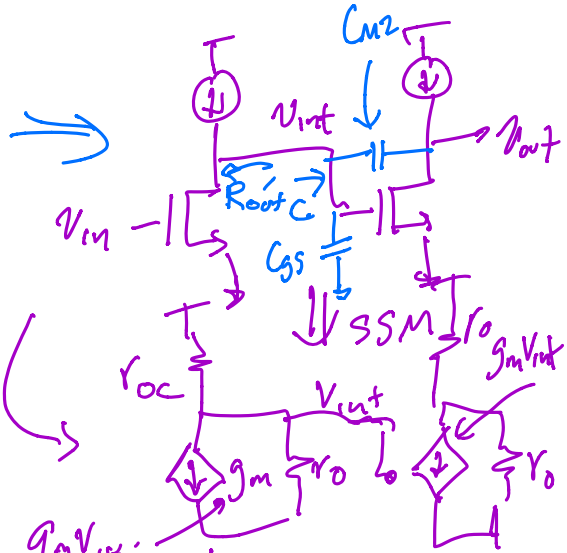
$R_{out} = R_{out2} = r_o // r_{oc}$

$A_V = v_{out}/v_{in} =$

gain of CS

$\frac{v_{out}}{v_{in}} = \frac{v_{int}}{v_{in}} \cdot \frac{v_{out}}{v_{int}} = -g_{m1}(r_o // r_{oc})$

$\times -g_{m2}(r_o // r_{oc})$



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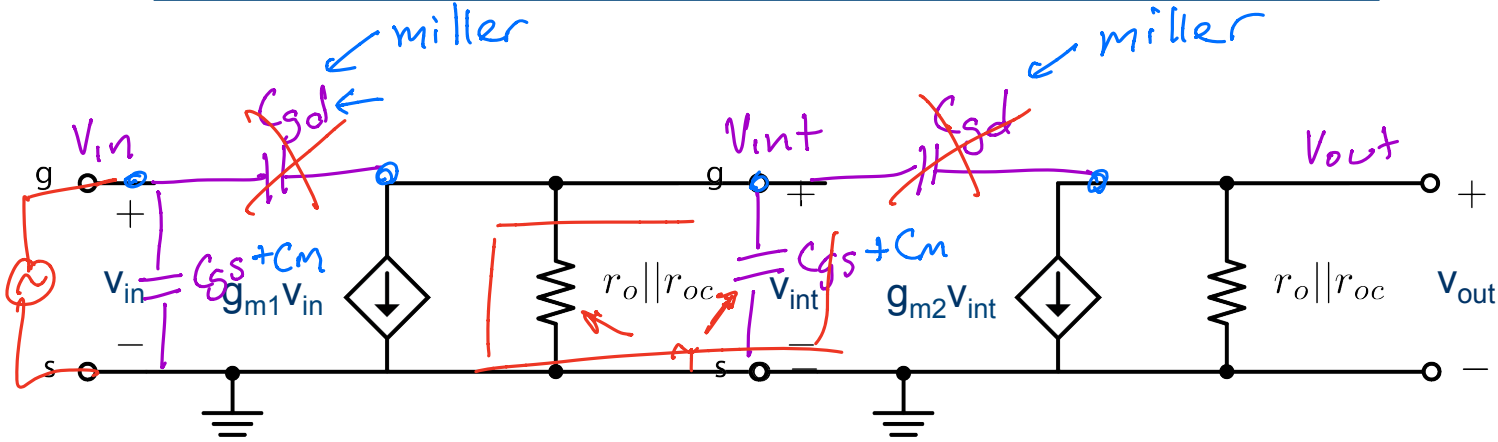
$= g_{m1} g_{m2} (r_o \| r_{oc})^2$

CS Cascade Bandwidth



$C_{M1} = C_{gd}(1-A) = C_{gd}(1+g_{m1}(r_o \| r_{oc}))$

$C_{M2} = C_{gd}(1+g_{m2}(r_o \| r_{oc}))$

$C \| R \Rightarrow \dfrac{\frac{1}{Cs} \cdot R}{\frac{1}{Cs}+R} = \dfrac{R}{RCs+1}$

$\omega_p = \frac{1}{RC}$

$\tau = RC$

- every capacitor in the signal path produces a pole
- look for largest τ associated w/ caps

Two time constants:

$\tau_1 = (C_{gs}+C_{M2}) \cdot (r_o \| r_{oc})$ (BIG) (BIG)

$\tau_2 = 0$

↖ cascaded high Rout' with high $C_{in} \Rightarrow$ large τ

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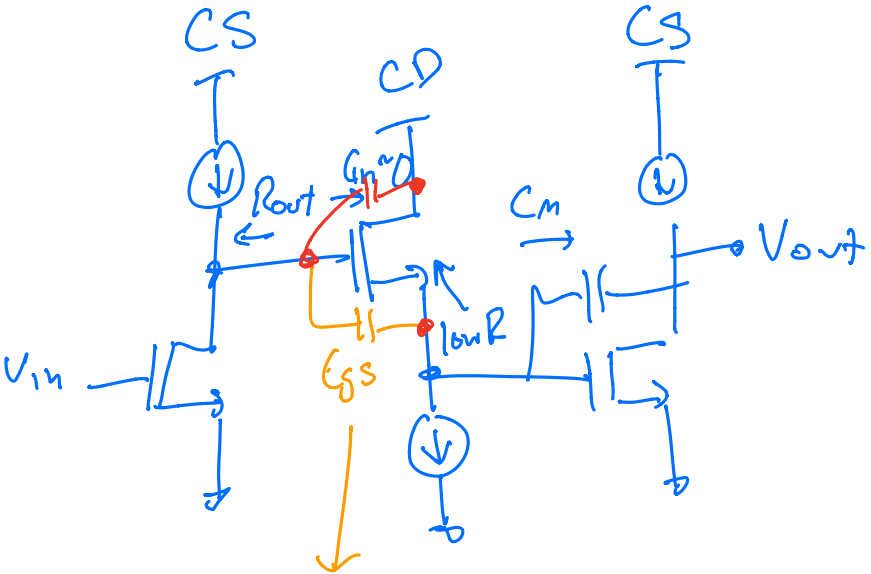
Bandwidth Extension

- Common Source stage has high gain, but low bandwidth
- Note that Miller effect is the culprit
- Follower stage can buffer source resistance from Miller cap



CD

$A_v \approx 1$

$R_{out} \approx \frac{1}{g_m}$

$R_{in} \sim \infty$

$C_{in} \to 0$

$$C_M = C_{gs}(1-A) \approx 0$$

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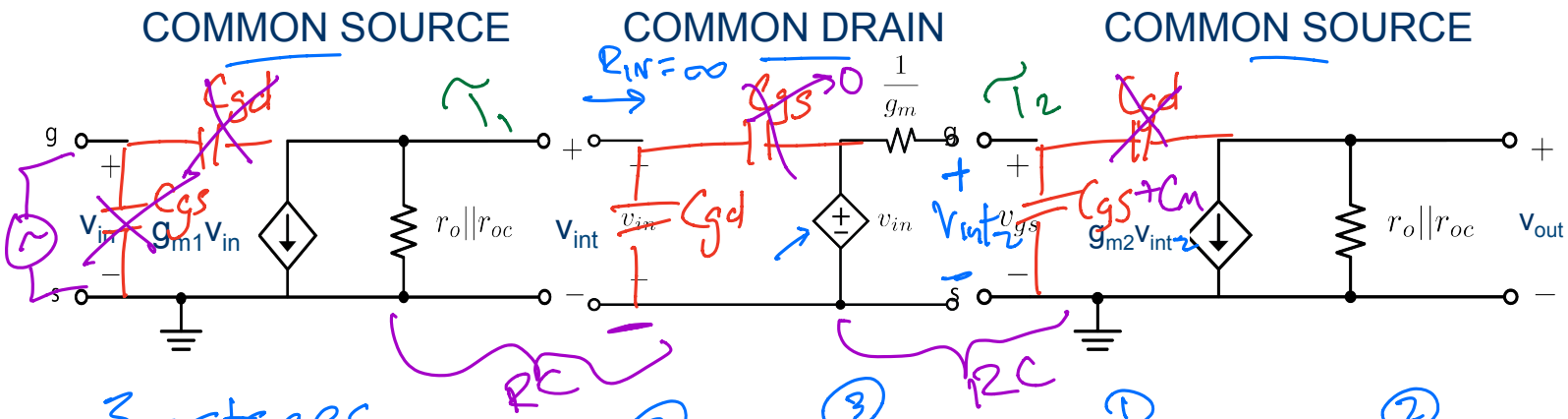
Bandwidth Extension Using SF



3-stages

$$\frac{V_{out}}{V_{in}} = \frac{V_{int}}{V_{in}} \cdot \frac{V_{int2}}{V_{int}} \cdot \frac{V_{out}}{V_{int2}} = -g_{m1}(r_o||r_{oc}) \cdot 1 \cdot \left(-g_{m2}(r_o||r_{oc})\right)$$

$$= g_{m1}g_{m2}(r_o||r_{oc})^2$$

unchanged

$$\tau_1 = C_{gd}(r_o||r_{oc})$$

$$\tau_2 = \frac{1}{g_m}\left(C_{gs} + C_{gd}\left(1 + g_{m2}(r_o||r_{oc})\right)\right)$$

BIGGER!

Both are smaller than slide 9

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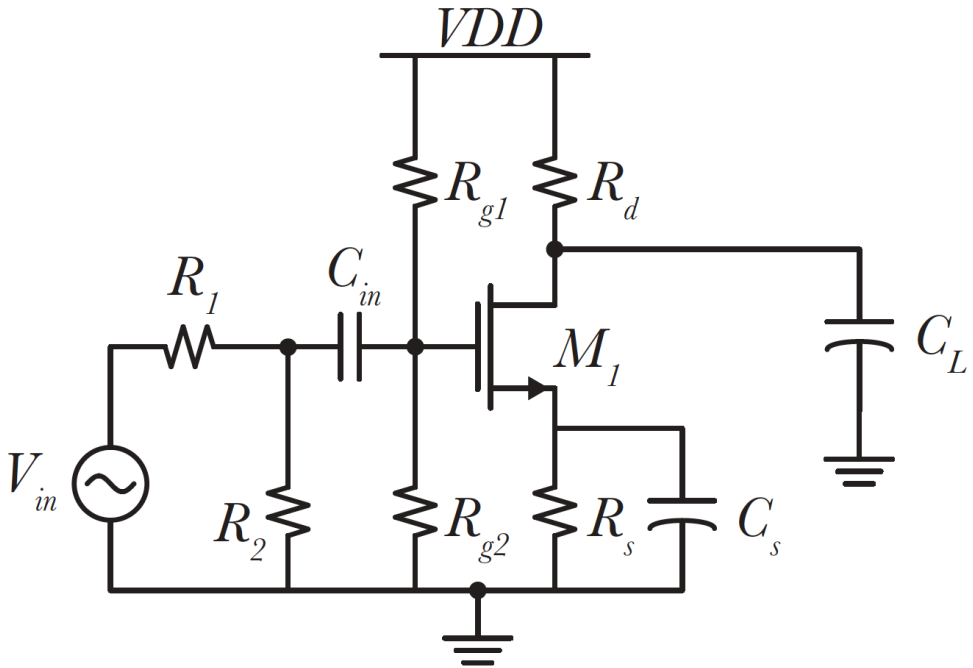
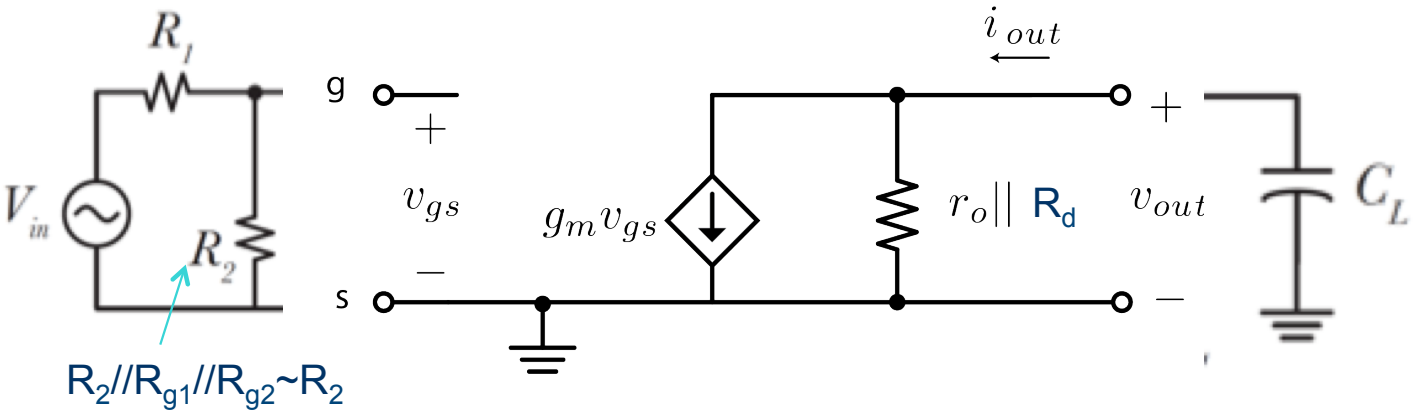
CS Example with Cap Load



- C_{in} and C_S are very large, therefore they look like short circuits to the AC signal.
- If C_L is very large, its pole dominates, let's analyze

CS with Cap Load– Small Signal



- What are the time constants associated with the capacitors in this circuit?
- What can we do if we have to drive a large C_L?

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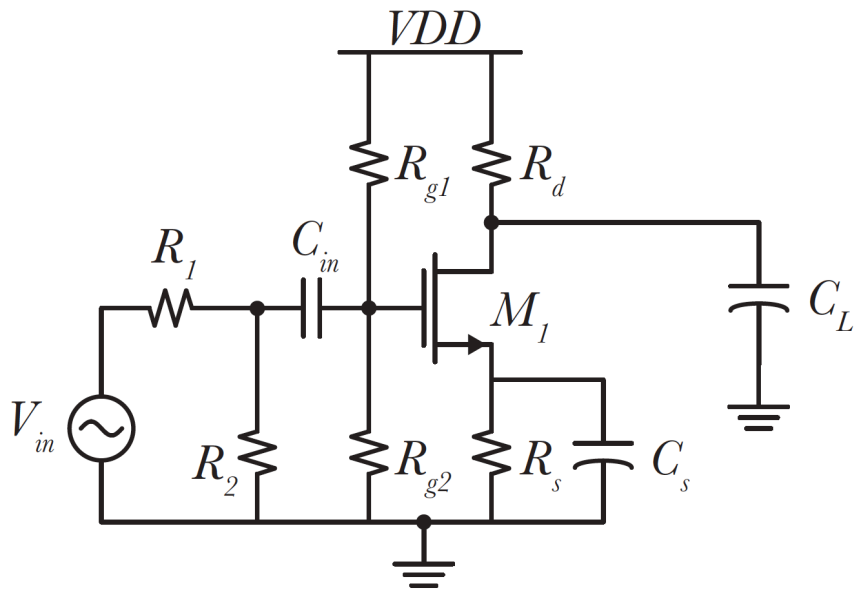
CS with Cap Load – Bandwidth



- How can we reduce the impact of C_L?
- One way is to reduce the resistance R_d, but this reduces our low-frequency gain
- To recover the gain we can increase g_{m1}. *What does this cost us?*

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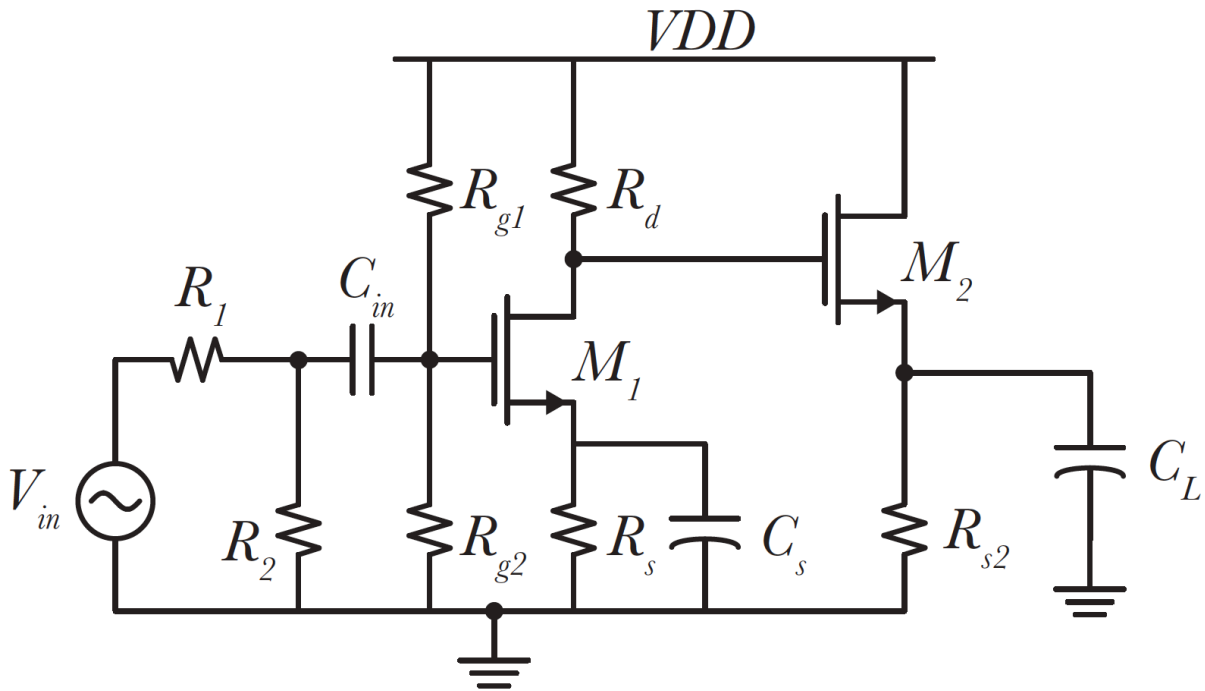
CS with Cap Load – BW Extension



- A better way to extend the bandwidth is to add a source-follower stage.
- Similar to previous example

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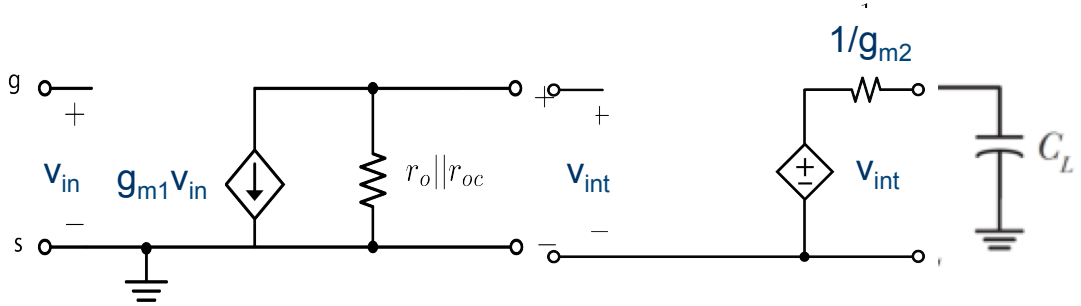
CS with Cap Load – BW Extension



- By adding a CD (Source Follower) we can increase the bandwidth
- It costs us power for the CD stage
- Remember that increasing the BW by increasing g_{m1} costs us much more

$V_B > 2V_{GS} - V_T = V_{DSAT} + V_{GS}$

$V_{GS} - V_T$

$V_{DS} > V_{GS} - V_T = V_{DSAT}$

V_{GS} — M1

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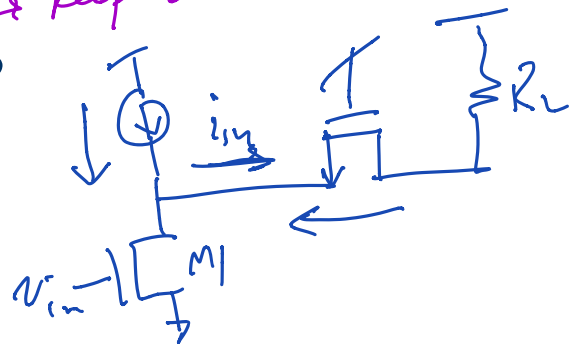
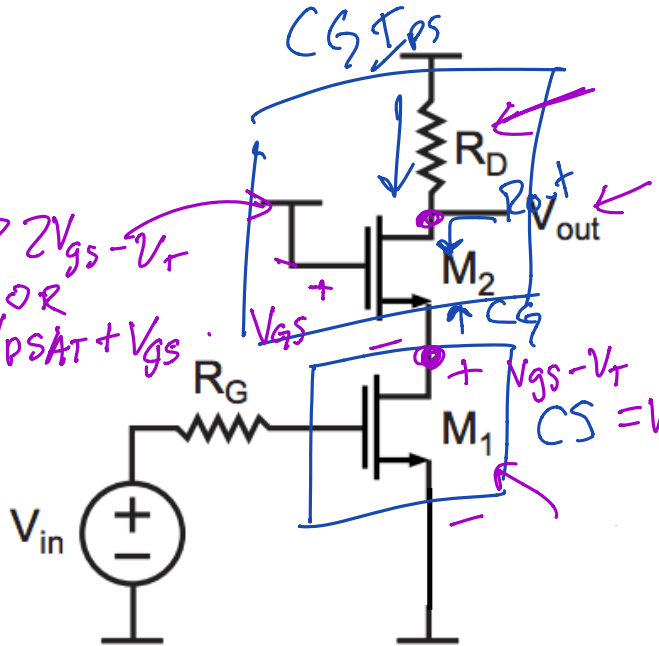
CS + CG

- Common source provides gain, CG acts as a buffer, but is it even helping?
- How do you bias this circuit?

keep devices saturated





$V > 2V_{gs} - V_T$ OR $V_{DSAT} + V_{gs}$

V_{gs}

$V_{gs} - V_T$

$I_{DS} \rightarrow$ CG & CS

CS $= V_{DSAT}$

Cascode → current mirrors

Cascode = high R_{out}

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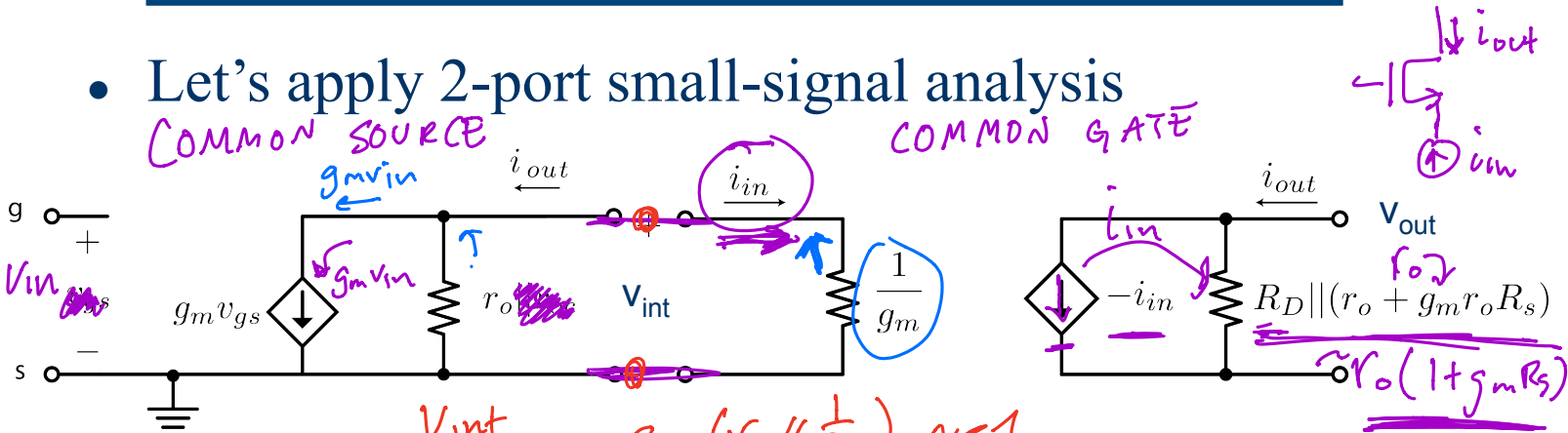
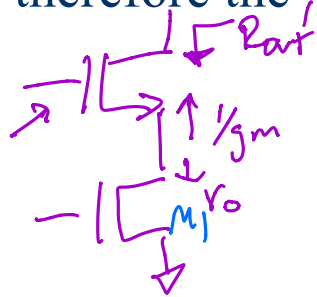
Merged CS + CG = Cascode

Amplifier

- Let's apply 2-port small-signal analysis



- In this case, we care about the *input current* to the second stage
- Note that the input resistance of the CG is low, therefore the majority of the CS current is fed to the CG
- $A_v = \frac{V_{out}}{V_{in}} = \frac{i_{in}}{V_{in}} \cdot \frac{V_{out}}{i_{in}} = -g_{m1}\left(\frac{r_o}{r_o + 1/g_m}\right) \cdot$ ... $\approx -g_{m1} R_{out}$



We can achieve high gain!

$R_D || r_o(1+g_m R_s)$ = R_{out}

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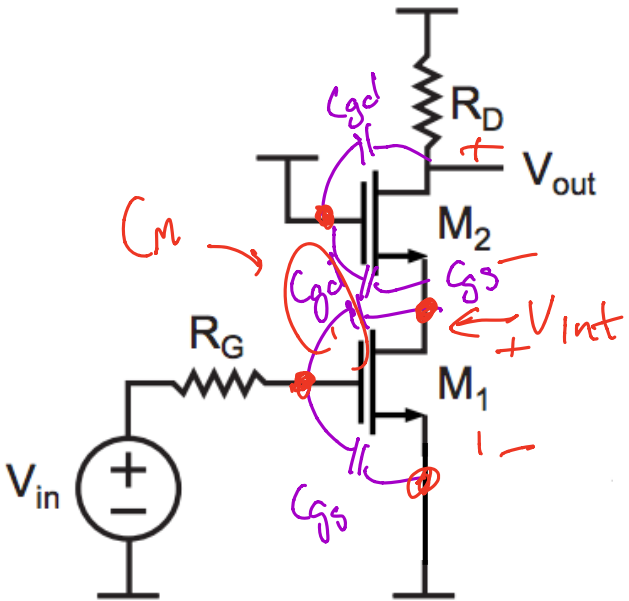
Cascode Bandwidth

- Draw in the C_{gs} and C_{gd} capacitors.
- Which ones are Miller effected?
- Is this better or worse than a CS without a CG?



Cost of cascode = swing

$C_{gd}(1-A)$

$A = \frac{V_{int}}{V_{in}} \approx -1$

$C_M = C_{gd}(1+1) \approx 2C_{gd}$

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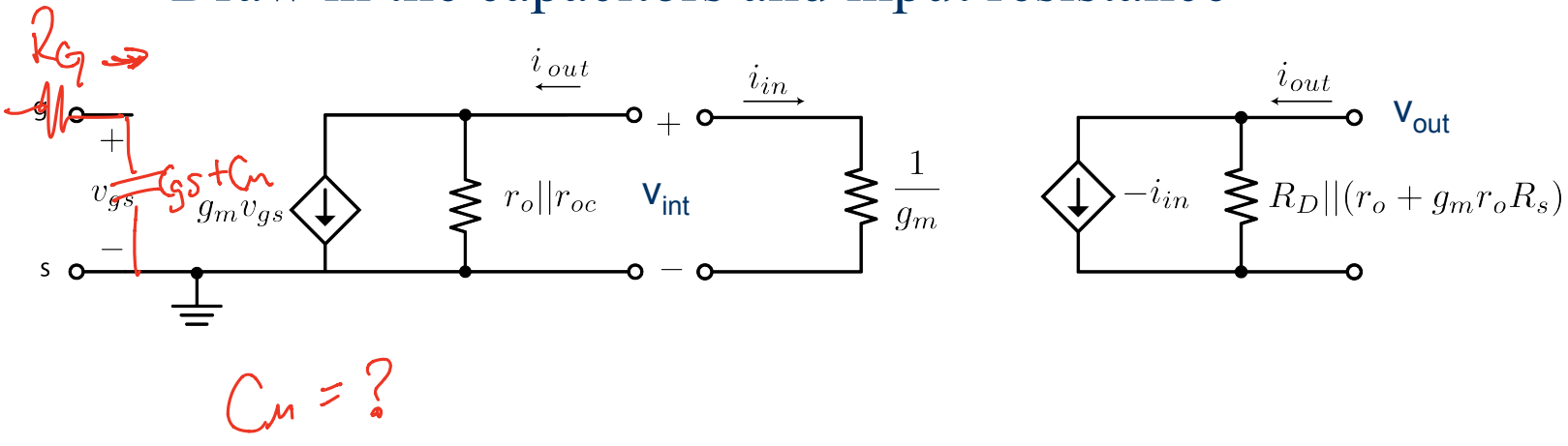
Cascode Bandwidth

- Draw in the capacitors and input resistance



$C_M = ?$

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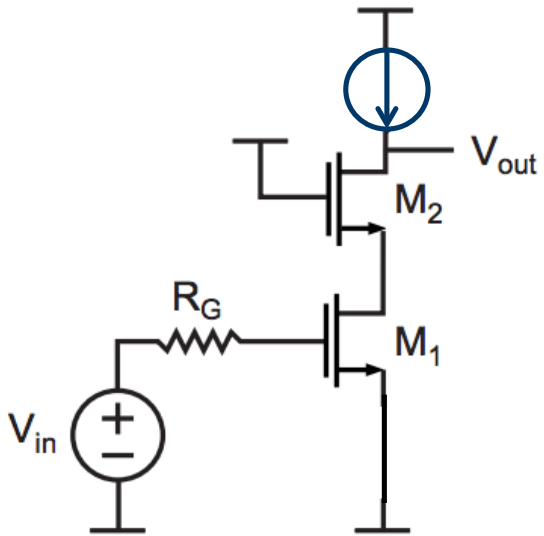
Cascode Biasing

- CG has a very large output resistance
- Loading it with R_D is likely to reduce the voltage gain
- We can increase the gain by using a current source load, but r_{oc} needs to be very large. Can use a cascode current mirror!



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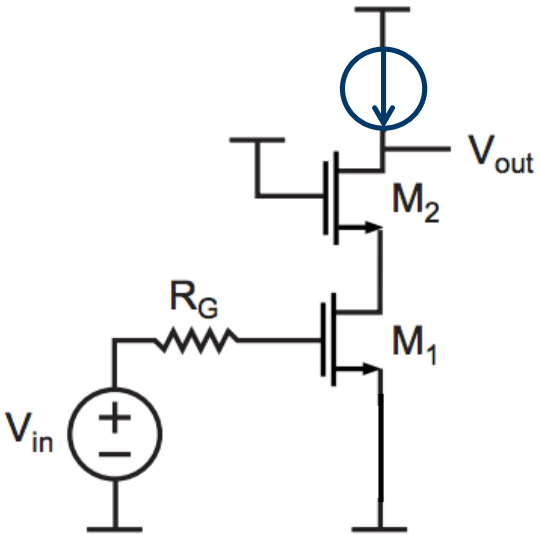
Complete Amplifier Design

Goals: $g_{m1} = 1$ mS, $R_{out} = 5$ MΩ

For simplicity, let's assume all g_m and r_o values are equal



$$A_V \approx -g_{m1}R_{out} = -1mS * 5M\Omega = -5{,}000$$

$$R_{out} \approx \frac{1}{2} g_m r_o^2 = 5M\Omega$$

$$r_o = \sqrt{\frac{20M\Omega}{g_m}} = \sqrt{\frac{10M\Omega}{1mS}} = 100k\Omega$$

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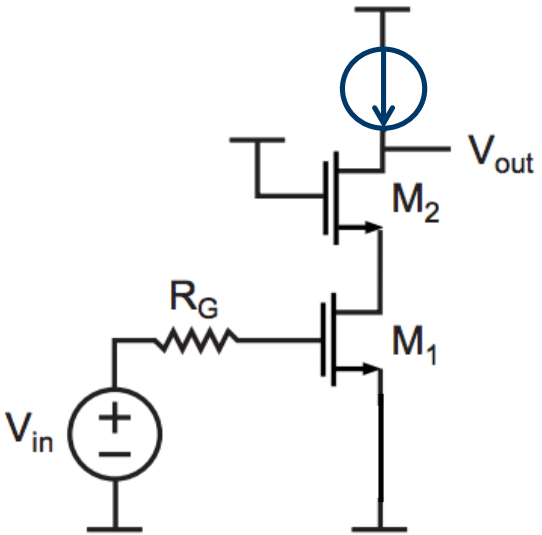
Bias Current & Device Sizing

Need to know process parameters to solve for W/L

$k' = 100\ \mu A/V^2$

$\lambda = 0.1\ [V^{-1}]$



$$r_o = \frac{1}{\lambda I_{DS}} = 100k\Omega$$

$$I_{DS} = \frac{1}{.1V^{-1} * 100k\Omega} = 100\mu A$$

$$g_m = \sqrt{2k'\left(\frac{W}{L}\right)I_{DS}} = 1mS$$

$$\frac{W}{L} = \frac{g_m^2}{2k'I_{DS}} = \frac{(1mS)^2}{2*100\mu*100\mu A} = 50$$

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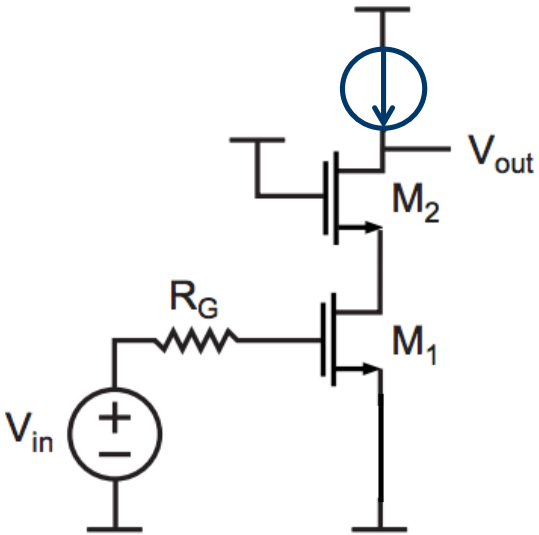
Output (Voltage) Swing

Need to know $V_{GS} - V_T$ (eg. V_{DSAT}, V_{OV})



$$g_m = \frac{2I_{DS}}{V_{GS} - V_T} = 1mS$$

$$V_{GS} - V_T = \frac{2I_{DS}}{g_m} = \frac{2 * 100\mu A}{1mS} = 0.2V$$

Maximum V_{OUT} =

Minimum V_{OUT} =

Input Bias V_{IN} =

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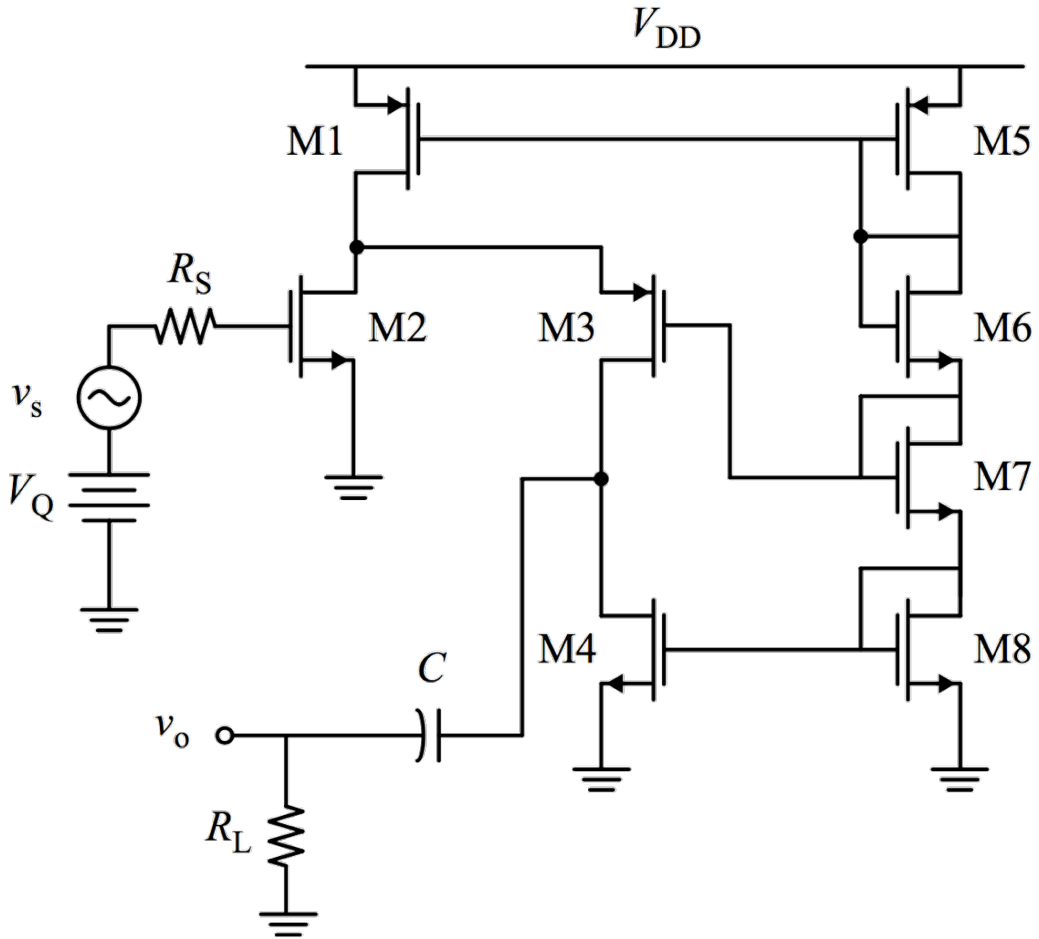
Analysis Example



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Cutting Through the Complexity

1. Identify the "signal path" between the input and output

2. Eliminate "background" transistors to reduce clutter

3. For "background transistors, understand their role (e.g. DC biasing)

4. For frequency response, identify "hi-Z" nodes.

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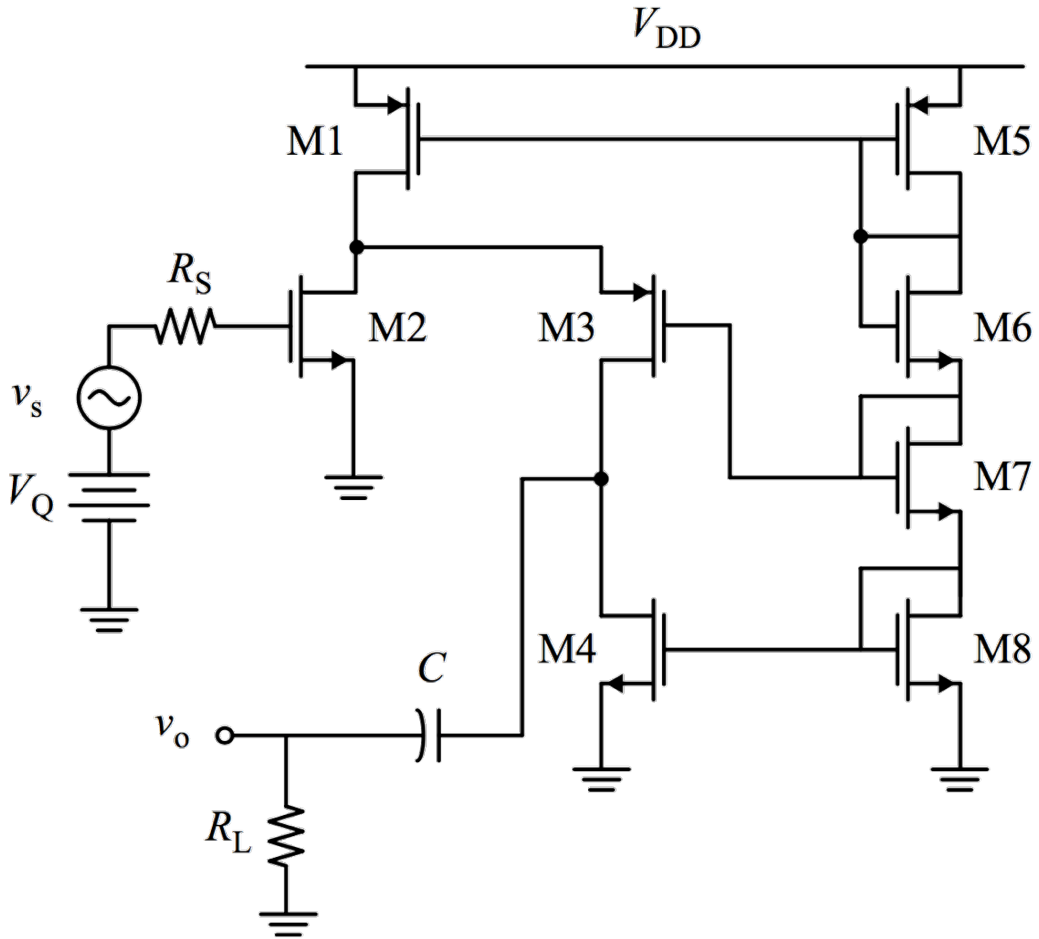
Eliminate Clutter



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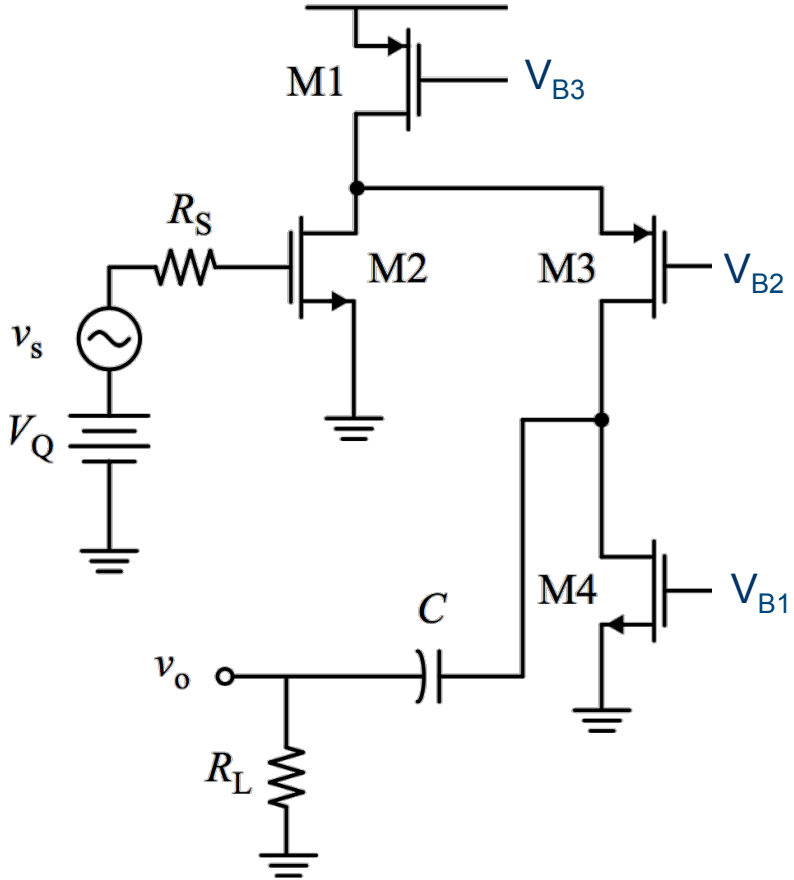
Identify Signal Path & Amplifier Stages



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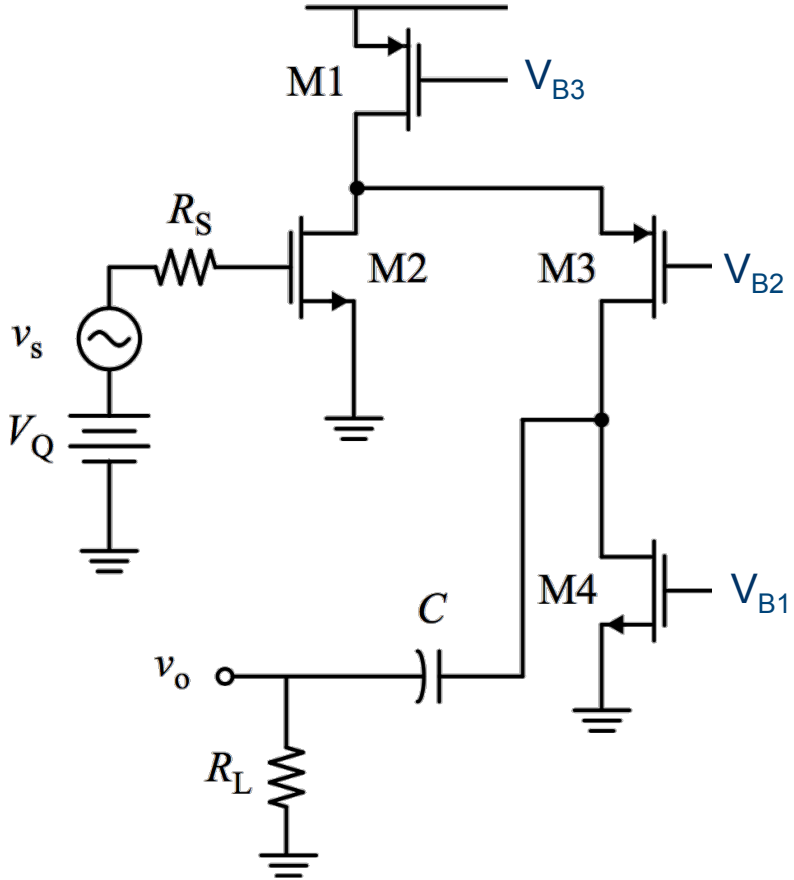
DC Biasing



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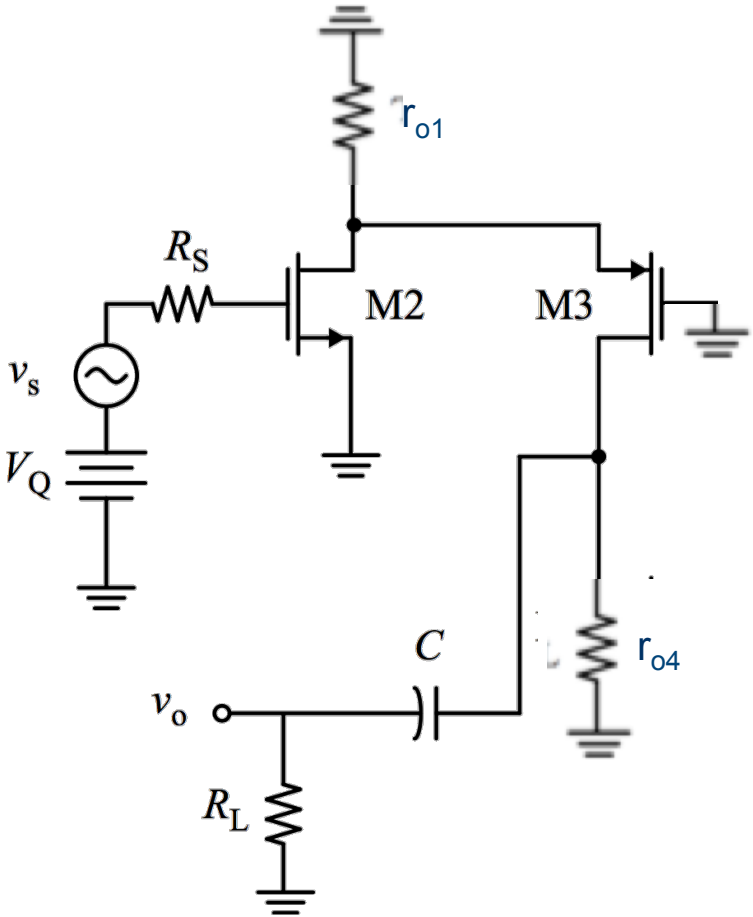
Small-Signal Models



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Two-Port Model

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External Loads

- Many applications must drive external loads that are very low impedance compared to on-chip levels
- These stages must drive high voltages/currents so linearity is a concert. We must consider "large signal" behavior
- Example: Speaker at 8 ohms versus Megaohms on-chip …
- Follower is natural choice, but it can only "source" current (think in terms of large signals)

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Design Issue: DC Coupling

Constraint: large inductors and capacitors are not available

Output of one stage is directly connected to the input of the next stage → must consider DC levels … why?