Current Mirrors and Biasing

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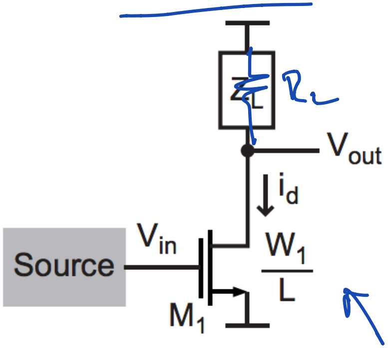
Announcements

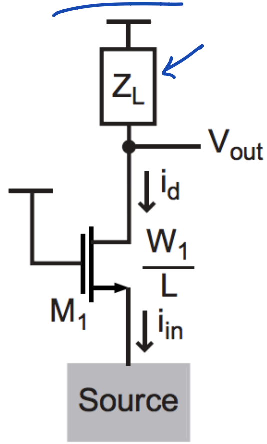
- HW9 due on Friday
- LAB 5 EXTENDED THROUGH NEXT WEEK
  - CHECK UPDATED SCHEDULE ON WEB SITE

Load Impedance

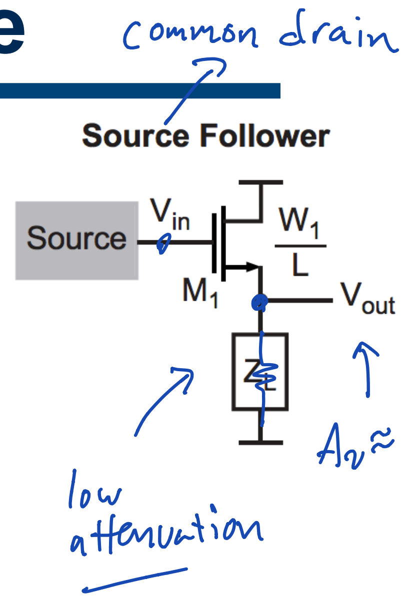
Common Source



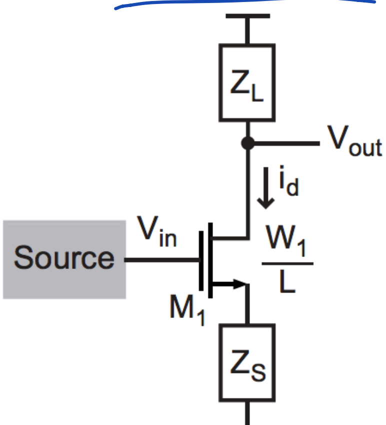
Common Gate



Source Follower



Common Source with Source Degeneration



- **To achieve high gain (or low attenuation in the case of a source follower), it is very desirable to achieve high load impedance, Z_L**
  - **Unfortunately, using a simple resistor of high value has issues**
    - What are these issues?

Courtesy M.H. Perrott

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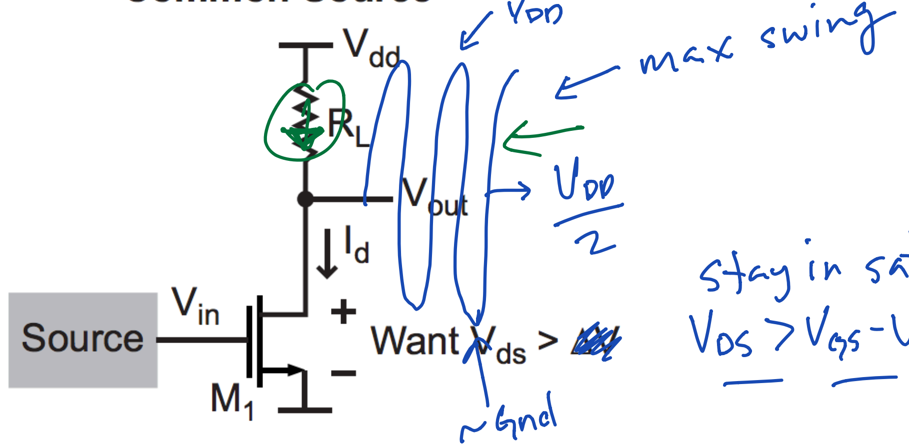
Issue: Headroom Limitations

Common Source



stay in saturation
$V_{DS} > V_{GS} - V_T$

- **The bias current of the device is a direct function of R_L**

largest R_L possible $V_{OUT} = V_{GS} - V_T$

$$I_d = \frac{V_{dd} - V_{ds}}{R_L}$$

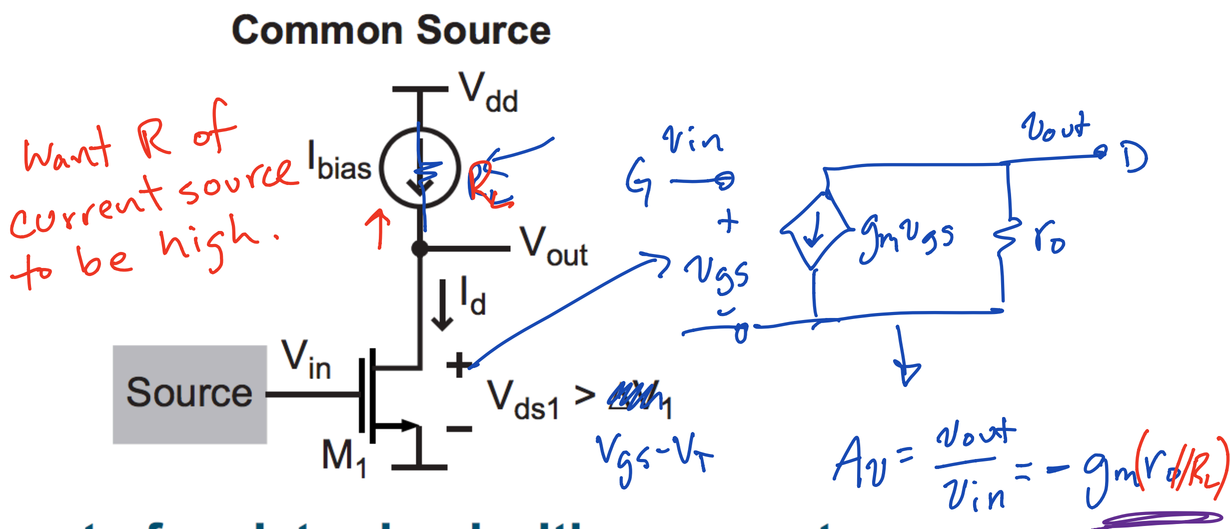
$$I_{DS} = \frac{V_{DD} - V_{DD}/2}{R_L}$$

  - **V_{dd} is < 3.6V for most modern CMOS processes**
  - **V_{ds} must be greater than ΔV to maintain device saturation**

Large R_L implies small I_d
(implies small g_m, poor frequency response, etc.)

Courtesy M.H. Perrott

Achieving High Gain



- Replacement of resistor load with a current source yields the highest possible DC gain out of the amplifier
  - Current source determines I_d of device
- We can make current sources out of transistors
  - Generally smaller area than polysilicon resistors

What is the small signal gain of the above circuit?

Courtesy M.H. Perrott

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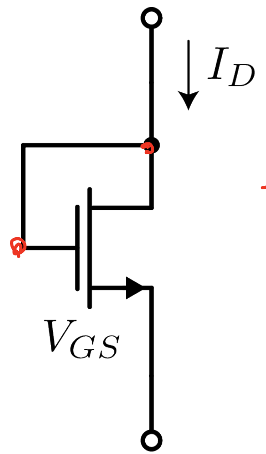
Diode Connected Device



$$V_{GS} = V_{DS}$$

(1) 2-terminal device

(2) $V_{DS} = 0$ $I_{DS} = 0$
cut-off

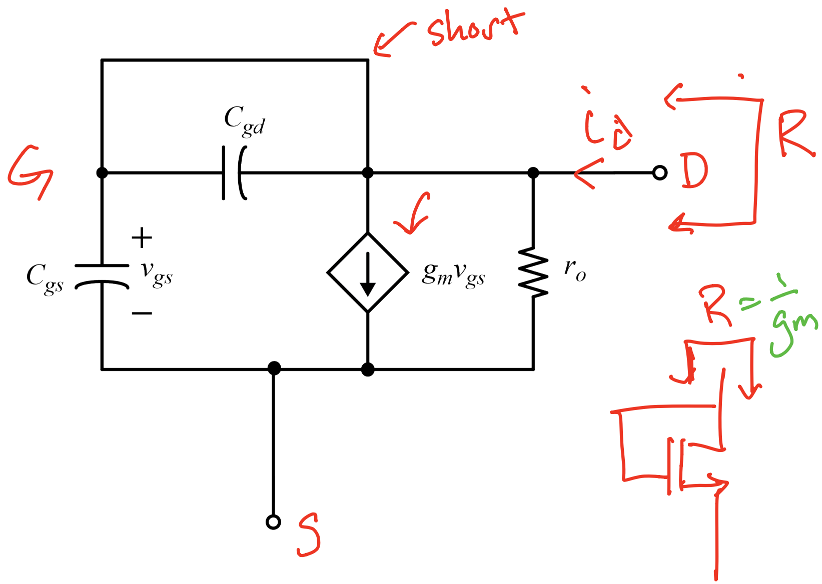
$V_{DS} \to$ large $I_{DS} \to$ large

(3) always in saturation when $V_{GS} > V_T$
$V_{DS} > V_{GS} - V_T$ if $V_{DS} = V_{GS}$
always true

- How do we build current sources?
- Let's start with a "diode connected" device
- A MOS device with gate and drain shorted operates like a diode (but not exponential)

BJT is actully exponential

Diode Connected -- SS Model



$$i_d = g_m v_{gs} + \frac{v_{ds}}{r_o}$$

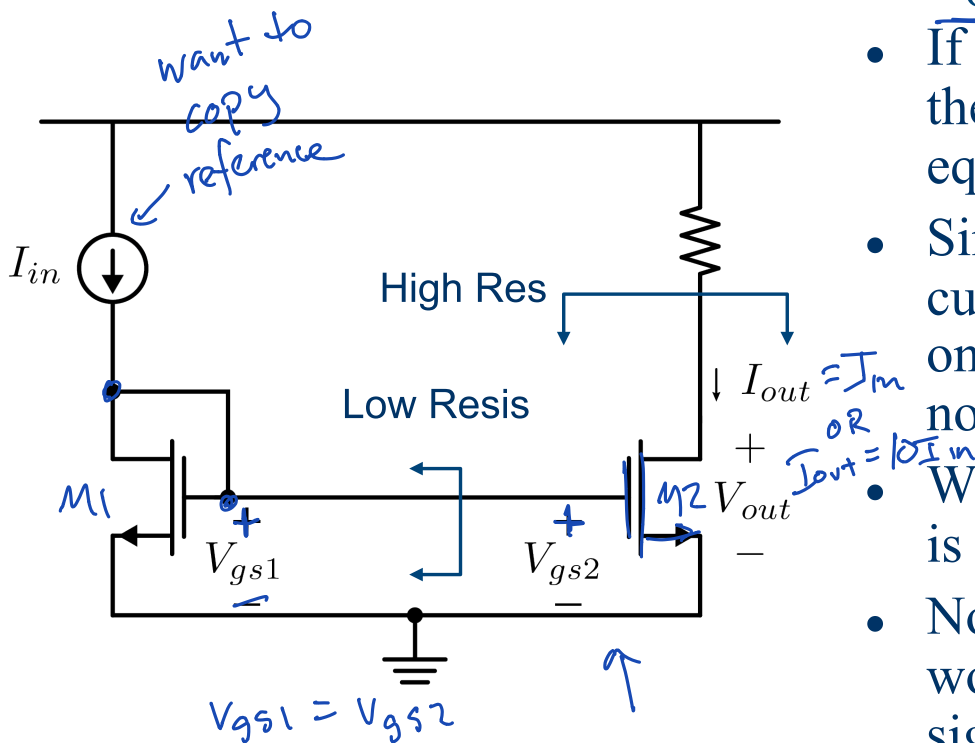
$$i_{ds} = g_m v_{ds} + \frac{v_{ds}}{r_o}$$

$$\frac{i_{ds}}{v_{ds}} = g_m + \frac{1}{r_o}$$

$$\frac{v_{ds}}{i_{ds}} = \left[g_m + \frac{1}{r_o}\right]^{-1} = \left[\frac{g_m r_o + 1}{r_o}\right]^{-1} = \frac{r_o}{g_m r_o + 1} \approx \frac{1}{g_m}$$

- We can derive the small-signal model by shorting out the hybrid-pi model
- Note that a Gm generator with it's controlling terminals connected to the Gm is more simply a …?

The Integrated "Current Mirror"



- M_1 and M_2 have the same V_{GS}
- If we neglect CLM (λ=0), then the drain currents are equal
- Since λ is small, the currents will nearly mirror one another even if V_{out} is not equal to V_{GS1}
- We say that the current I_{REF} is mirrored into i_{OUT}
- Notice that the mirror works for small and large signals!

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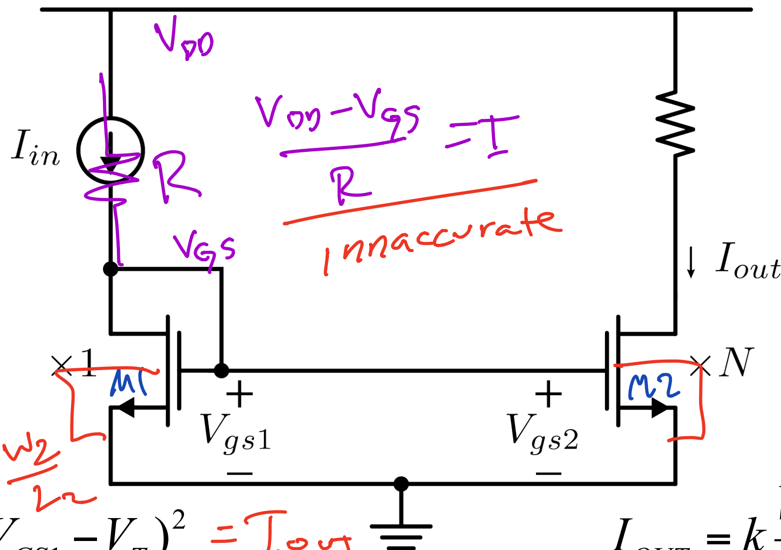
Multiplication Ratio



if we want $I_{OUT} = 2 I_{in}$, $W_2/L_2 = 2 W_1/L_1$

in practice $L_1 = L_2$, just scale width

M2 in saturation

$\frac{V_{DD} - V_{GS}}{R} = I$ — innacurate

$k = \frac{1}{2}\mu C_{ox}$

$$I_{IN} = k\frac{W_1}{L_1}(V_{GS1} - V_T)^2$$

$$I_{OUT} = k\frac{W_2}{L_2}(V_{GS2} - V_T)^2$$

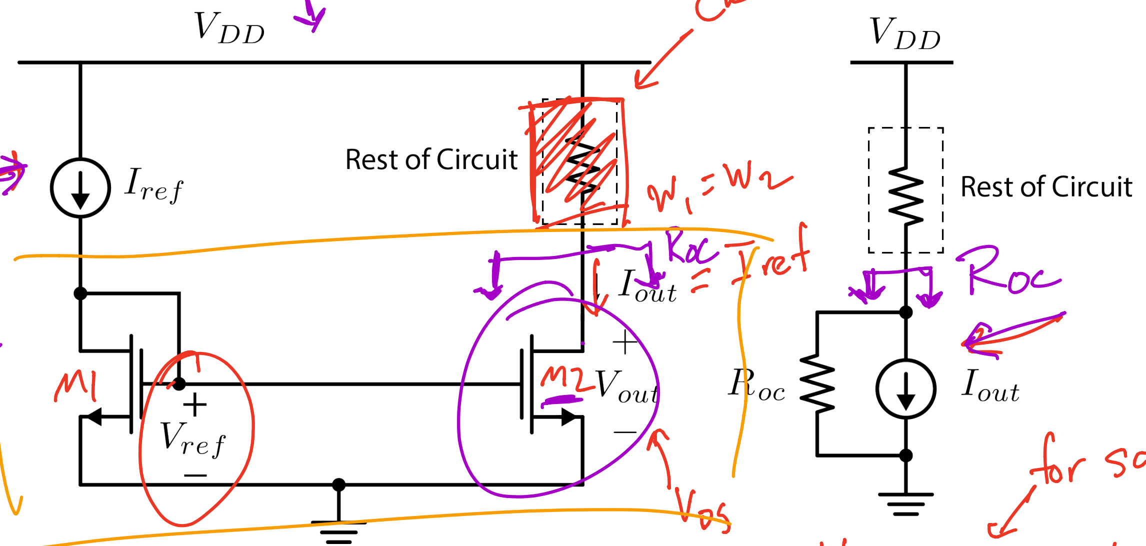
$$V_{GS1} = V_{GS2}$$

also know ks are equal

$$I_{OUT} = k\frac{W_2}{L_2}(V_{GS2} - V_T)^2 = I_{IN}\frac{W_2 / L_2}{W_1 / L_1} = NI_{IN}$$

ratio gives N

Current Mirror as Current Source



- The output current of M_2 is only weakly dependent on v_{OUT} due to high output resistance of FET
- M2 acts like a current source to the rest of the circuit
- For good current source behavior, what is the minimum v_{OUT}?

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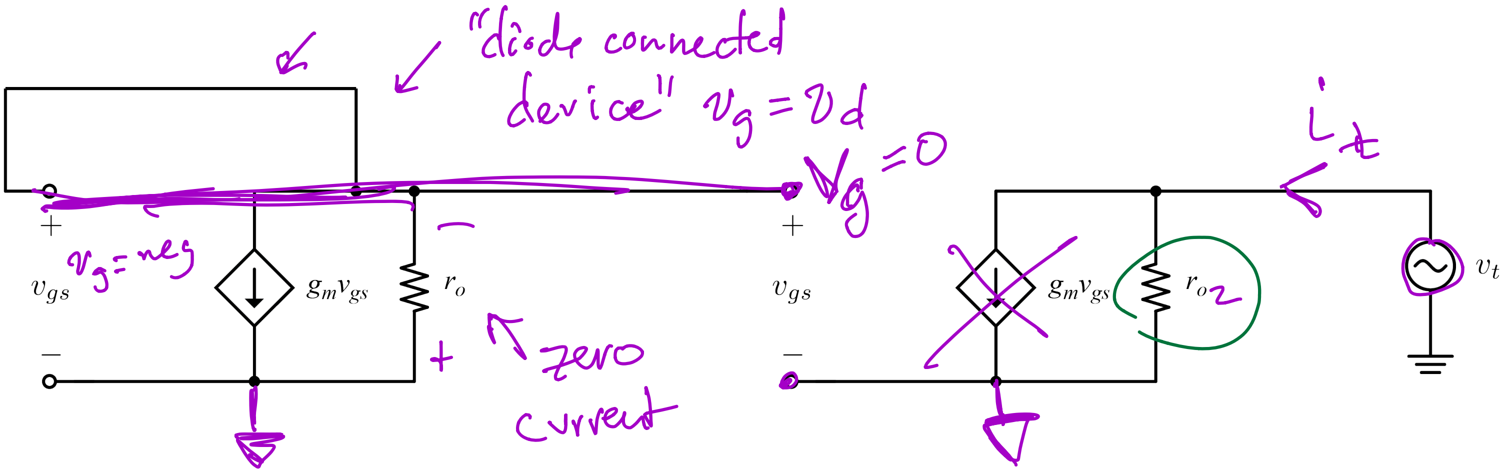
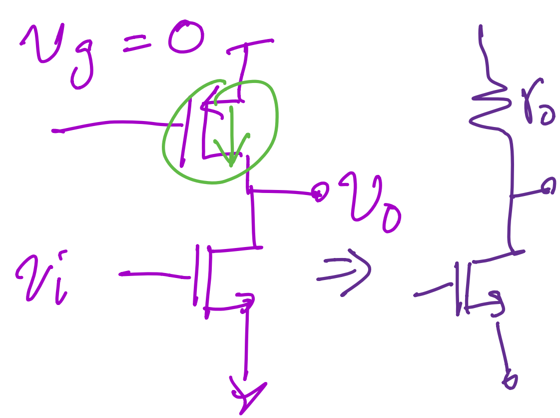
Small-Signal Resistance of *I*-Source



what happens to v_g?
no current in left branch

$$R_{oc} = \frac{v_t}{i_t} = r_{o2}$$



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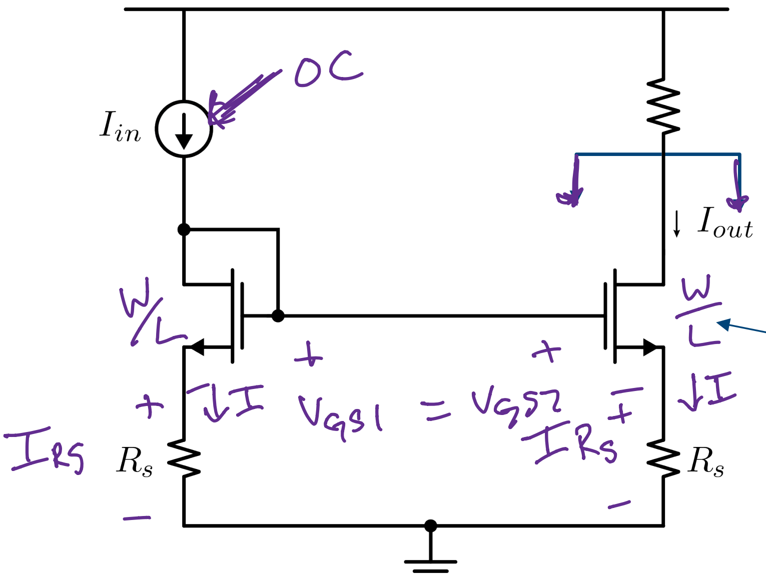
Improved Current Sources

Goal: increase $R_{o(ut)}$ = Roc

Approach: look at *amplifier* output resistance results … to see topologies that boost resistance

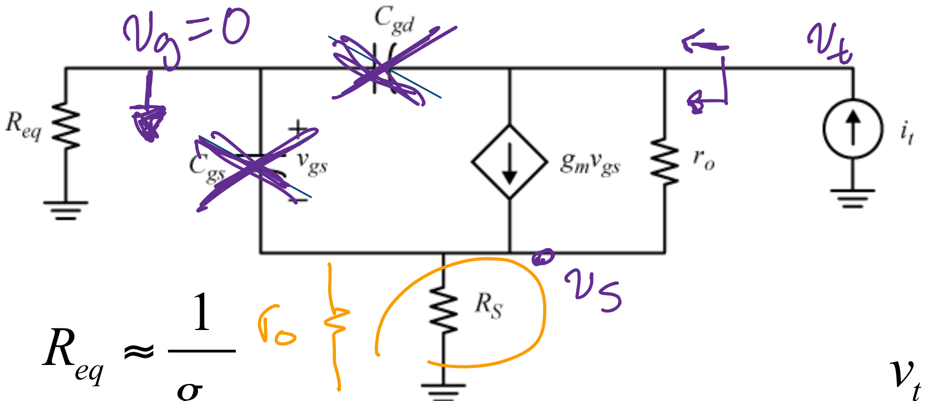


$R_{out} >> r_o$

Iout = IIN

Looks like the output impedance of a common-source amplifier with source degeneration

Effect of Source Degeneration



$$R_{eq} \approx \frac{1}{g_m}$$

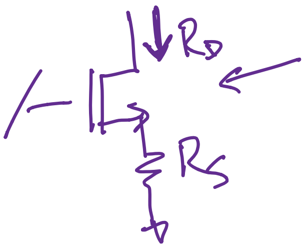
$$v_t = (i_t - g_m v_{gs}) r_o + v_{R_S}$$

$$v_{gs} \approx -v_{R_S}$$

$$v_{R_S} = i_t R_S$$

$$v_t = (i_t + g_m R_S i_t) r_o + i_t R_S$$

$$R_o = \frac{v_t}{i_t} \approx (1 + g_m R_S) r_o$$

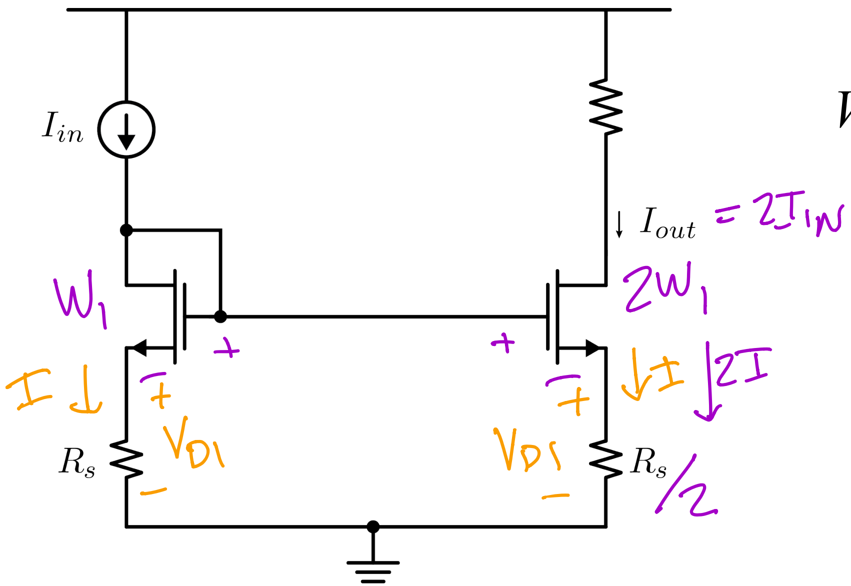


use result in saturation

- Equivalent resistance loading gate is dominated by the diode resistance … assume this is a small impedance
- Output impedance is boosted by factor $(1 + g_m R_S)$

Improved Current Sources

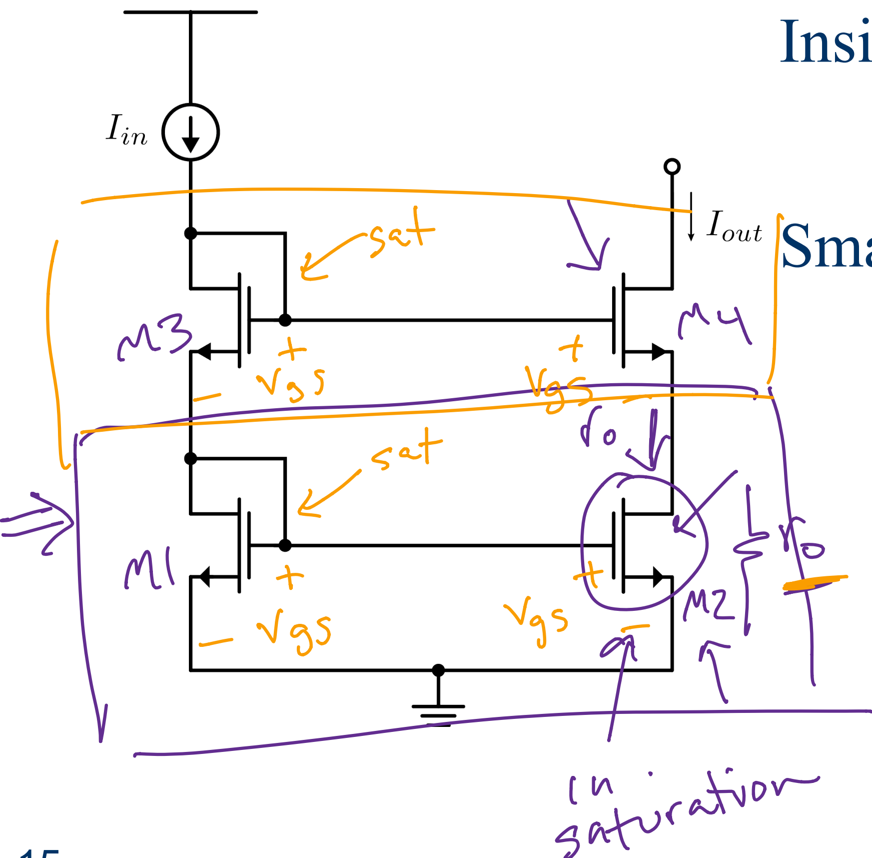
How would you scale the output current?



$$I_{IN} = k\frac{W_1}{L_1}(V_G - V_S - V_T)^2$$

$$V_S = I_{IN} R_S$$

Cascode (or Stacked) Current Source



Insight: V_{GS2} = constant AND V_{DS2} = constant

Small-Signal Resistance R_o:

$R_s = r_o$

$$R_o \approx (1 + g_m R_S) r_o$$

$$R_o \approx (1 + g_m r_o) r_o$$

$$R_o \approx g_m r_0^2 >> r_o$$

really high

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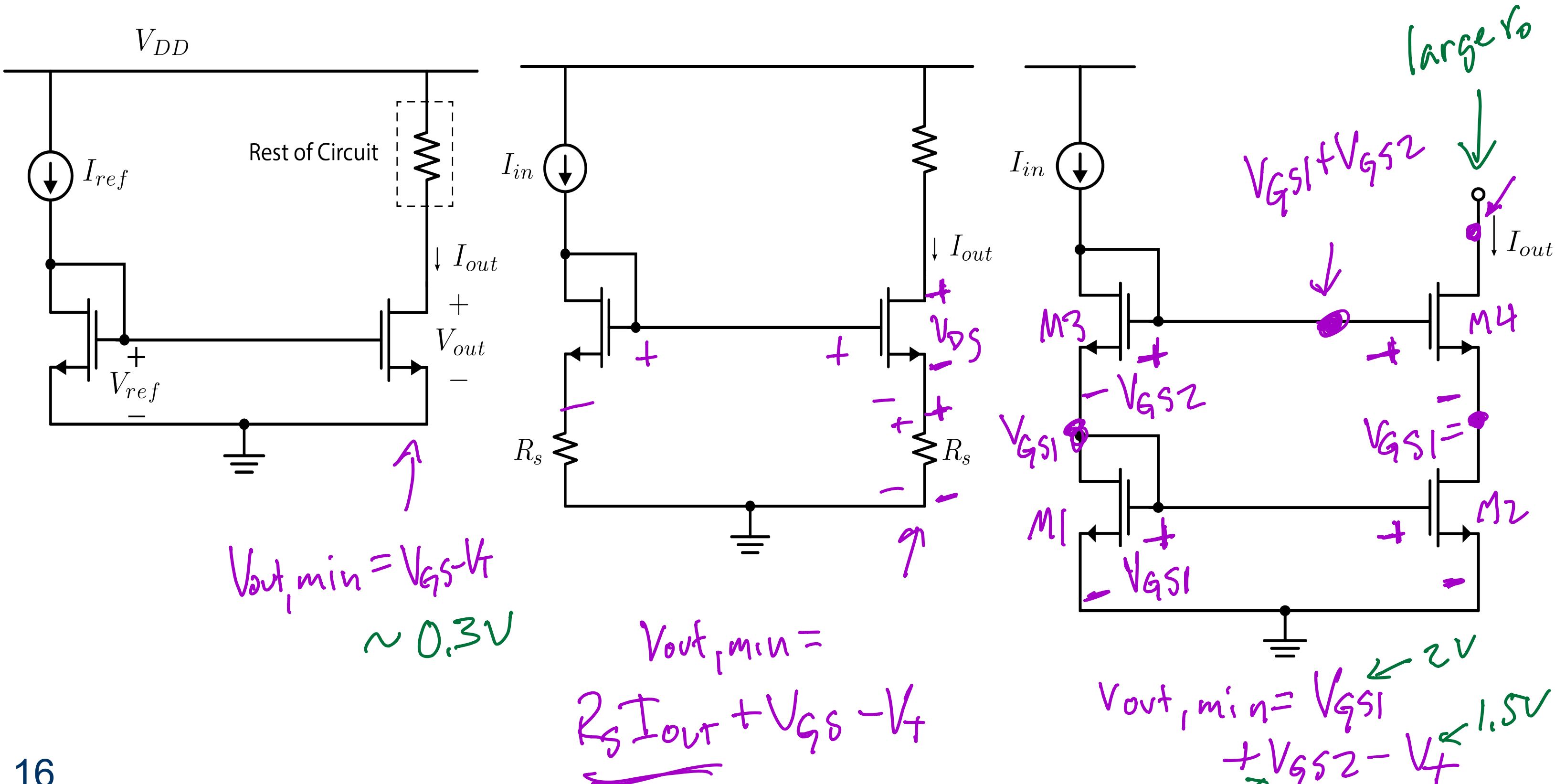
Drawback of Cascode *I*-Source

What is the minimum output voltage to keep all transistors in saturation?



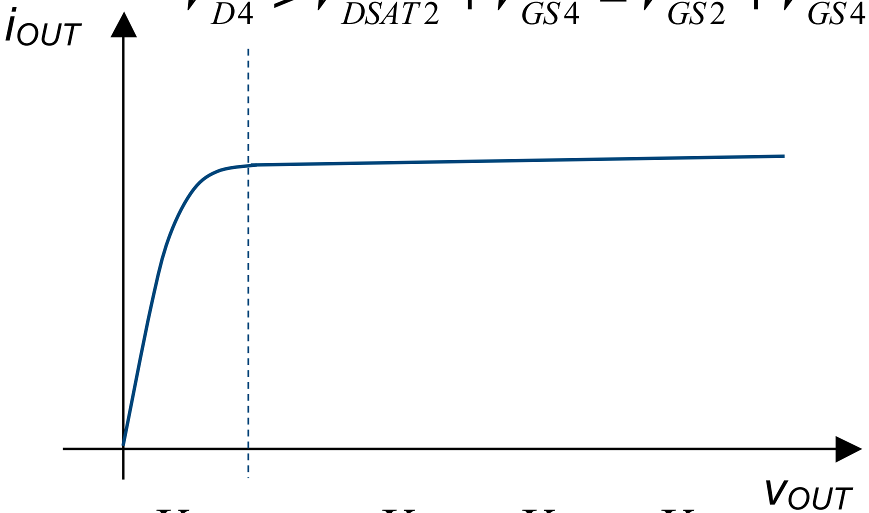
Drawback of Cascode *I*-Source

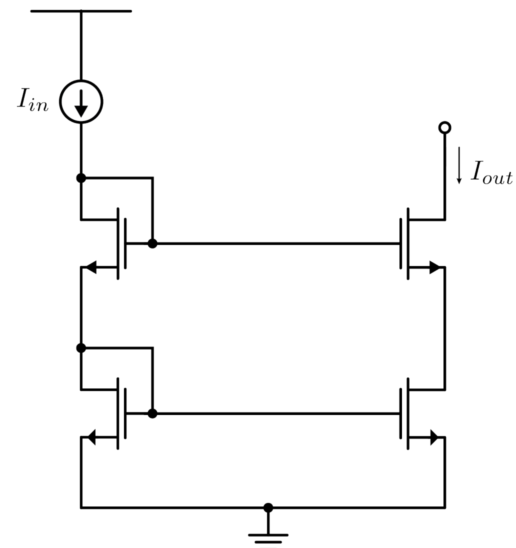
Minimum output voltage to keep both transistors in saturation:

$$V_{OUT,MIN} = V_{DS4,MIN} + V_{DS2,MIN}$$

$$V_{DS2,MIN} > V_{GS2} - V_{T0} = V_{DSAT2}$$

$$V_{D4} > V_{DSAT2} + V_{GS4} = V_{GS2} + V_{GS4} - V_{T0}$$





$$V_{OUT,MIN} = V_{GS2} + V_{GS4} - V_{T0}$$

In EE140 we will learn circuit tricks to overcome this problem!

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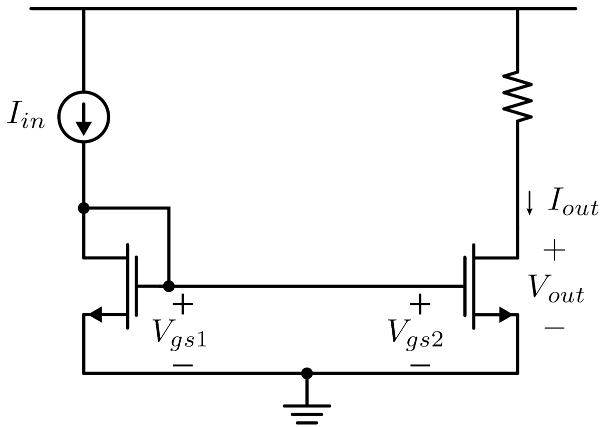
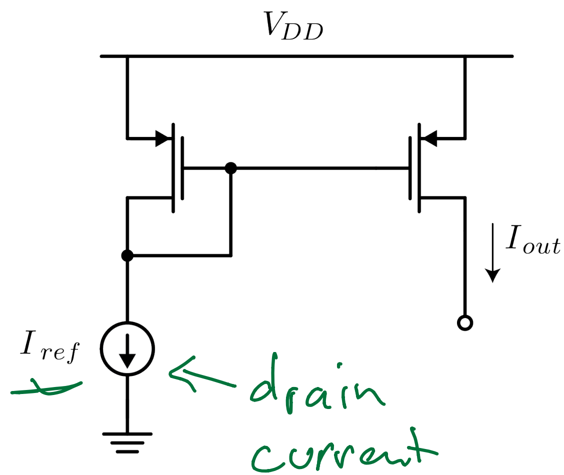
Current Sinks and Sources

Sink: output current goes to ground

Source: output current comes from voltage supply





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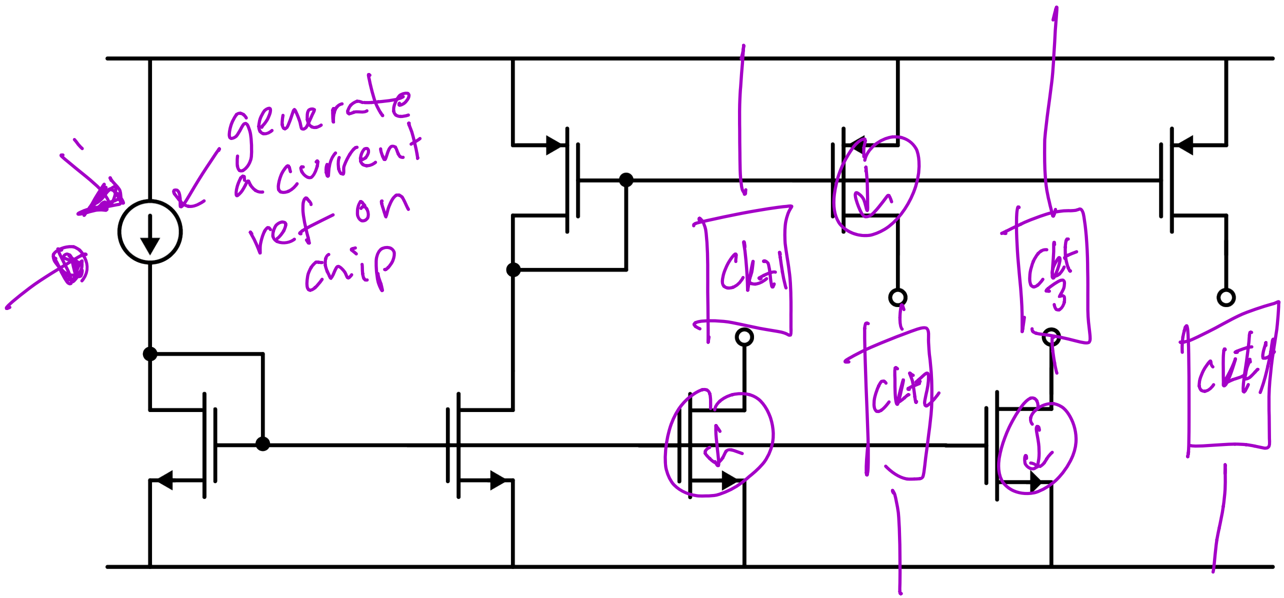
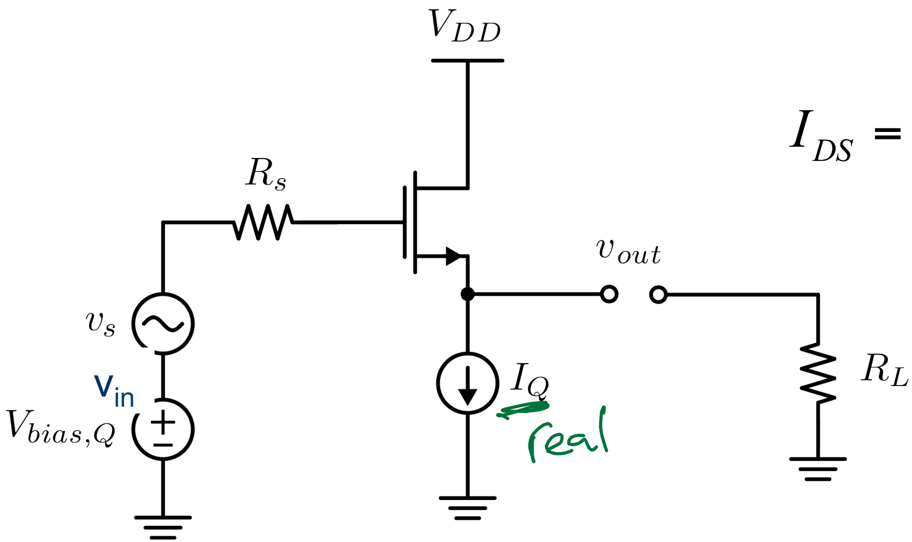
Current Mirrors

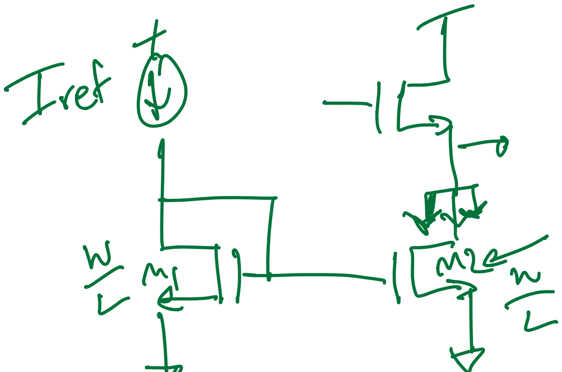
Idea: we only need one reference current to set up all the current sources and sinks needed for a multistage amplifier.



Example: Common-Drain Amplifier



$$I_{DS} = \mu C_{ox} \frac{W}{L} \frac{1}{2} (V_{GS} - V_T)^2$$



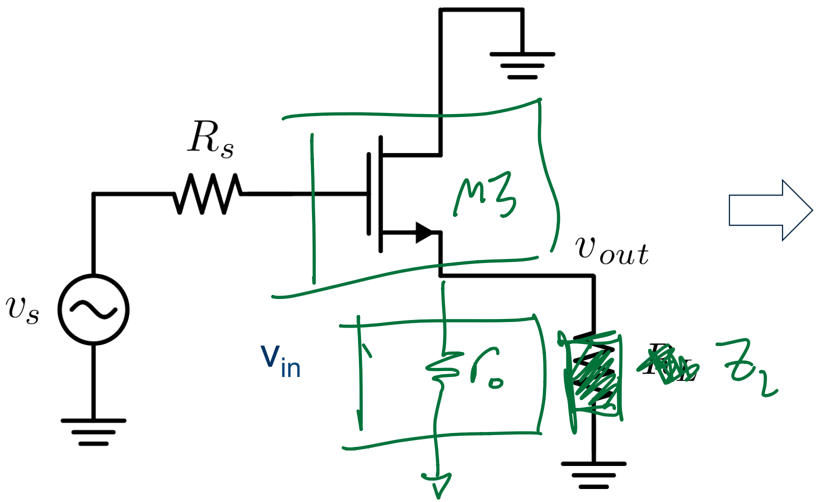
$I_D = I_{ref}$

$R_D = ?$ in small signal

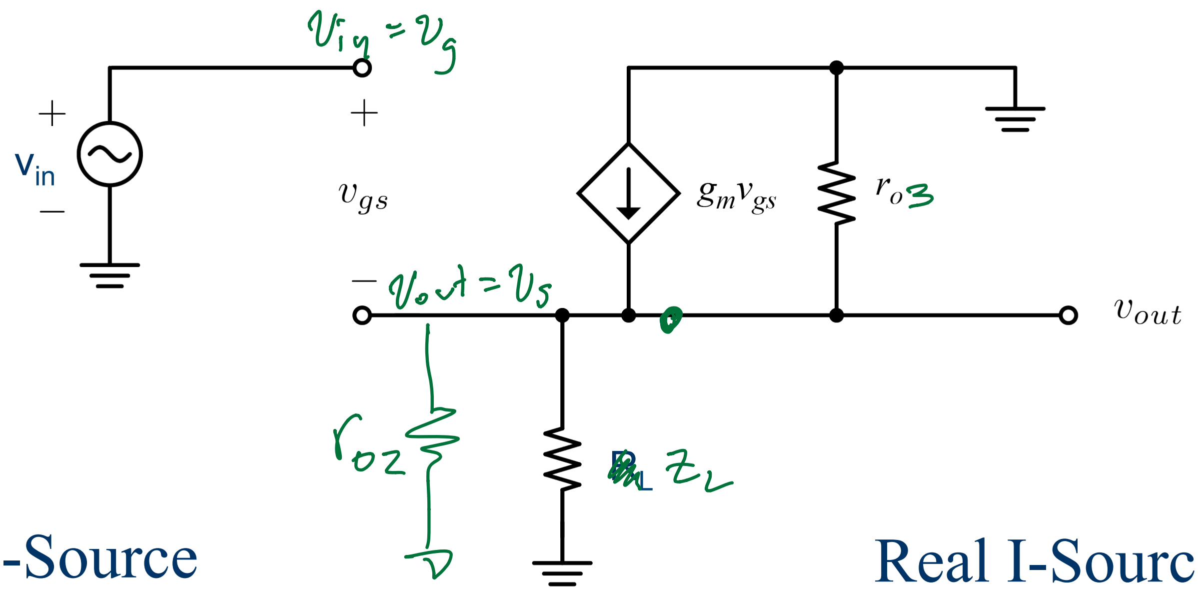
r_{o2}

Common Drain AC Schematic

How does a REAL current source fit in to the small-signal model?



CD Voltage Gain With Real I-Source



Ideal I-Source

$$\frac{v_{out}}{R_L \| r_o} = g_m v_{gs}$$

$$\frac{v_{out}}{R_L \| r_o} = g_m \left(v_{in} - v_{out} \right)$$

Real I-Source

$$\frac{v_{out}}{Z_L \| r_{o2} \| r_{o3}} = g_m v_{gs}$$

$$= g_m \left(v_{in} - v_{out} \right)$$

CD Voltage Gain (Cont.)

KCL at source node:

$$\frac{v_{out}}{Z_L \| r_{o2} \| r_{o3}} + g_m v_{out} = g_m v_{in}$$

Voltage gain:

$$\frac{v_{out}}{v_{in}} = \frac{g_m}{g_m + \frac{1}{Z_L \| r_{o2} \| r_{o3}}}$$

$Z_L = \infty$

$r_{o2} = r_{o3}$

$$\frac{g_m}{g_m + \frac{1}{r_o/2}} = \frac{g_m}{g_m + 2/r_o}$$

$$= \boxed{\frac{g_m r_o}{g_m r_o + 2}} \leftarrow$$

ideally want $A_V = 1$

$g_m r_o \sim 10$

$\frac{10}{12} \sim \frac{5}{6}$ 8X%