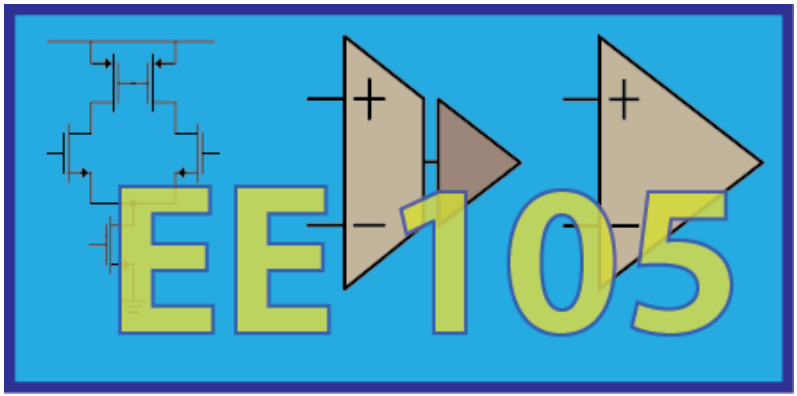

Complete MOS Small-Signal Model

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Announcements

- Welcome back!
- Pick up graded MT2 in lecture on Tuesday
- Check updated syllabus
- No lab this week
- HW8 due on Friday

↳ AVE = 78
$\sigma \sim 15$

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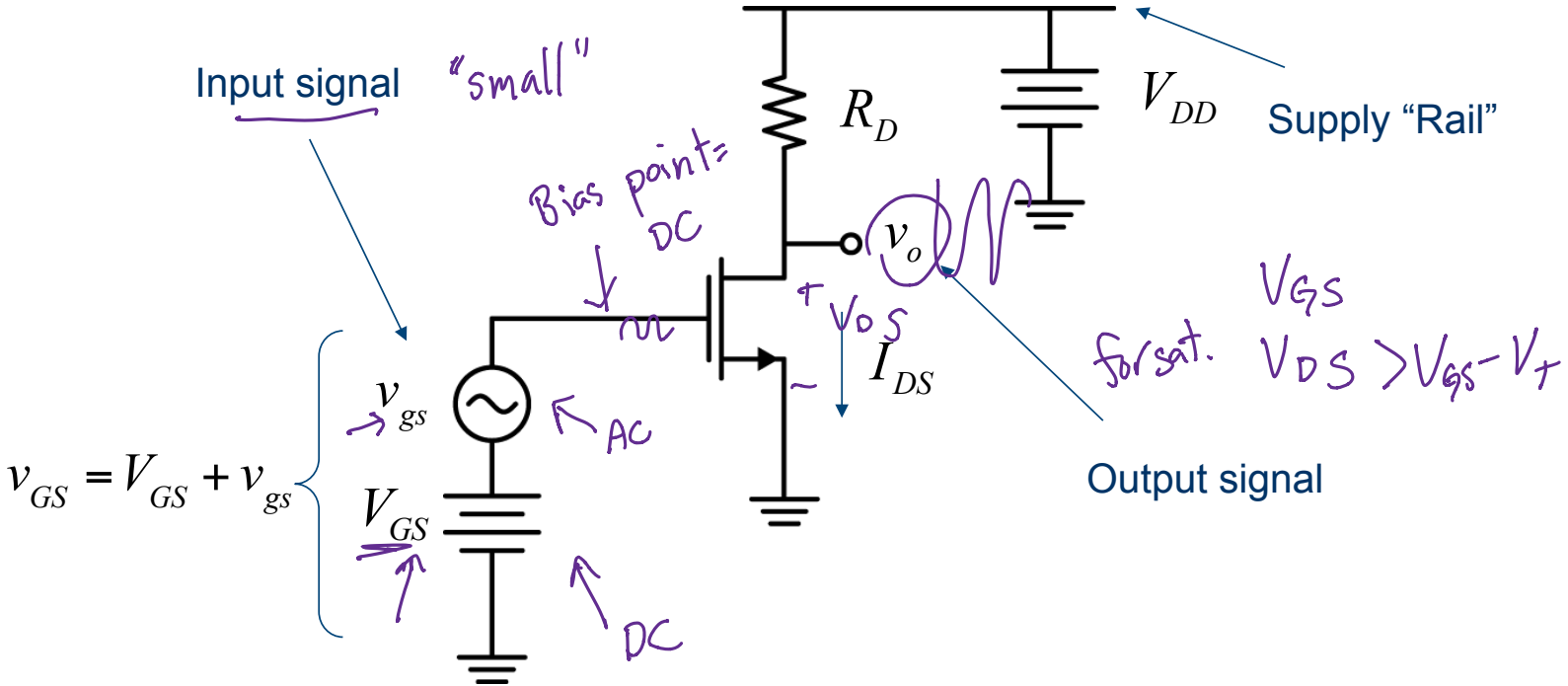
Review: An MOS Amplifier



This type of amplifier is known as "Common Source (CS)"

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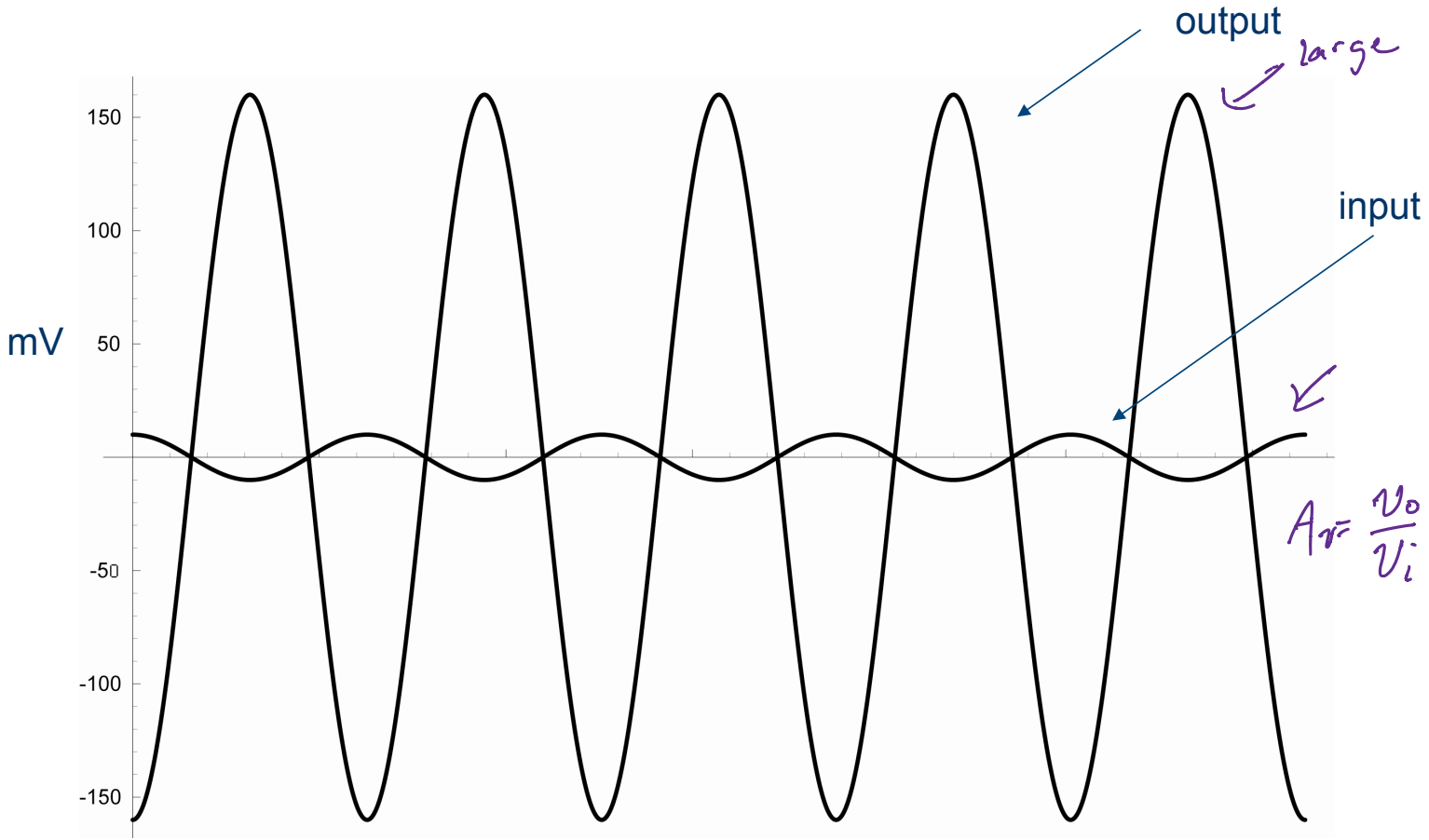
Plot of Output Waveform (Gain!)



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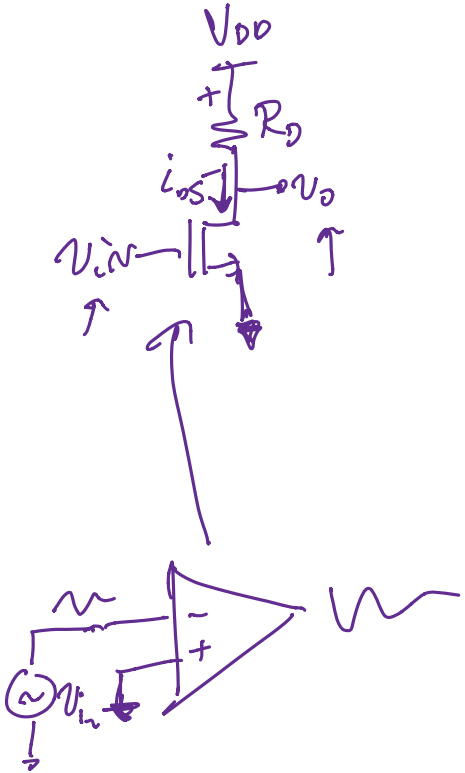
Total Small Signal Current



$$i_{DS}(t) = I_{DS} + i_{ds}$$

DC AC

BIAS POINT

$V_o = V_{DD} - I_{DS} \cdot R_D$

$$i_{ds} = \frac{\partial i_{DS}}{\partial v_{gs}} v_{gs} + \frac{\partial i_{DS}}{\partial v_{ds}} v_{ds}$$

$$i_{ds} = g_m v_{gs} + \frac{1}{r_o} v_{ds}$$

large

large

small

*Trans*conductance

Conductance

want

i_{ds} changes a lot w/ v_{gs}

don't want

i_{ds} change w/ v_{ds}

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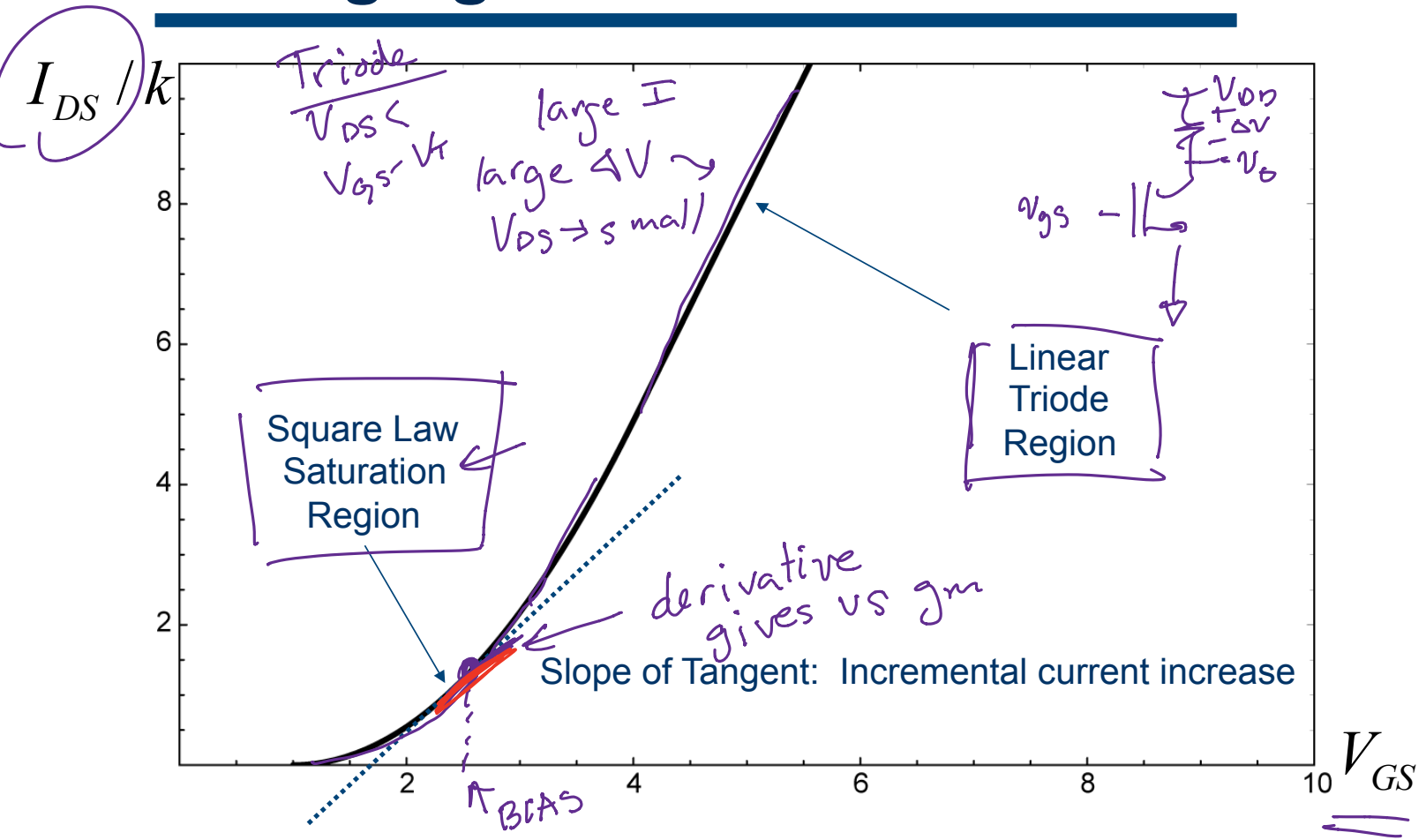
Changing One Variable at a Time



Assumption: $V_{DS} > V_{DS,SAT} = V_{GS} - V_{Tn}$ (square law)

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The *Transconductance* g_m

Defined as the change in drain current due to a change in the *gate-source* voltage, with *everything else constant*

$$I_{DS,sat} = \frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

$\lambda \rightarrow$ small

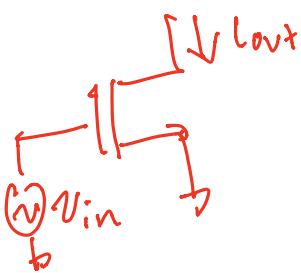
$$g_m = \left.\frac{\Delta i_D}{\Delta v_{GS}}\right|_{V_{GS},V_{DS}} = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{V_{GS},V_{DS}} = \mu C_{ox}\frac{W}{L}(V_{GS}-V_T)(1+\lambda V_{DS})$$

≈ 0

bias point

$$g_m = \mu C_{ox}\frac{W}{L}(V_{GS}-V_T)$$ ← Gate Bias

input V to output I



$$g_m = \mu C_{ox}\frac{W}{L}\sqrt{\frac{2I_{DS}}{\frac{W}{L}\mu C_{ox}}} = \sqrt{2\mu C_{ox}\frac{W}{L}I_{DS}}$$ ← Drain Current Bias

$$g_m = \frac{2I_{DS}}{(V_{GS}-V_T)}$$ ← Drain Current Bias and Gate Bias

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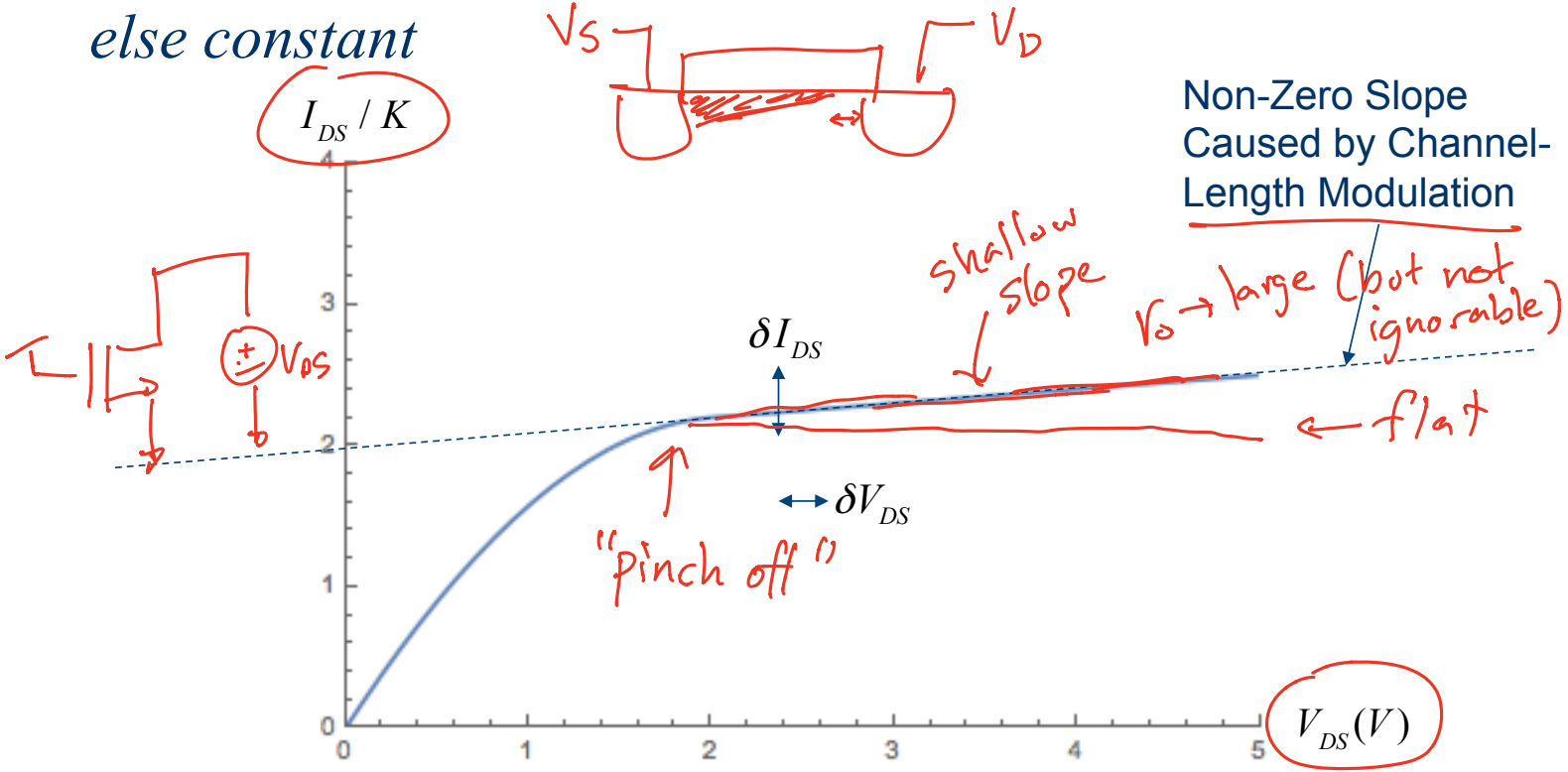
Output Resistance r_o

Defined as the inverse of the change in drain current due to a change in the *drain-source* voltage, with *everything else constant*



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Evaluating r_o

$$i_D = \frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

$$r_o = \left(\left.\frac{\partial i_D}{\partial v_{DS}}\right|_{V_{GS},V_{DS}}\right)^{-1}$$

$$r_0 = \frac{1}{\frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS}-V_T)^2\lambda}$$

$$r_0 \approx \frac{1}{\lambda I_{DS}}$$

output V (V_{DS})

output I

$\Omega = \left[\frac{\partial i_o}{\partial v_{ds}} \Rightarrow \frac{1}{\Omega}\right]^{-1}$

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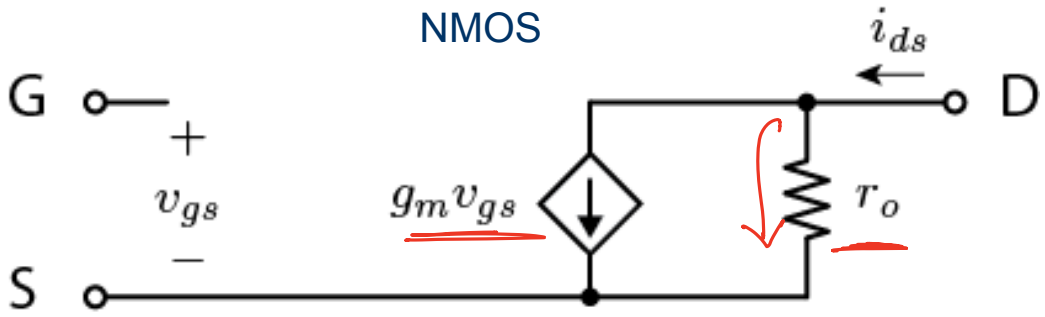
Simple Small Signal Model for MOSFET



- This is a simplified, 3-terminal small-signal model for a MOSFET
- In later lectures we will develop a more complete model
- g_m = transconductance
  - defined as di_{ds}/dv_{gs}, units $[Ohms]^{-1}$
- r_o = output resistance
  - defined as $[di_{ds}/dv_{ds}]^{-1}$, units Ohms

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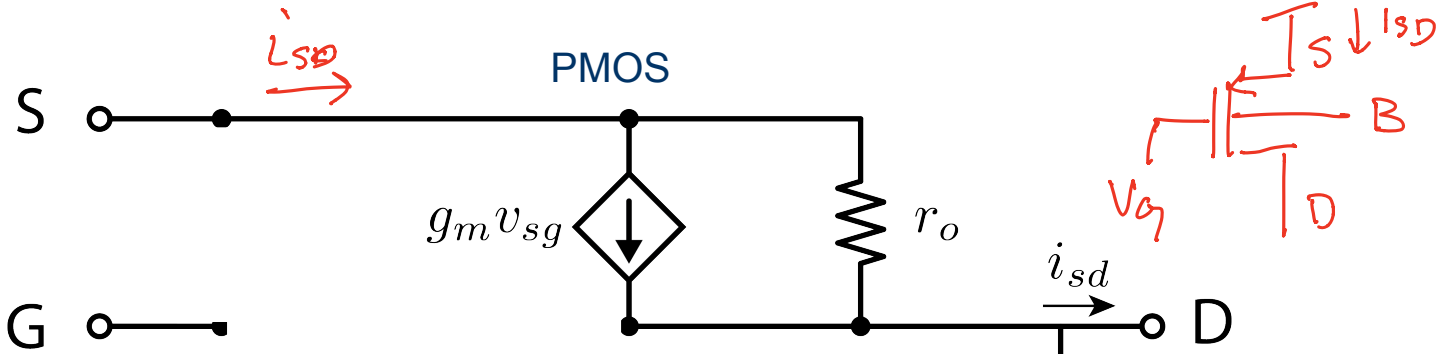
Small-Signal PMOS Model



- This is a simplified, 3-terminal small-signal model for a MOSFET
- In later lectures we will develop a more complete model
- g_m = transconductance
  - defined as di_{sd}/dv_{sg}, units $[Ohms]^{-1}$
- r_o = output resistance
  - defined as $[di_{sd}/dv_{sd}]^{-1}$, units Ohms

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What we've ignored…until now!

- The fourth terminal of the MOSFET is the body of the transistor… it can act like a second gate, or "back gate"
- The junctions of the transistor form pn-junction diodes with body, this introduces parasitic capacitance

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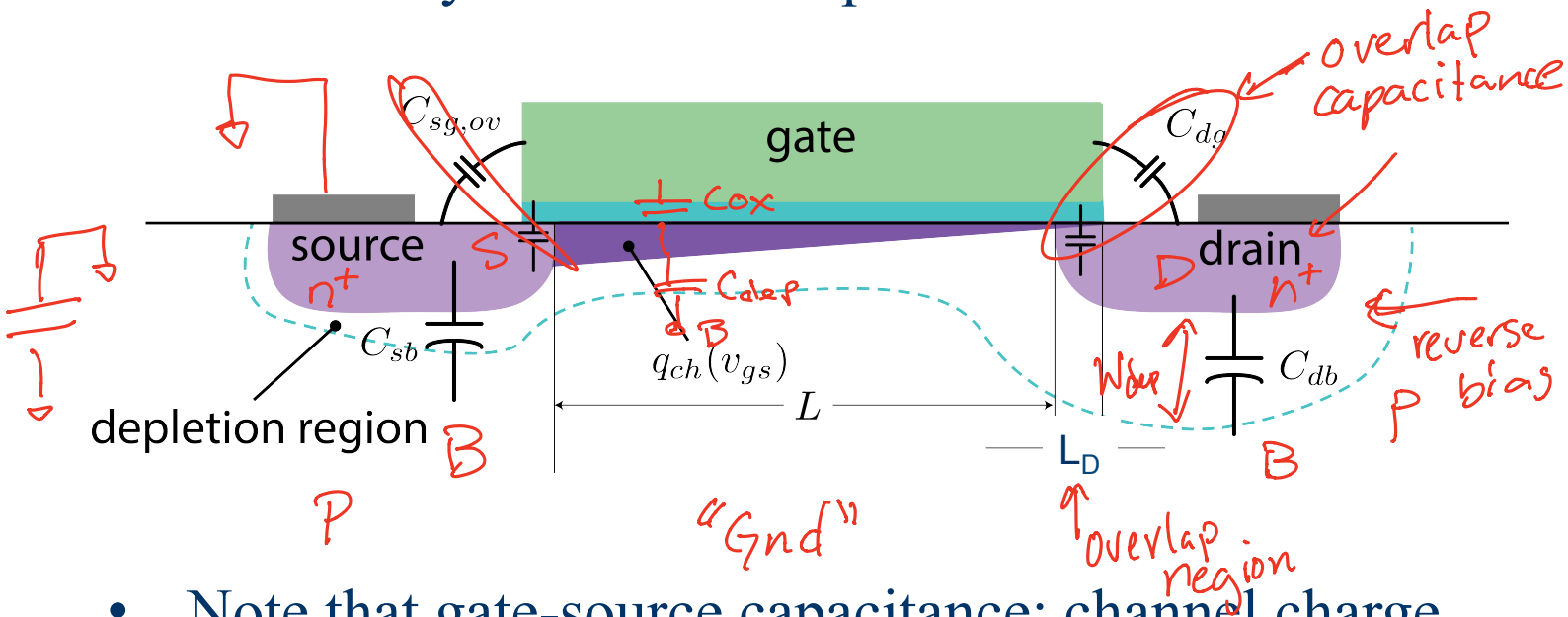
MOSFET Capacitances in Saturation

MOSFETS have many parasitic capacitances
Let us analyze where each parasitic comes from



- Note that gate-source capacitance: channel charge is mostly controlled by gate-source and not drain in saturation

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Gate-Source Capacitance C_{gs}

Wedge-shaped charge in saturation → effective area is $(2/3)WL$

larger

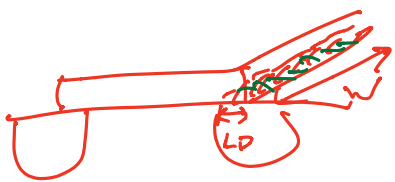
parallel plate

$$C_{gs} = (2/3)WLC_{ox} + C_{ov}$$

Overlap capacitance along source edge of gate →

$$C_{ov} = L_D W C_{ox}$$

(Underestimate due to fringing fields)



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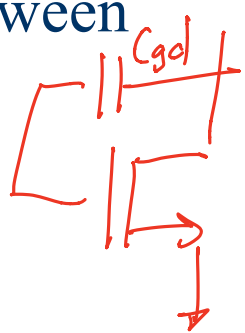
Gate-Drain Capacitance C_{gd}

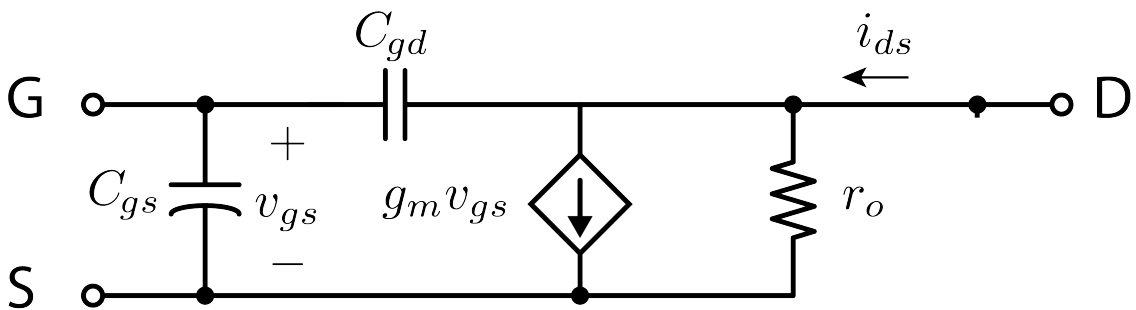
IN SATURATION

Not due to change in inversion charge in channel.

Overlap (and fringing) capacitance C_{ov} between drain and source is C_{gd}



$$C_{gd} = C_{ov} = L_D W C_{ox}$$



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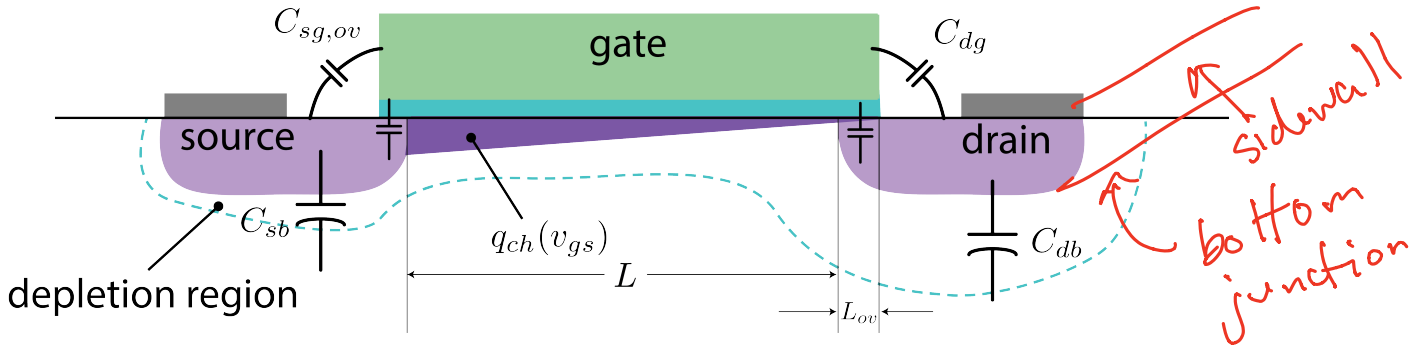
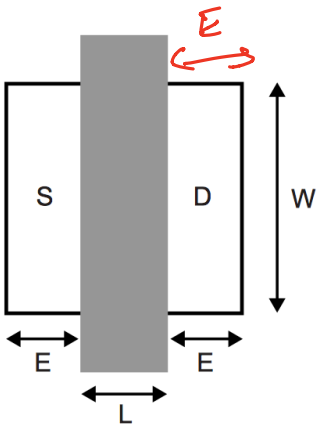
Drain-Bulk Capacitance C_{db}



- Drain-Bulk and Source-Bulk capacitance is caused by p-n junction depletion



junction bottom wall cap (per area)

junction sidewall cap (per length)

source to bulk cap: $C_{jsb} = \frac{C_j(0)}{\sqrt{1 + V_{SB}/|\Phi_B|}} WE + \frac{C_{jsw}(0)}{\sqrt{1 + V_{SB}/|\Phi_B|}} (W + 2E)$

drain to bulk cap: $C_{jsd} = \frac{C_j(0)}{\sqrt{1 + V_{DB}/|\Phi_B|}} WE + \frac{C_{jsw}(0)}{\sqrt{1 + V_{DB}/|\Phi_B|}} (W + 2E)$

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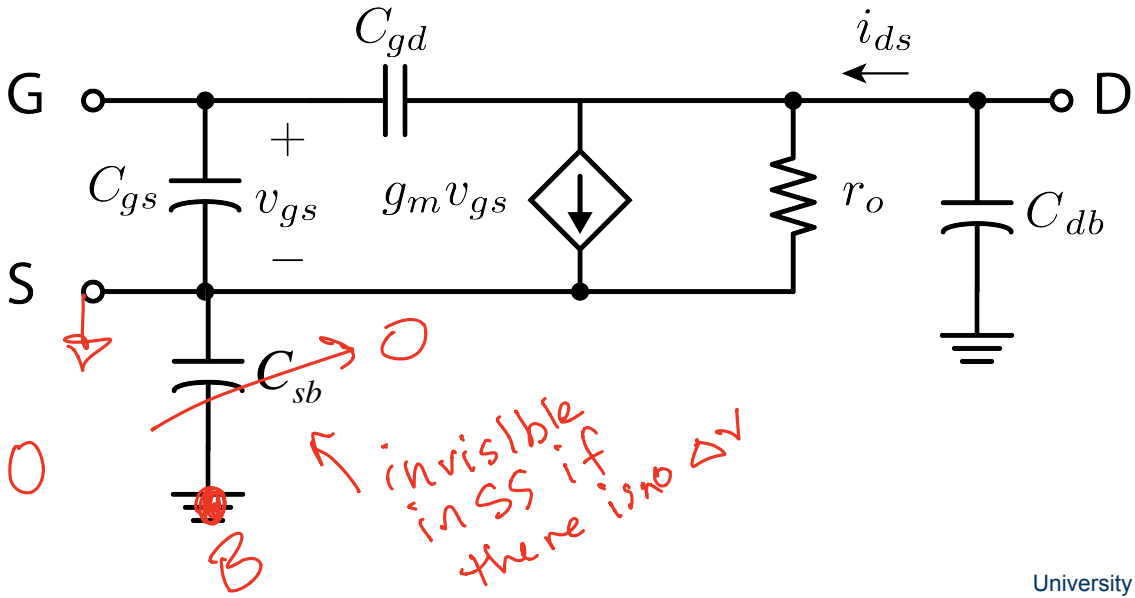
Summary of Capacitance Models

$$C_{gs} = (2/3)WLC_{ox} + C_{ov}$$

$$C_{gd} = C_{ov}$$

$$C_{sb} = C_{jsb}(area + perimeter)\,junction$$

$$C_{db} = C_{jdb}(area + perimeter)\,junction$$



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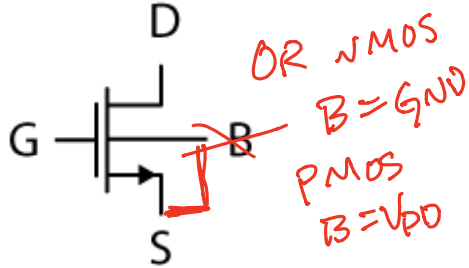
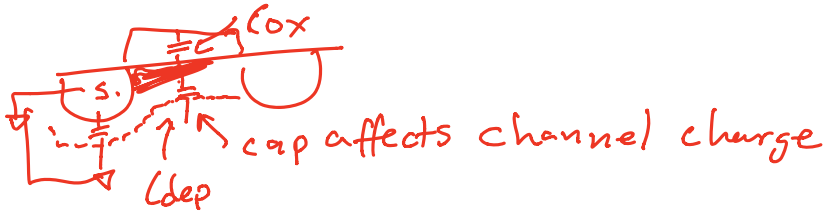
Back-Gate Effect

- Transistor really has *four* terminals:
  - Source / Drain
  - Gate / Body



- There is a symmetry between the gate and the body. The body can act like a "back gate"
- In many instances the body terminal is simply tied to the source (ground or VSS for NMOS, supply or VDD for PMOS)
- What happens if there is a DC or AC voltage swing on the body?



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Body Bias Affects V_T

- If there is a body bias V_{SB}, a depletion capacitance appears in parallel with C_{ox} and affects the amount of channel charge:

$$C_{dep} = \varepsilon_s / x_{dep,\max} \quad [F/cm^2]$$

$$Q_{inv} = -C_{ox}(V_{GS} - V_T) + C_{dep} V_{SB}$$

channel charge

$$Q_{inv} = -C_{ox}\left[V_{GS} - V_T - \frac{C_{dep}}{C_{ox}} V_{SB}\right]$$

injects additional charge

$$V_T(V_{SB}) = V_{T0} + \frac{C_{dep}}{C_{ox}} V_{SB}$$

$V_{t,eff}$

where it comes from

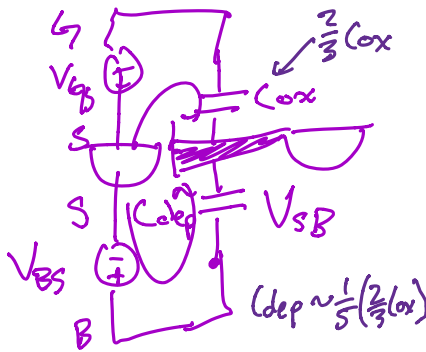
- C_{dep} changes with body bias, if we account for this:

$$V_{T0n} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}}\sqrt{2q\varepsilon_s N_a(-2\phi_p)}$$

model

$$\Delta V_T = \frac{1}{C_{ox}}\sqrt{2q\varepsilon_s N_a}\left(\sqrt{-2\phi_p + V_{SB}} - \sqrt{-2\phi_p}\right)$$

$$V_T = V_{T0} + \gamma\left(\sqrt{V_{SB} - 2\phi_p} - \sqrt{-2\phi_p}\right)$$



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Role of the Substrate Potential

Note: Need not be the source potential, but $V_B < V_S$

don't turn on the diode!

Effect: changes threshold voltage, which changes the drain current … substrate acts like a "backgate"

$$g_{mb} = \left.\frac{\Delta i_D}{\Delta v_{BS}}\right|_Q = \left.\frac{\partial i_D}{\partial v_{BS}}\right|_Q$$

$$Q = (V_{GS}, V_{DS}, V_{BS})$$

$V_{bs} \rightarrow$ affects i_{ds}

$$g_{mb} = \left.\frac{\partial i_D}{\partial v_{BS}}\right|_Q = \left.\frac{\partial i_D}{\partial V_{Tn}}\right|_Q \left.\frac{\partial V_{Tn}}{\partial v_{BS}}\right|_Q$$

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Backgate Transconductance

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

$$V_T = V_{T0} + \gamma\left(\sqrt{V_{SB}-2\phi_p} - \sqrt{-2\phi_p}\right)$$

Result: $$g_{mb} = \left.\frac{\partial i_D}{\partial v_{BS}}\right|_Q = \left.\frac{\partial i_D}{\partial V_{Tn}}\right|_Q \left.\frac{\partial V_{Tn}}{\partial v_{BS}}\right|_Q = \frac{\gamma g_m}{2\sqrt{-V_{BS}-2\phi_p}}$$

$$\frac{\partial V_T}{\partial V_{BS}} = \frac{\partial}{\partial V_{BS}}\left[\gamma\left[(-V_{BS}-2\phi_p)^{1/2} - (-2\phi_p)^{1/2}\right]\right]$$

$$= -\frac{1}{2}\gamma\left(-V_{BS}-2\phi_p\right)^{-1/2}$$

$$\frac{\partial i_D}{\partial V_T} = \frac{\partial}{\partial V_T}\left[\frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_T)^2\right]$$

$$= -\mu C_{ox}\frac{W}{L}(V_{GS}-V_T) = -g_m$$

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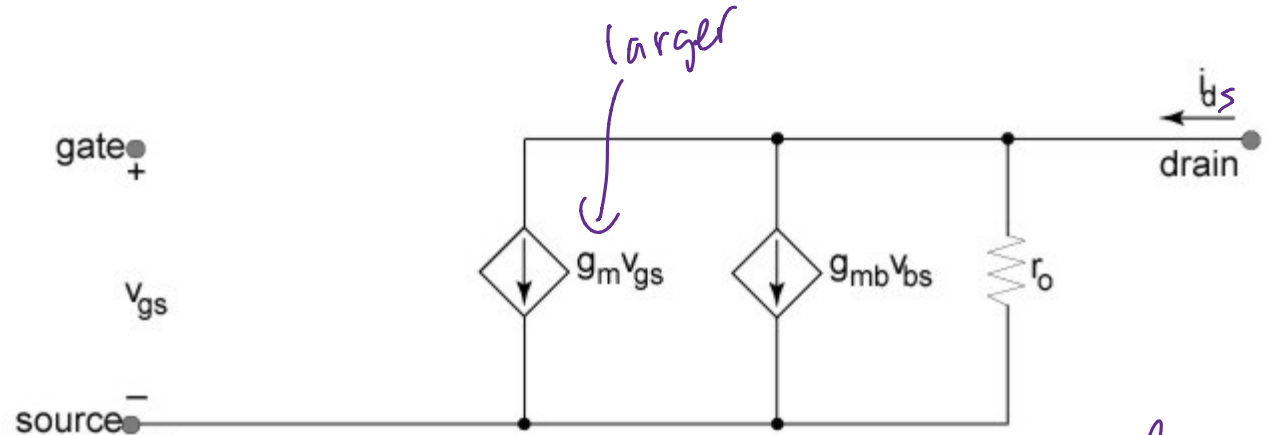
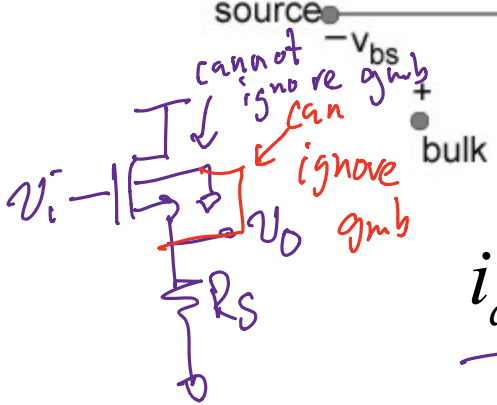
Four-Terminal Small-Signal Model





if in small signal $v_{bs}=0$ $g_{mb}v_{bs}=0$

$$i_{ds} = g_m v_{gs} + g_{mb} v_{bs} + \frac{1}{r_o} v_{ds}$$

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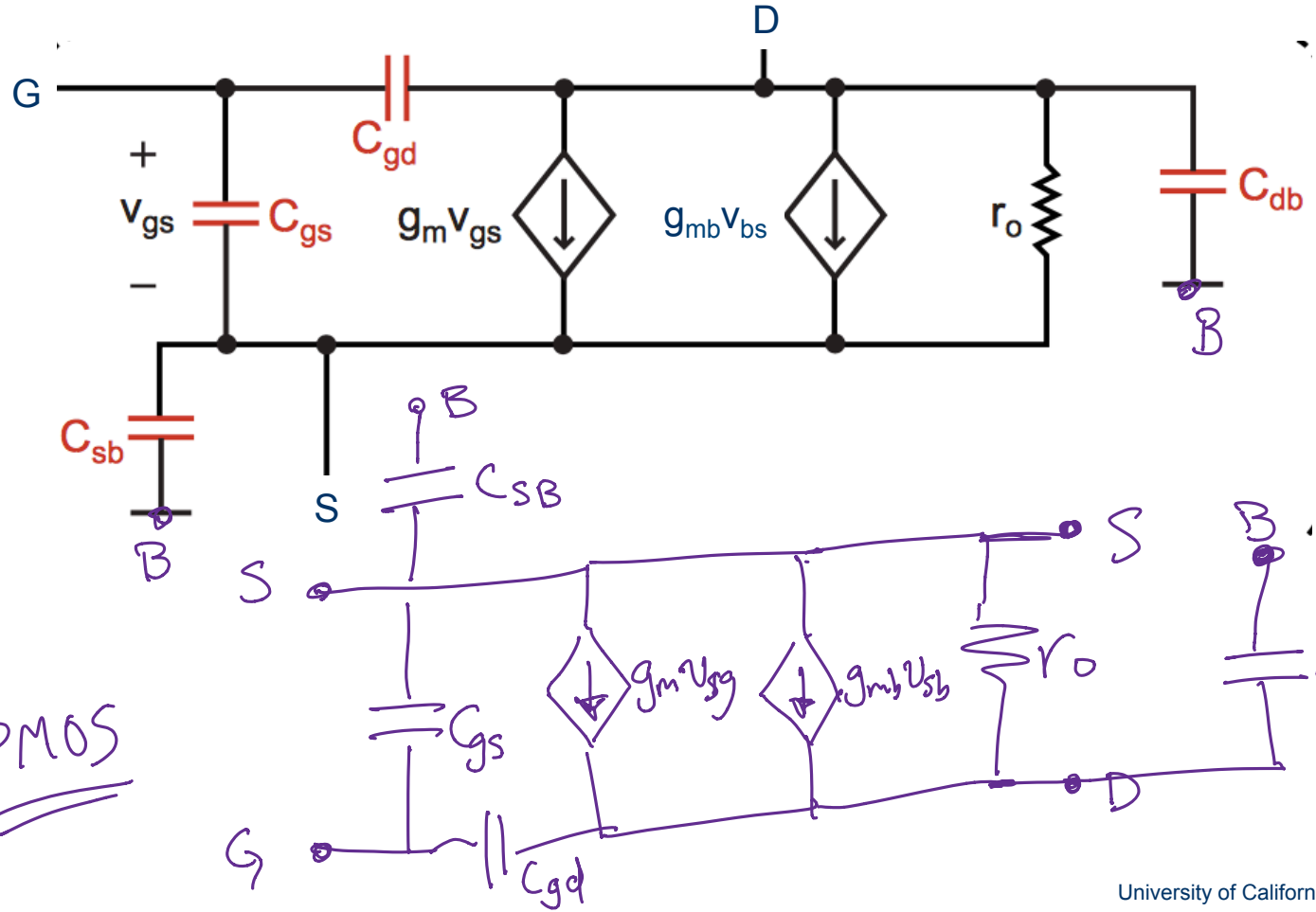
Complete Small-Signal Model NMOS



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Complete Small-Signal Model PMOS