Circuits and MOS Small-Signal Models

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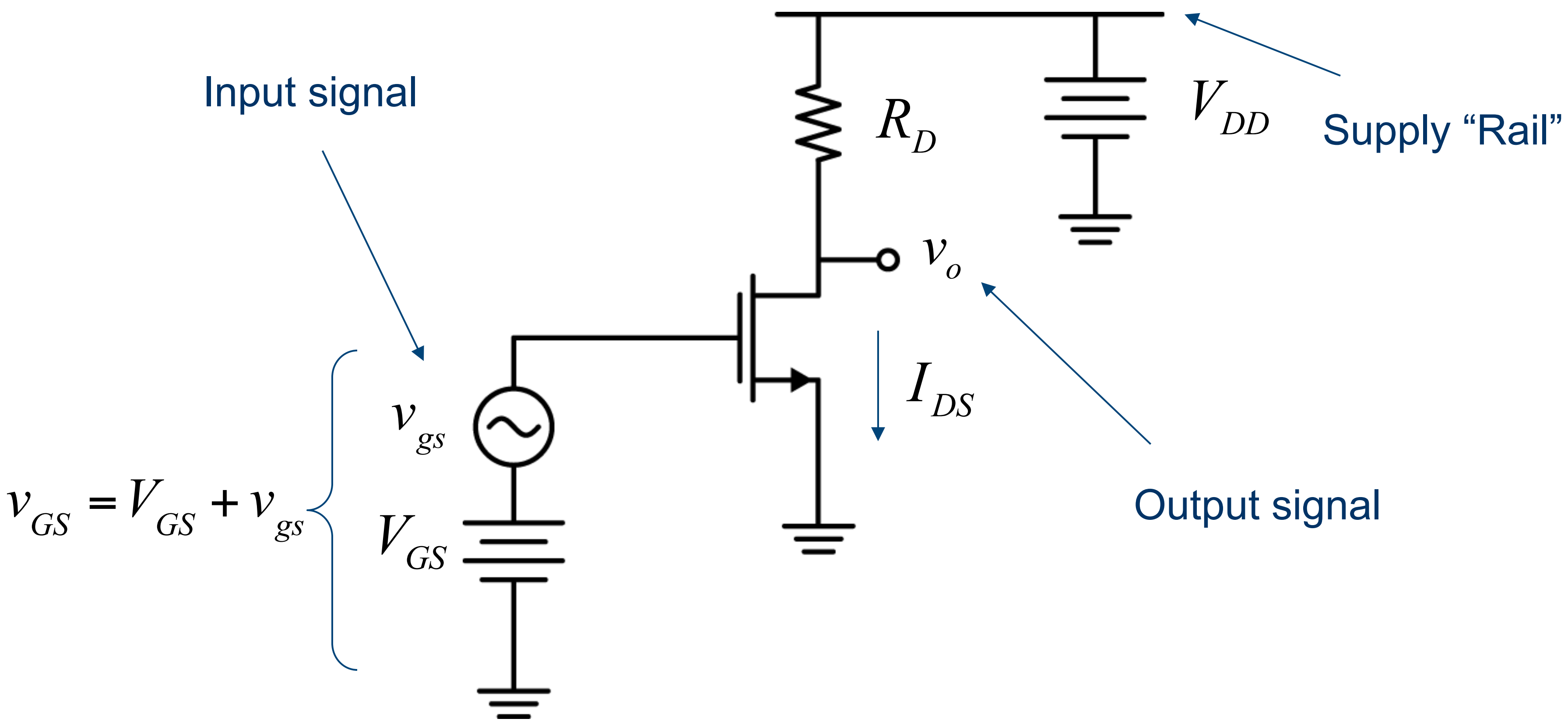
Announcements

- HW 7 is last HW before Midterm
- Next HW will be posted before Spring Break and due Friday after Spring Break (2 weeks to complete)
- Next week: Midterm Review (Tuesday), Midterm (Thursday)
- Syllabus after Spring Break will be updated

A Simple Circuit: An MOS Amplifier



Selecting the Output Bias Point

- The bias voltage V_{GS} is selected so that the output is mid-rail (between V_{DD} and ground)
- For gain, the transistor is biased in saturation
- Constraint on the DC drain current:

$$I_R = \frac{V_{DD} - V_o}{R_D} = \frac{V_{DD} - V_{DS}}{R_D}$$

- All the resistor current flows into transistor:

$$I_R = I_{DS,sat}$$

- Must ensure that this gives a self-consistent solution (transistor is biased in saturation)

$$V_{DS} > V_{GS} - V_T$$

Finding the Input Bias Voltage

- Ignoring the output impedance

$$I_{DS,sat} = \frac{W}{L}\mu_n C_{ox}\frac{1}{2}(V_{GS} - V_{Tn})^2$$

- Typical numbers: $W = 40$ μm, $L = 2$ μm, $R_D =$ 25kΩ, $\mu_n Cox = 100$ μA/V2, $V_{Tn} = 1$ V, $V_{DD} = 5$ V

$$I_{R_D} = \frac{V_{DD}}{2R_D} = I_{DS,sat} = \frac{W}{L}\mu_n C_{ox}\frac{1}{2}(V_{GS} - V_{Tn})^2$$

$$\frac{5\text{V}}{50\text{k}\Omega} = 100\mu\text{A} = 20 \cdot 100\frac{\mu\text{A}}{\text{V}^2} \cdot \frac{1}{2}(V_{GS} - 1)^2$$

$$.1 = (V_{GS} - 1V)^2 \qquad V_{GS} = 1.32V \qquad V_{GS} - V_T = .32V < V_{DS} = 2.5V \checkmark$$

Applying the Small-Signal Voltage

Approach I. Just use v_{GS} in the equation for the total drain current i_D and find v_{o}

$$v_{GS} = V_{GS} + v_{gs}$$

$$v_s = \hat{v}_s \cos \omega t$$

$$v_O = V_{DD} - R_D i_{DS} = V_{DD} - R_D \mu_n C_{ox} \frac{W}{L} \frac{1}{2} (V_{GS} + v_{gs} - V_T)^2$$

Note: Neglecting charge storage effects. Ignoring device output impedance.

Solving for the Output Voltage v_O

$$v_O = V_{DD} - R_D i_{DS} = V_{DD} - R_D \mu_n C_{ox} \frac{W}{L} \frac{1}{2} (V_{GS} + v_{gs} - V_T)^2$$

$$v_O = V_{DD} - R_D i_{DS} = V_{DD} - R_D \underbrace{\mu_n C_{ox} \frac{W}{L} \frac{1}{2} (V_{GS} - V_T)^2}_{I_{DS}} \left(1 + \frac{v_{gs}}{V_{GS} - V_T}\right)^2$$

$$v_O = V_{DD} - \underbrace{R_D I_{DS}}_{\frac{V_{DD}}{2}} \left(1 + \frac{v_{gs}}{V_{GS} - V_T}\right)^2$$

Small-Signal Case

- Linearize the output voltage for the s.s. case
- Expand $(1 + x)^2 = 1 + 2x + x^2$ … last term can be dropped when $x << 1$

$$\left(1+\frac{2v_{gs}}{V_{GS}-V_T}\right)^2 = 1+\frac{2v_{gs}}{V_{GS}-V_T}+\left(\frac{v_{gs}}{V_{GS}-V_T}\right)^2$$

Neglect

$$v_O \approx V_{DD} - R_D I_{DS}\left(1+\frac{2v_{gs}}{V_{GS}-V_T}\right)$$

Linearized Output Voltage

For this case, the total output voltage is:

$$v_O \approx V_{DD} - I_D R_{DS}\left(1 + \frac{2v_{gs}}{V_{GS} - V_T}\right)$$

$$v_O \approx (V_{DD} - I_D R_{DS}) - \frac{2 I_D R_{DS} v_{gs}}{V_{GS} - V_T} = \frac{V_{DD}}{2} - \frac{V_{DD} v_{gs}}{V_{GS} - V_T}$$

"DC"

Small-signal output

The small-signal output voltage:

$$v_o \approx -\frac{2 I_D R_{DS} v_{gs}}{V_{GS} - V_T} = -\frac{V_{DD} v_{gs}}{V_{GS} - V_T} A_v v_{gs}$$

Voltage gain

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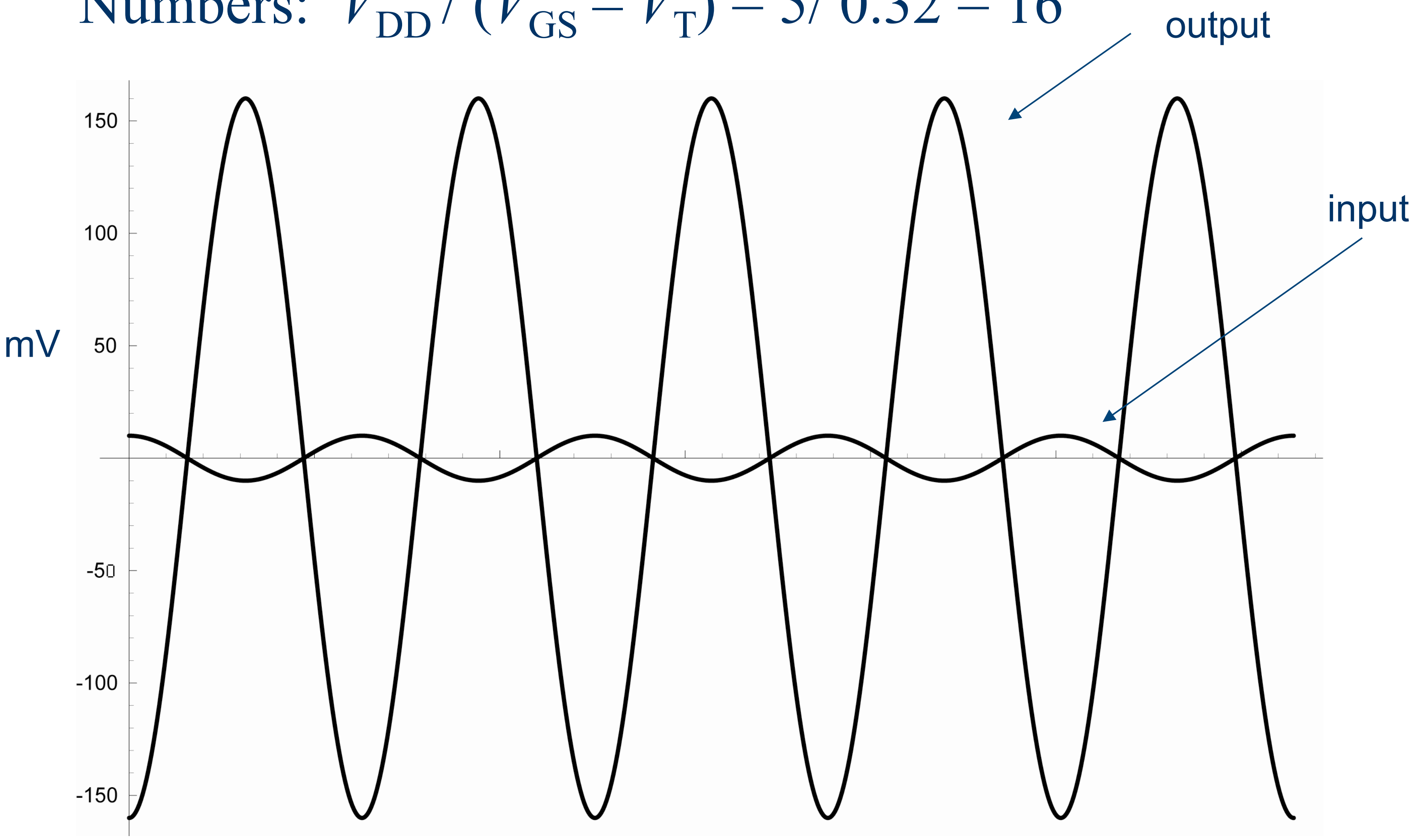
Plot of Output Waveform (Gain!)

Numbers: $V_{\mathrm{DD}} / (V_{\mathrm{GS}} - V_{\mathrm{T}}) = 5/ 0.32 = 16$



There is a Better Way!

- *What's missing: didn't include device output impedance or charge storage effects (must solve non-linear differential equations…)*
- *Approach II*: Solve problem in two steps.
  - 1) DC voltages and currents (ignore small signals sources): set bias point of the MOSFET ... we had to do this to pick V_{GS} already
  - 2) Substitute the small-signal model of the MOSFET and the small-signal models of the other circuit elements …
- This constitutes small-signal analysis

Total Small Signal Current

$$i_{DS}(t) = I_{DS} + i_{ds}$$

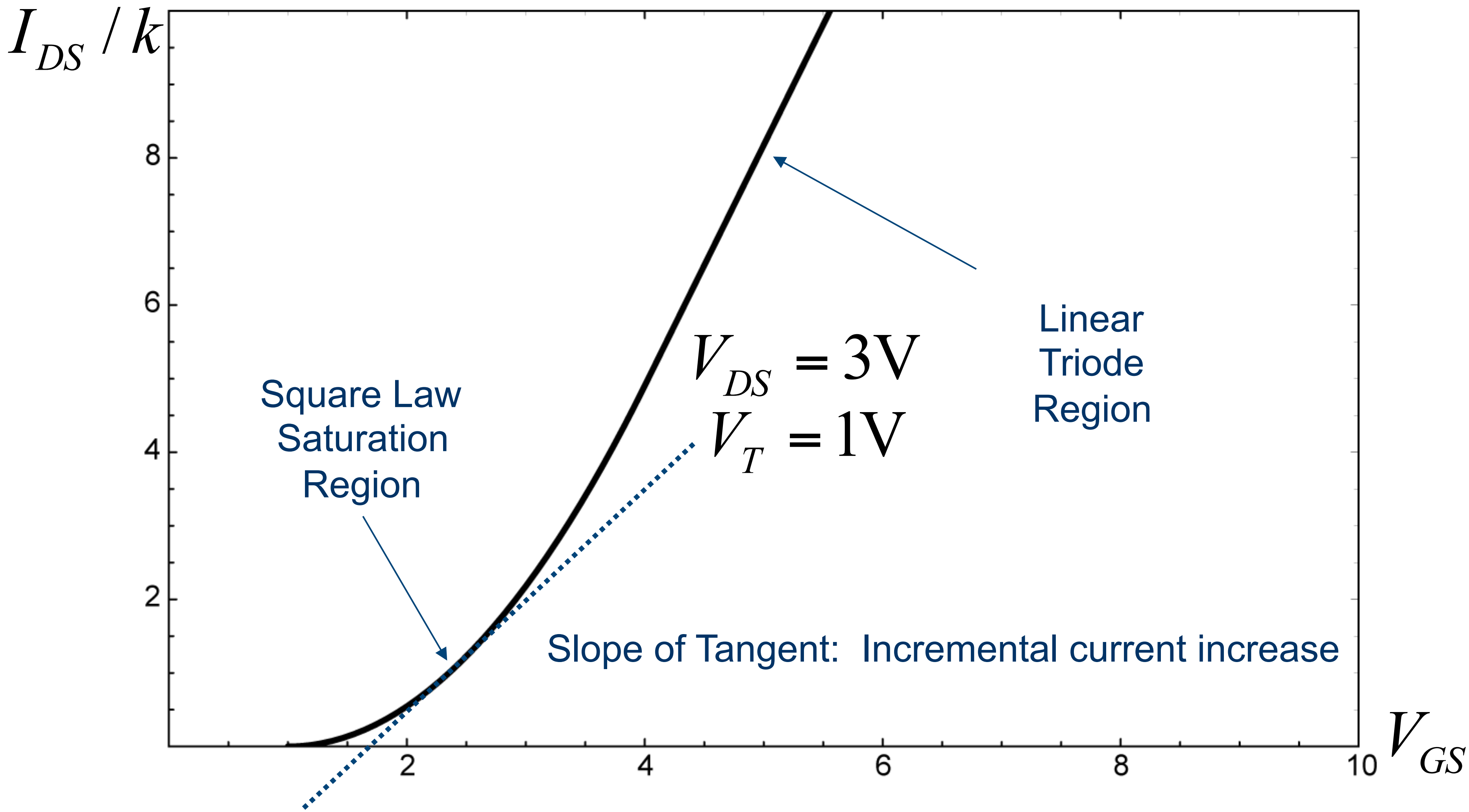
$$i_{ds} = \frac{\partial i_{DS}}{\partial v_{gs}} v_{gs} + \frac{\partial i_{DS}}{\partial v_{ds}} v_{ds}$$

$$i_{ds} = g_m v_{gs} + \frac{1}{r_o} v_{ds}$$

*Trans*conductance

Conductance

Changing One Variable at a Time



Assumption: $V_{DS} > V_{DS,SAT} = V_{GS} - V_{Tn}$ (square law)

The *Transconductance* g_m

Defined as the change in drain current due to a change in the *gate-source* voltage, with *everything else constant*

$$I_{DS,sat} = \frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

$$g_m = \left.\frac{\Delta i_D}{\Delta v_{GS}}\right|_{V_{GS},V_{DS}} = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{V_{GS},V_{DS}} = \mu C_{ox}\frac{W}{L}(V_{GS}-V_T)(1+\lambda V_{DS})$$

$\lambda V_{DS} \approx 0$

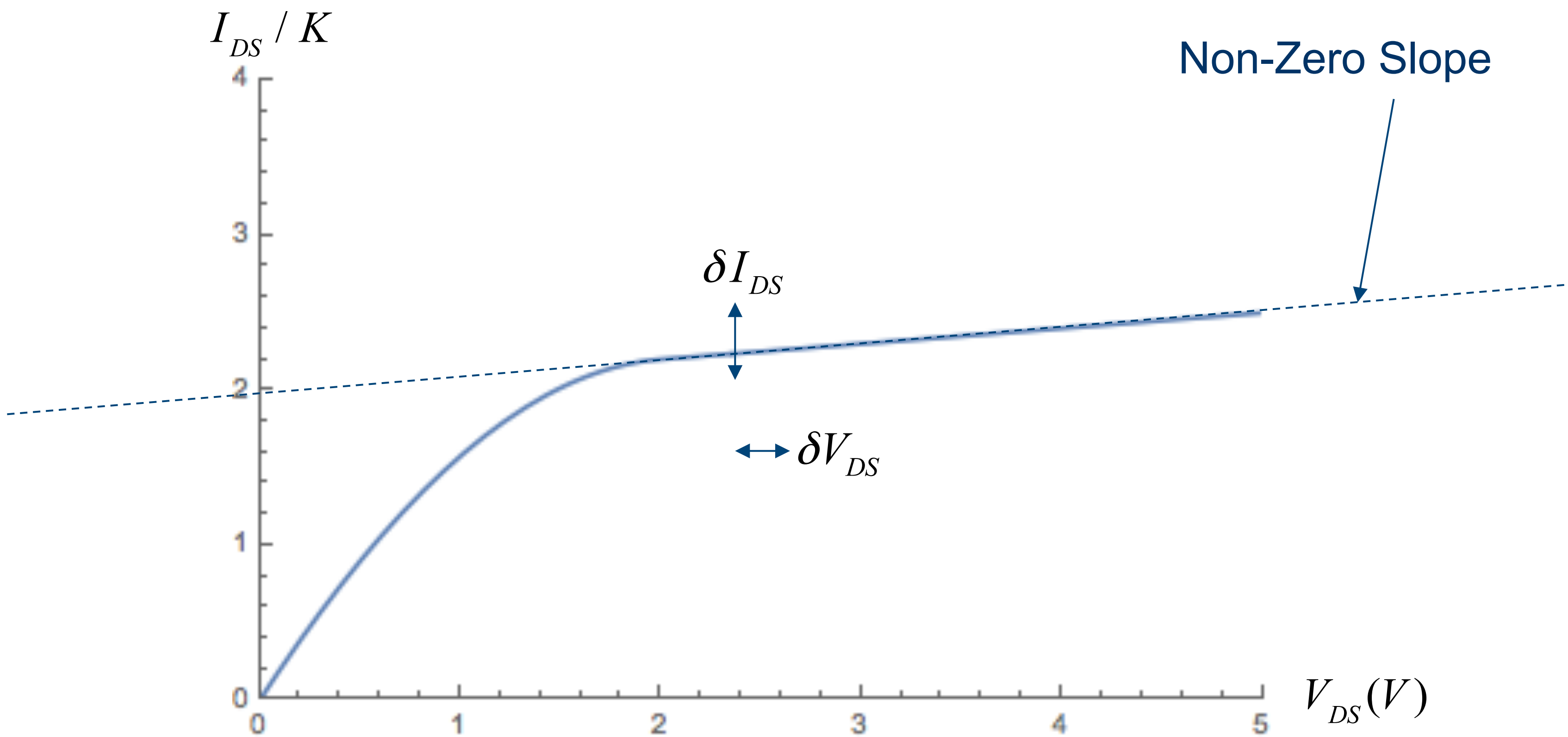
$$g_m = \mu C_{ox}\frac{W}{L}(V_{GS}-V_T)$$ ← Gate Bias

$$g_m = \mu C_{ox}\frac{W}{L}\sqrt{\frac{2I_{DS}}{\frac{W}{L}\mu C_{ox}}} = \sqrt{2\mu C_{ox}\frac{W}{L}I_{DS}}$$ ← Drain Current Bias

$$g_m = \frac{2I_{DS}}{(V_{GS}-V_T)}$$ ← Drain Current Bias and Gate Bias

Output Resistance r_o

Defined as the inverse of the change in drain current due to a change in the *drain-source* voltage, with *everything else constant*



Evaluating r_o

$$i_D = \frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$r_o = \left(\left. \frac{\partial i_D}{\partial v_{DS}} \right|_{V_{GS}, V_{DS}} \right)^{-1}$$

$$r_0 = \frac{1}{\frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS} - V_T)^2 \lambda}$$

$$r_0 \approx \frac{1}{\lambda I_{DS}}$$

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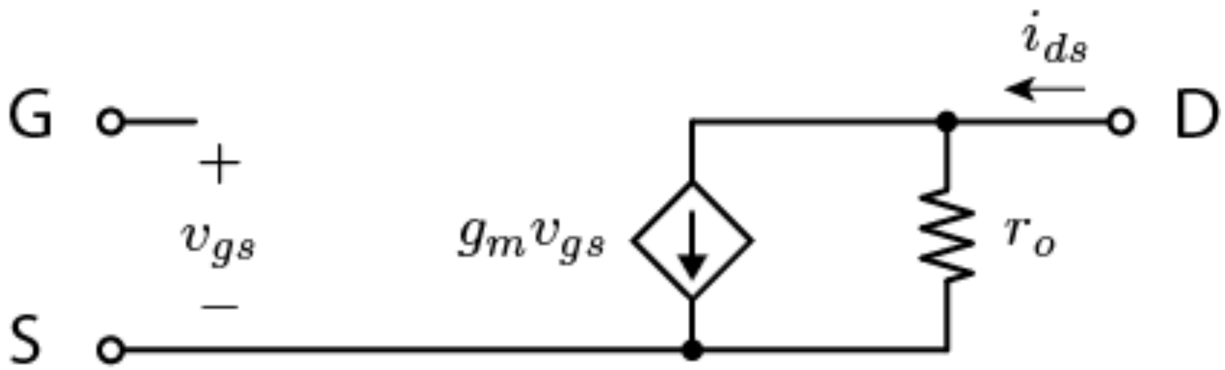
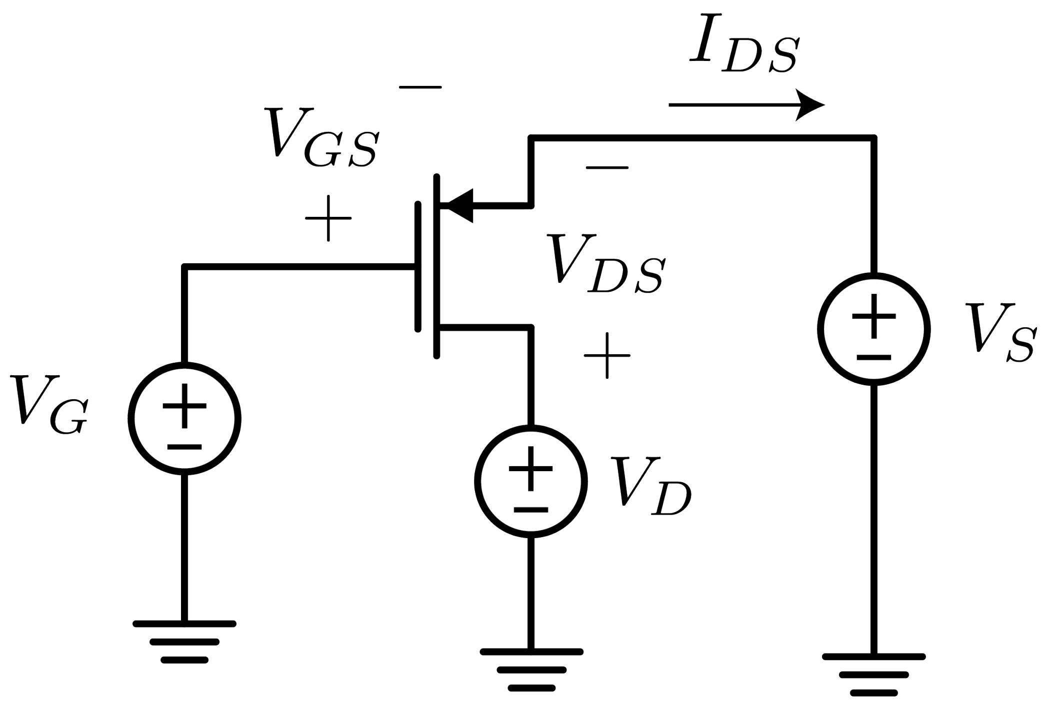
Three-Terminal Small-Signal Model



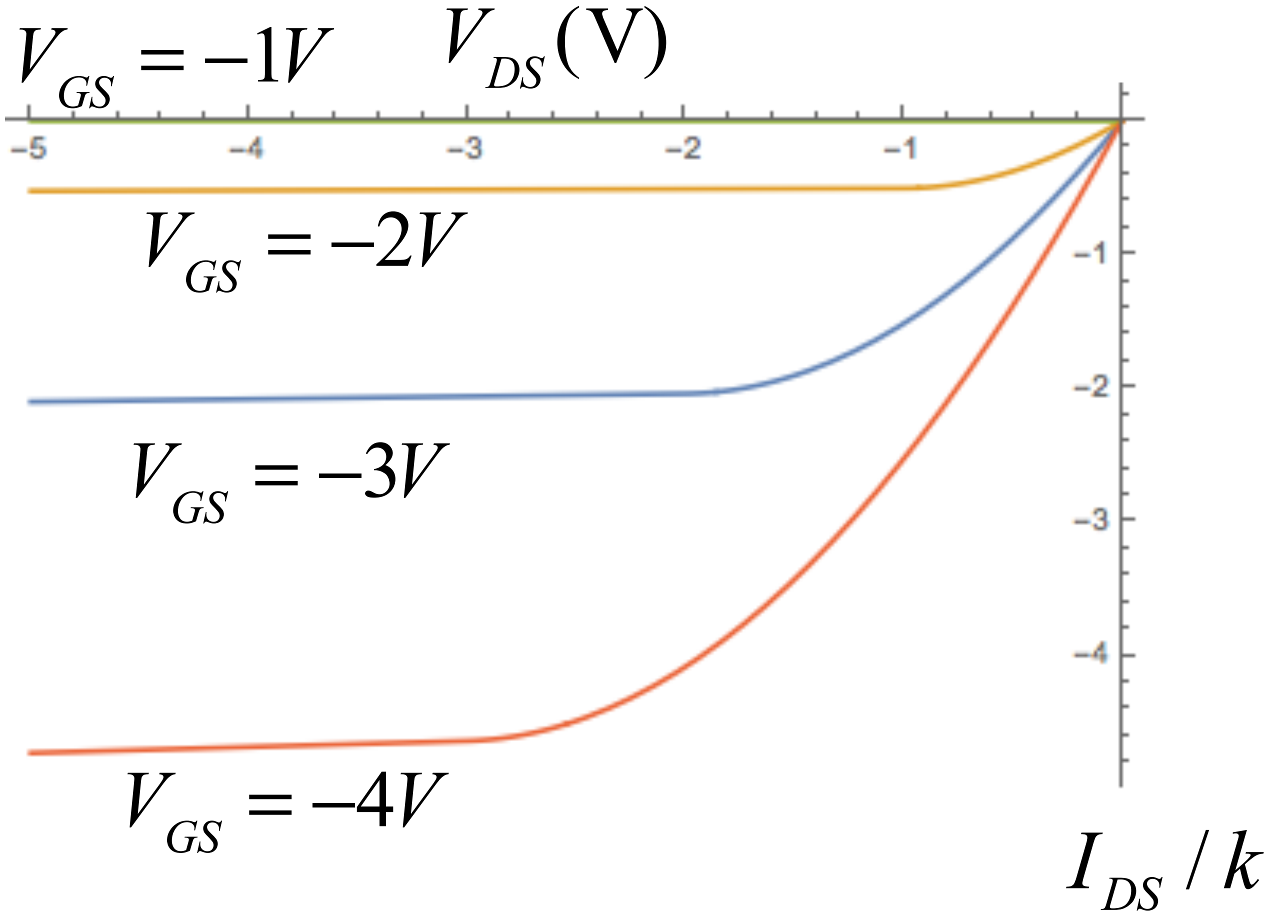
$$i_{ds} = g_m v_{gs} + \frac{1}{r_o} v_{ds}$$

P-Channel MOSFET

Everything is flipped around compared to an NMOS.
Currents are negative of NMOS.



Square-Law PMOS Characteristics



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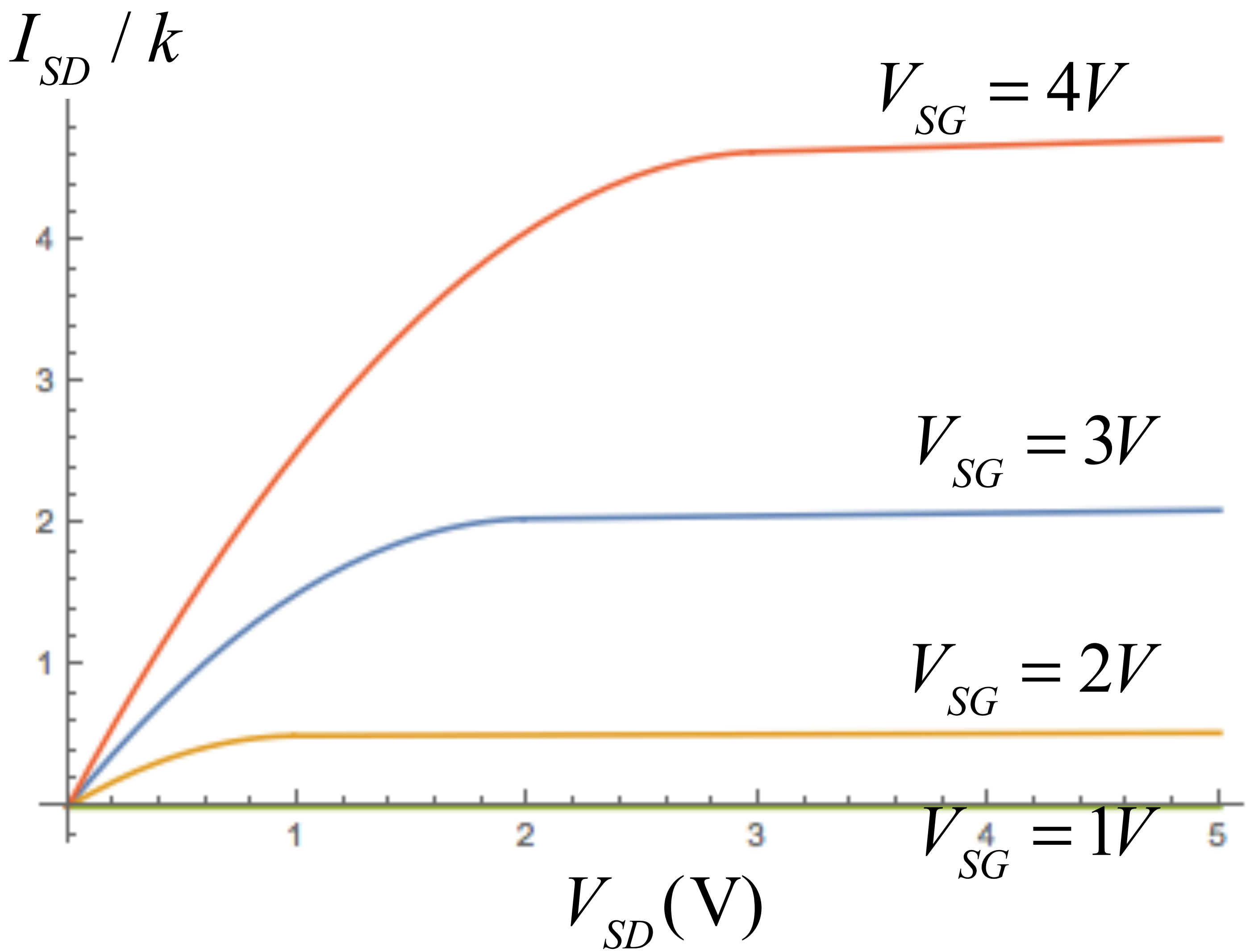
Right Side Up!



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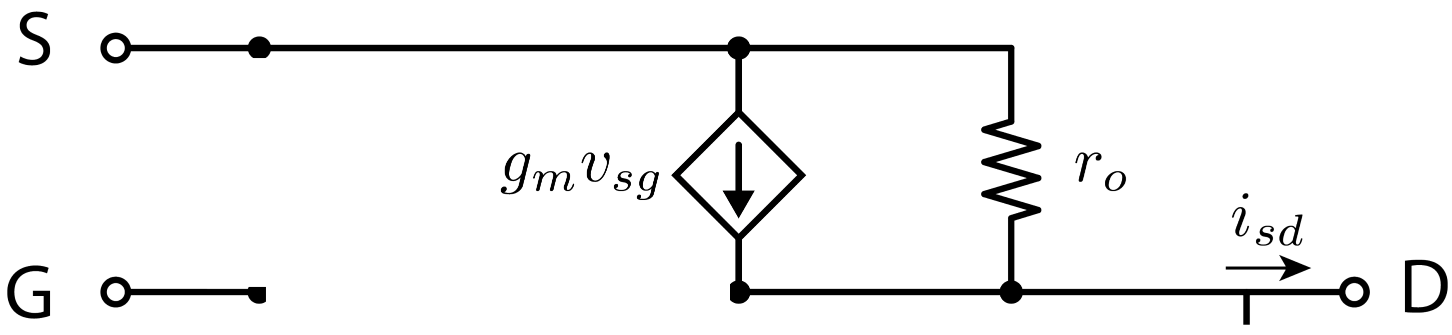
Small-Signal PMOS Model



What we're ignoring for now…

- The fourth terminal of the MOSFET is the body of the transistor… it can act like a second gate, or "back gate"
- The junctions of the transistor form pn-junction diodes with body, this introduces parasitic capacitance
- Modern transistors are very short channel lengths, and there are many "short channel" effects that we're ignoring, most prominently velocity saturation
- Subthreshold conduction
- Capacitance!