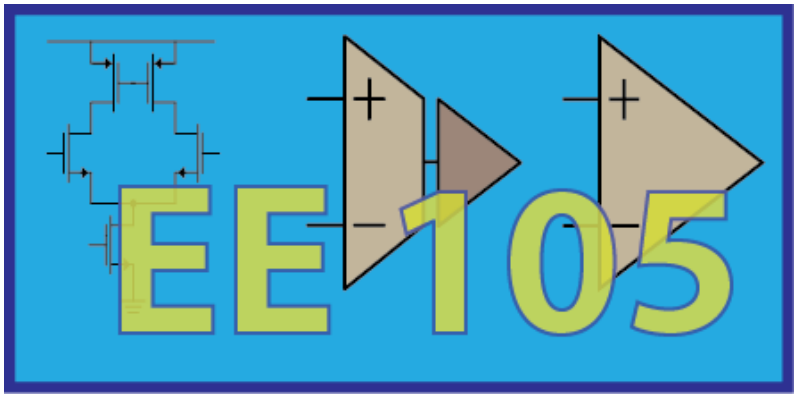

Circuits and MOS Small-Signal Models

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Announcements

- HW 7 is last HW before Midterm
- Next HW will be posted before Spring Break and due Friday after Spring Break (2 weeks to complete)
- Next week: Midterm Review (Tuesday), Midterm (Thursday)
- Syllabus after Spring Break will be updated

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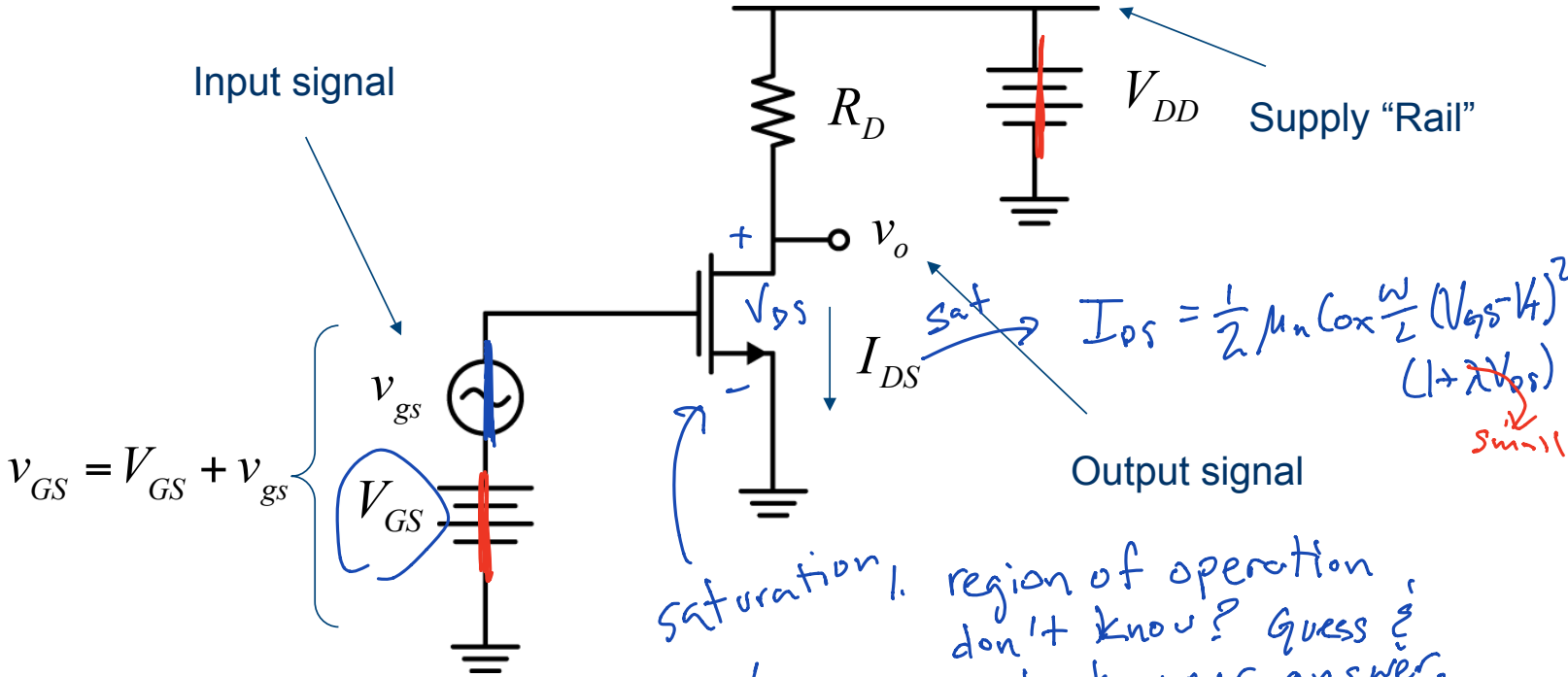
A Simple Circuit: An MOS Amplifier



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Selecting the Output Bias Point

- The bias voltage V_{GS} is selected so that the output is mid-rail (between V_{DD} and ground)
- For gain, the transistor is biased in saturation
- Constraint on the DC drain current:

$$I_R = \frac{V_{DD} - V_o}{R_D} = \frac{V_{DD} - V_{DS}}{R_D}$$

- All the resistor current flows into transistor:

$$I_R = I_{DS,sat}$$

- Must ensure that this gives a self-consistent solution (transistor is biased in saturation)

$$V_{DS} > V_{GS} - V_T$$

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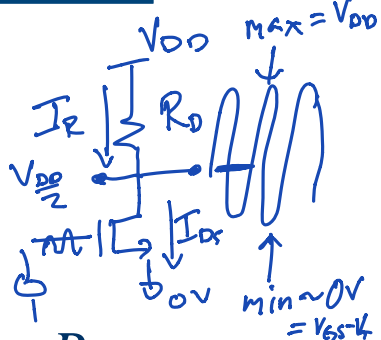
Finding the Input Bias Voltage

- Ignoring the output impedance

$$I_{DS,sat} = \frac{W}{L}\mu_n C_{ox}\frac{1}{2}(V_{GS} - V_{Tn})^2$$



- Typical numbers: $W = 40\ \mu m$, $L = 2\ \mu m$, $R_D = 25k\Omega$, $\mu_n Cox = 100\ \mu A/V2$, $V_{Tn} = 1\ V$, $V_{DD} = 5\ V$

$$I_{R_D} = \frac{V_{DD}}{2R_D} = I_{DS,sat} = \frac{W}{L}\mu_n C_{ox}\frac{1}{2}(V_{GS} - V_{Tn})^2$$

$$\frac{5V}{50k\Omega} = 100\mu A = 20\cdot 100\frac{\mu A}{V^2}\cdot\frac{1}{2}(V_{GS} - 1)^2$$

$$.1 = (V_{GS} - 1V)^2 \qquad V_{GS} = 1.32V \qquad V_{GS} - V_T = .32V < V_{DS} = 2.5V$$

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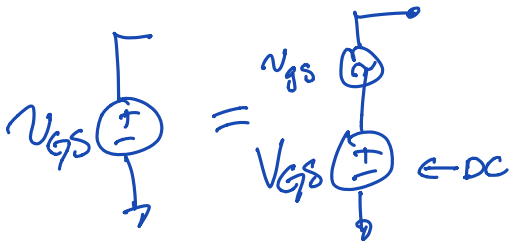
Applying the Small-Signal Voltage

Approach I. Just use v_{GS} in the equation for the total drain current i_D and find v_o

$$v_{GS} = V_{GS} + v_{gs}$$

$$v_{gs} = \hat{v}_{gs} \cos \omega t$$



$$v_O = V_{DD} - R_D i_{DS} = V_{DD} - R_D \mu_n C_{ox} \frac{W}{L} \frac{1}{2} (V_{GS} + v_{gs} - V_T)^2$$

I_{DS}

$I_{DS} + i_{ds}$

Note: Neglecting charge storage effects. Ignoring device output impedance.

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Solving for the Output Voltage v_O

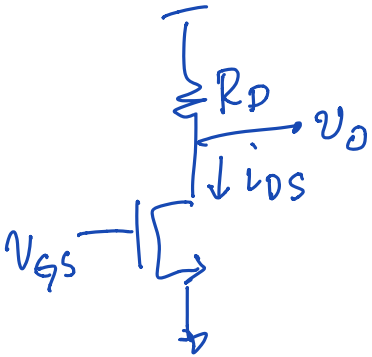
$$v_O = V_{DD} - R_D i_{DS} = V_{DD} - R_D \mu_n C_{ox} \frac{W}{L}\frac{1}{2}(V_{GS} + v_{gs} - V_T)^2$$

$$v_O = V_{DD} - R_D i_{DS} = V_{DD} - R_D \mu_n C_{ox} \frac{W}{L}\frac{1}{2}(V_{GS} - V_T)^2 \left(1 + \frac{v_{gs}}{V_{GS} - V_T}\right)^2$$

$$I_{DS}$$

$$v_O = V_{DD} - R_D I_{DS} \left(1 + \frac{v_{gs}}{V_{GS} - V_T}\right)^2$$

$$\frac{V_{DD}}{2}$$



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Small-Signal Case

- Linearize the output voltage for the s.s. case
- Expand $(1+x)^2 = 1 + 2x + x^2$ … last term can be dropped when $x << 1$

if small

$$\left(1+\frac{v_{gs}}{V_{GS}-V_T}\right)^2 = 1+\frac{2v_{gs}}{V_{GS}-V_T}+\left(\frac{v_{gs}}{V_{GS}-V_T}\right)^2$$

Neglect

$$v_O \approx V_{DD} - R_D I_{DS}\left(1+\frac{2v_{gs}}{V_{GS}-V_T}\right)$$

new term $\propto f(v_{gs})$

Output DC bias $= \frac{V_{DD}}{2}$

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Linearized Output Voltage

For this case, the total output voltage is:

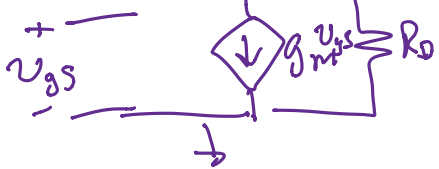
$$v_O \approx V_{DD} - I_D R_{DS}\left(1 + \frac{2v_{gs}}{V_{GS} - V_T}\right)$$

special case

$$v_O \approx \underbrace{(V_{DD} - I_D R_{DS}) - \frac{2I_D R_{DS} v_{gs}}{V_{GS} - V_T}}_{\text{“DC”}} = \frac{V_{DD}}{2} - \frac{V_{DD} v_{gs}}{V_{GS} - V_T}$$

Small-signal output

The small-signal output voltage:



$$v_o \approx -\frac{2I_D R_{DS} v_{gs}}{V_{GS} - V_T} = -\frac{V_{DD} v_{gs}}{V_{GS} - V_T} = A_v v_{gs}$$

g_m

A_v

Voltage gain

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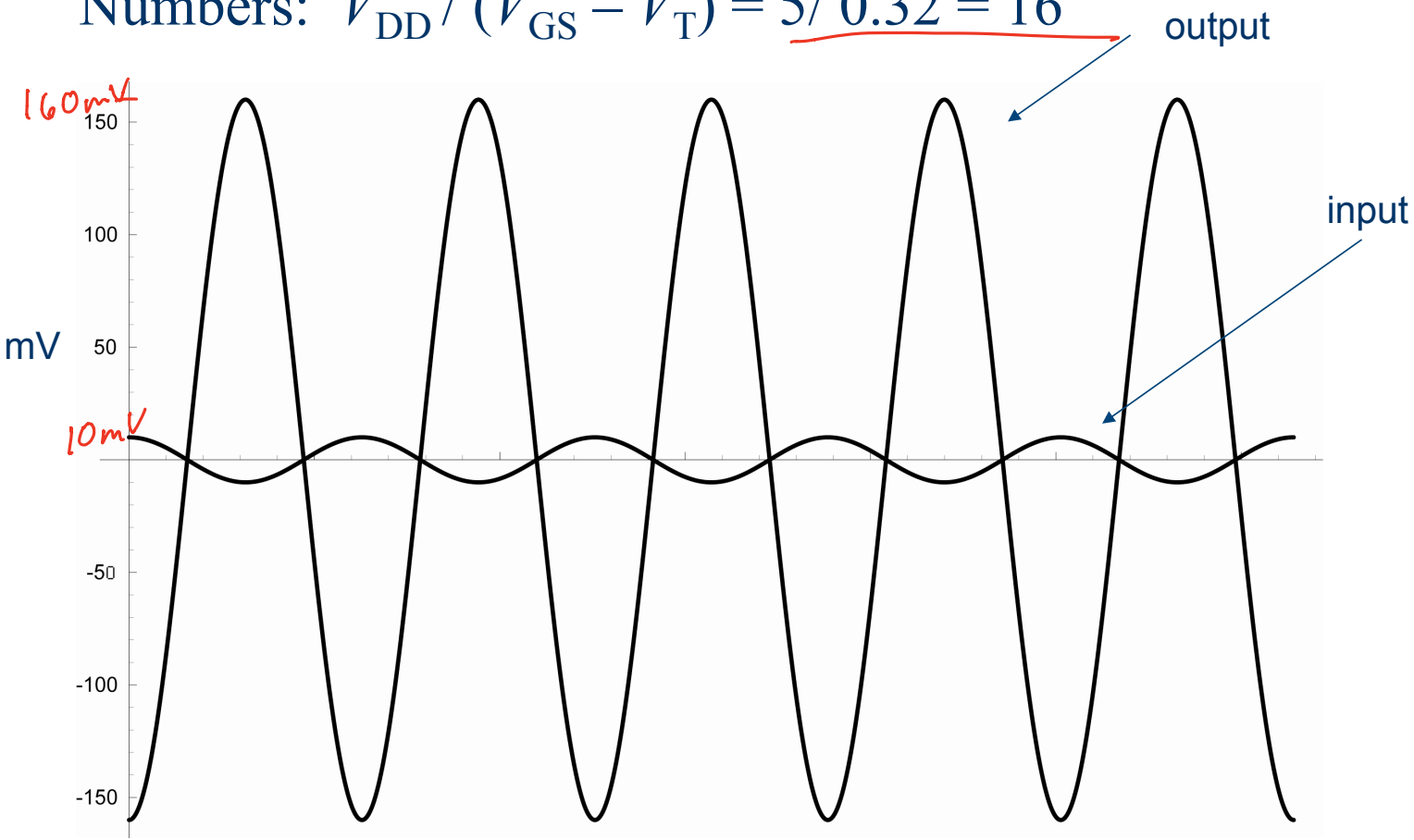
Plot of Output Waveform (Gain!)

Numbers: $V_{DD} / (V_{GS} - V_T) = 5/ 0.32 = 16$



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There is a Better Way!

- *What's missing: didn't include device output impedance or charge storage effects (must solve non-linear differential equations…)*
- *Approach II*: Solve problem in two steps.
  - 1) DC voltages and currents (ignore small signals sources): set bias point of the MOSFET ... we had to do this to pick V_{GS} already
  - 2) Substitute the small-signal model of the MOSFET and the small-signal models of the other circuit elements …
- This constitutes small-signal analysis

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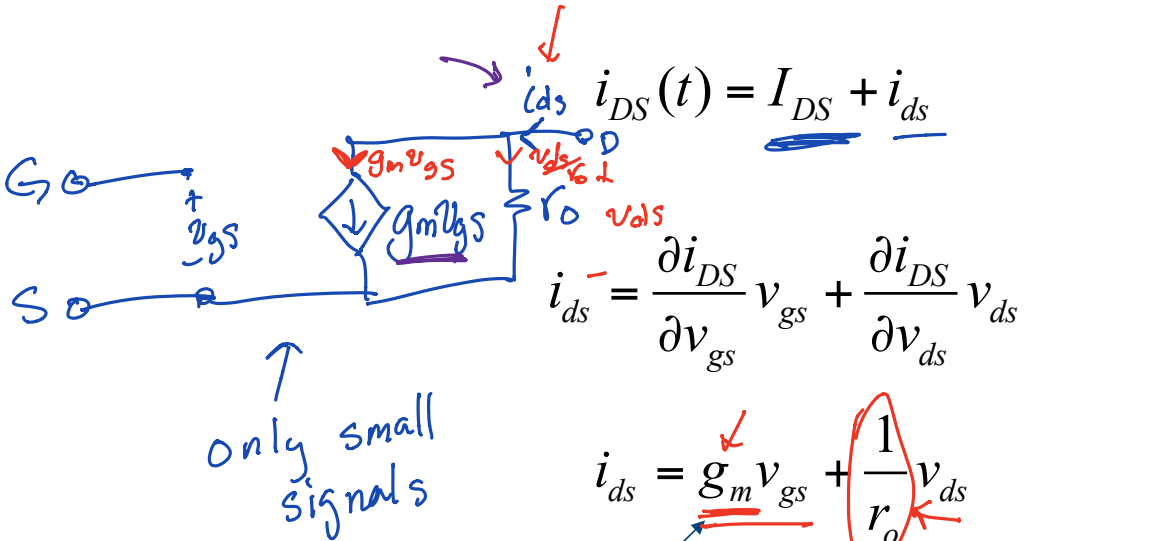
Total Small Signal Current



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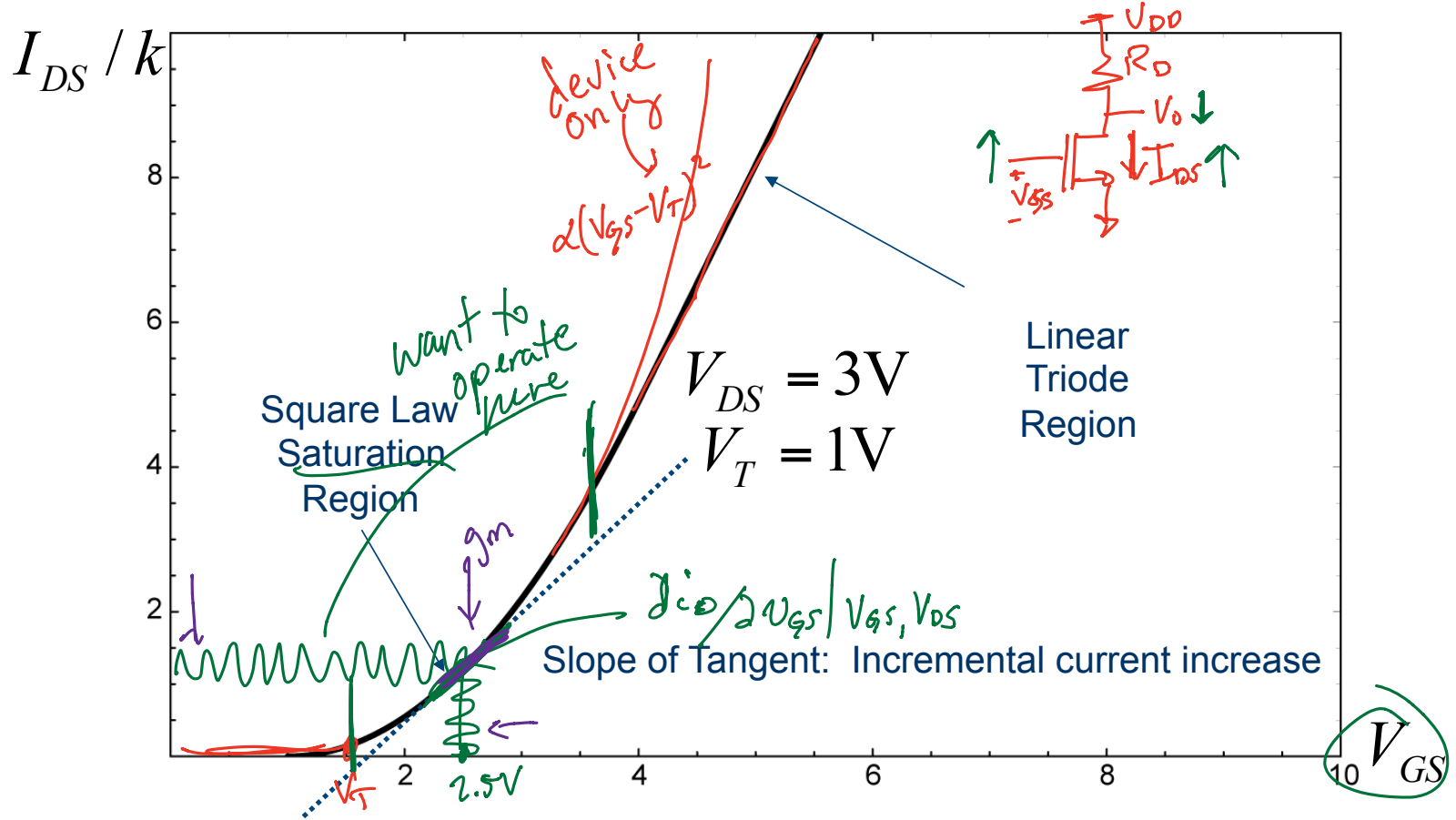
Changing One Variable at a Time



Assumption: $V_{DS} > V_{DS,SAT} = V_{GS} - V_{Tn}$ (square law)

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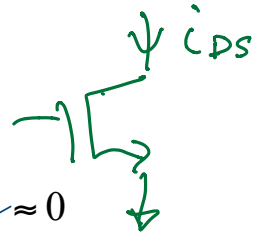
The *Transconductance* g_m

Defined as the change in drain current due to a change in the *gate-source* voltage, with *everything else constant*



$$I_{DS,sat} = \frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

Bias, small

$$g_m = \left.\frac{\Delta i_D}{\Delta v_{GS}}\right|_{V_{GS},V_{DS}} = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{V_{GS},V_{DS}} = \mu C_{ox}\frac{W}{L}(V_{GS}-V_T)(1+\lambda V_{DS})$$

What is the slope at our bias point

$$g_m = \mu C_{ox}\frac{W}{L}(V_{GS}-V_T)$$ ← Gate Bias

$$g_m = \mu C_{ox}\frac{W}{L}\sqrt{\frac{2I_{DS}}{\frac{W}{L}\mu C_{ox}}} = \sqrt{2\mu C_{ox}\frac{W}{L}I_{DS}}$$ ← Drain Current Bias

$I_{DS} = \frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS}-V_T)^2$

$g_m = \frac{W}{L}\mu C_{ox}(V_{GS}-V_T)$

$$g_m = \frac{2I_{DS}}{(V_{GS}-V_T)}$$ ← Drain Current Bias and Gate Bias

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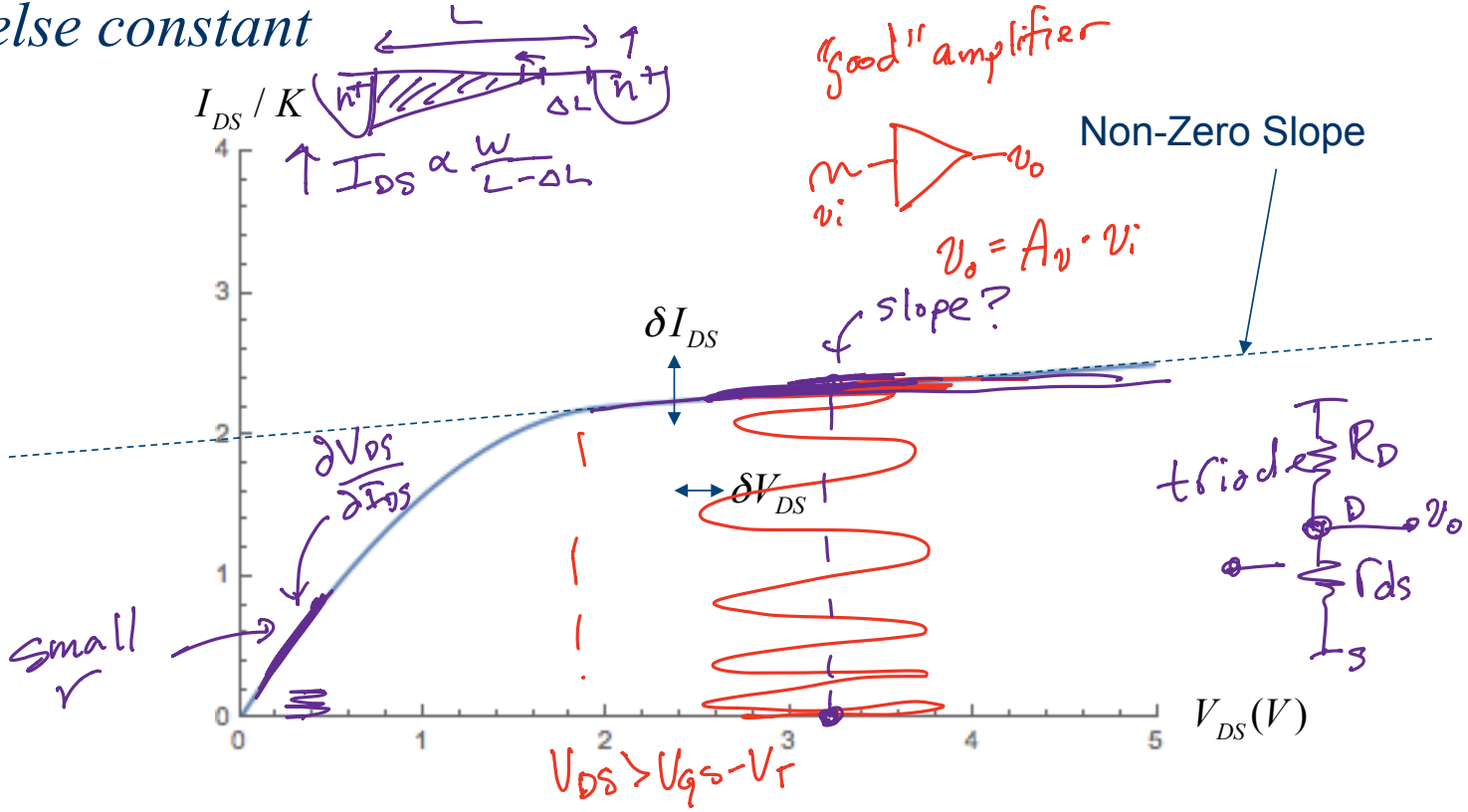
Output Resistance r_o

Defined as the inverse of the change in drain current due to a change in the *drain-source* voltage, with *everything else constant*



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Evaluating r_o

$$i_{DS} = \frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

$$r_o = \left(\left. \frac{\partial i_{DS}}{\partial v_{DS}} \right|_{V_{GS}, V_{DS}} \right)^{-1} = \left[\frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS} - V_T)^2 \lambda \right]^{-1}$$

$$r_0 = \frac{1}{\frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS} - V_T)^2 \lambda}$$

I_{DS}

should be large → $r_0 \approx \frac{1}{\lambda I_{DS}}$

$\lambda = 0$

$r_0 = \infty$

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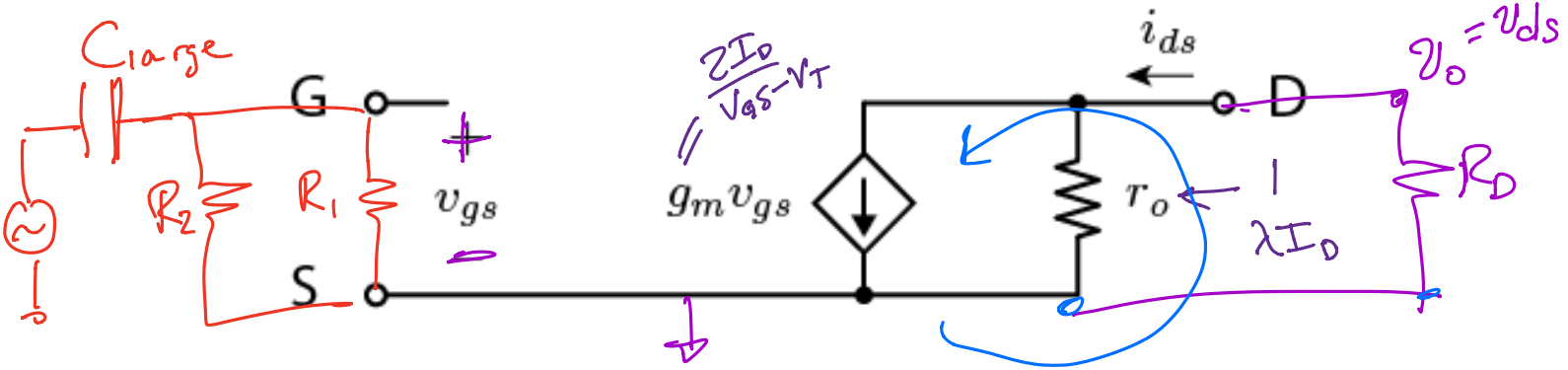
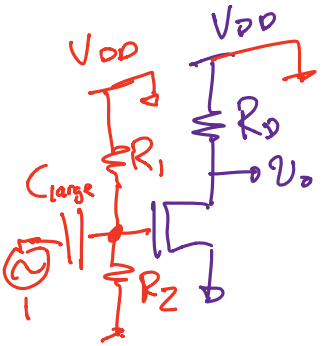
Three-Terminal Small-Signal Model





$$i_{ds} = g_m v_{gs} + \frac{1}{r_o} v_{ds} = g_m v_{gs} + \frac{1}{r_o} v_o$$

$$= \underbrace{\frac{2I_D}{V_{GS}-V_t}}\, v_{gs} + \lambda I_D v_o$$

$$v_o = -R_D\left(g_m v_{gs} + \frac{1}{r_o} v_o\right)$$

$$v_o\left(1+\frac{R_D}{r_o}\right) = -R_D g_m v_{gs}$$

simpler way

$v_o \,//\, R_D$

$v_o = -g_m v_{gs}\,(r_o \,//\, R_D)$

"inspection"

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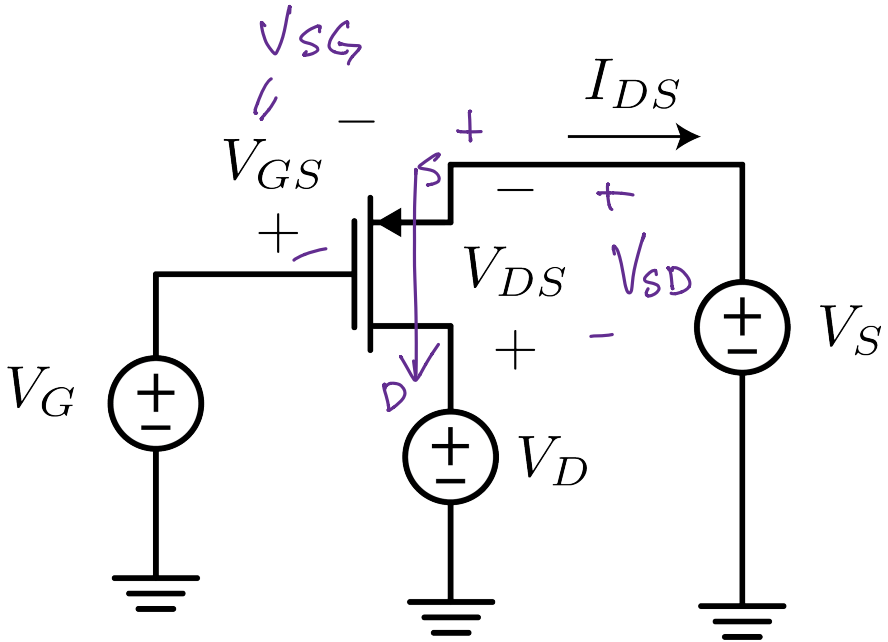
P-Channel MOSFET

Everything is flipped around compared to an NMOS.
Currents are negative of NMOS.



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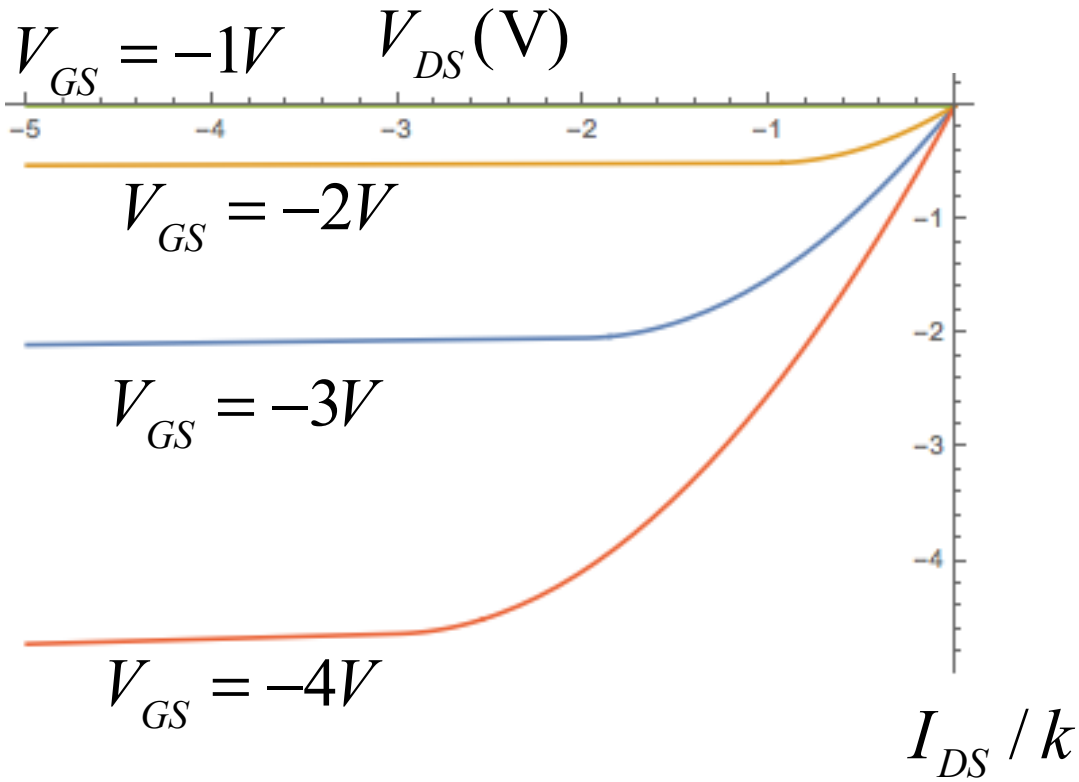
Square-Law PMOS Characteristics



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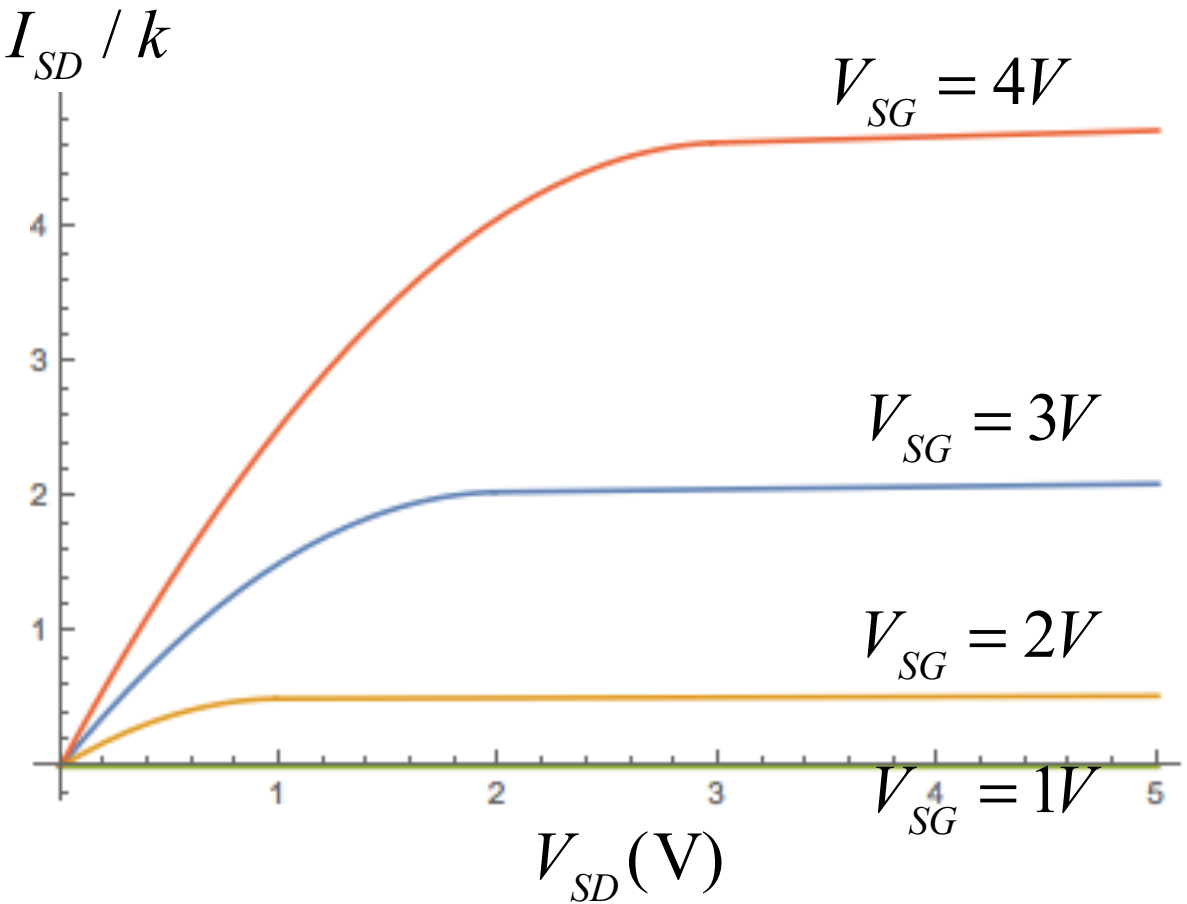
Right Side Up!



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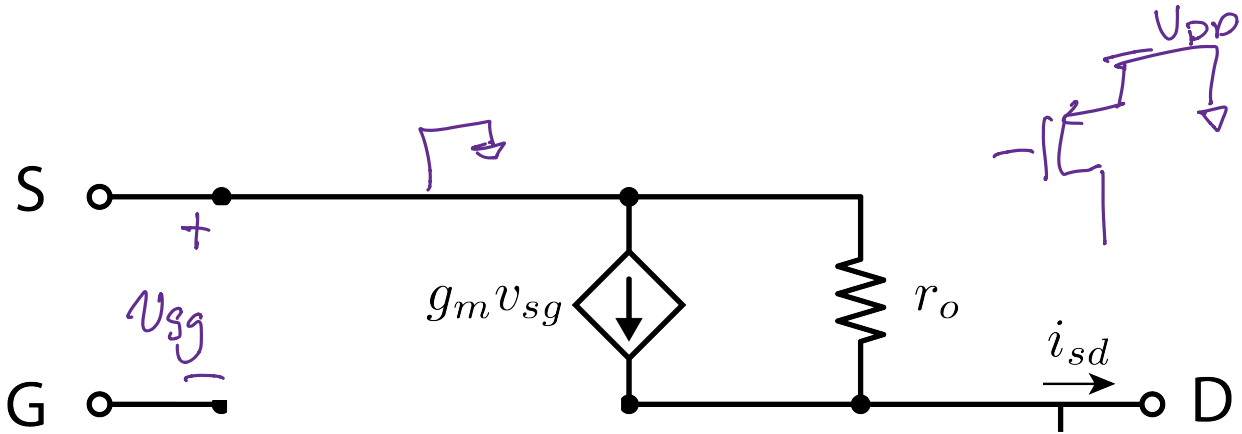
Small-Signal PMOS Model



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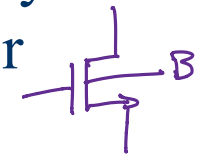
What we're ignoring for now…

- The fourth terminal of the MOSFET is the body of the transistor… it can act like a second gate, or "back gate"



- The junctions of the transistor form pn-junction diodes with body, this introduces parasitic capacitance
- Modern transistors are very short channel lengths, and there are many "short channel" effects that we're ignoring, most prominently velocity saturation EE140
- Subthreshold conduction $V_{GS} < V_T$ "weak inversion" $i_{DS} = 0$
- Capacitance!