

Module 2.2: IC Resistors and Capacitors

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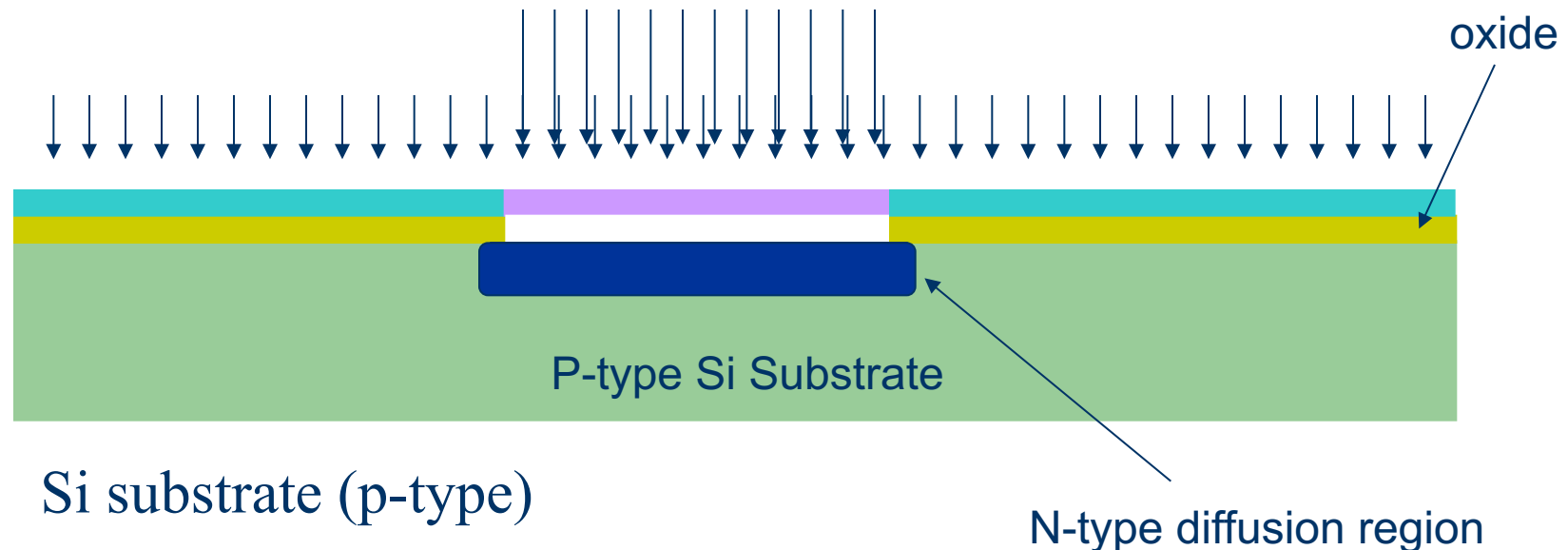
IC Fabrication: Si Substrate

- Pure Si crystal is starting material (wafer)
- The Si wafer is extremely pure (~ 1 part in a billion impurities)
- Why so pure?
 - Si density is about 5×10^{22} atoms/cm³
 - Desire intentional doping from $10^{14} - 10^{18}$
 - Want unintentional dopants to be about 1-2 orders of magnitude less dense $\sim 10^{12}$
- Si wafers are polished to about 700 μm thick (mirror finish)
- The Si forms the substrate for the IC

IC Fabrication: Oxide

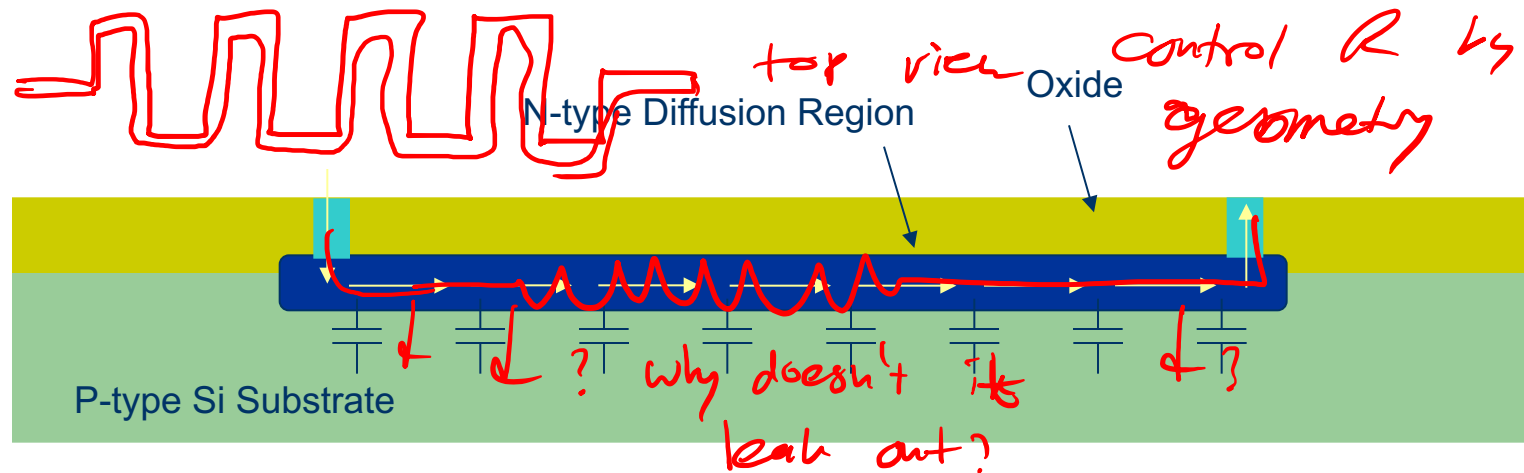
- Si has a native oxide: SiO_2
- SiO_2 (Quartz) is extremely stable and very convenient for fabrication
- It's an insulators so it can be used for house interconnection
- It can also be used for selective doping
- SiO_2 windows are etched using photolithography
- These openings allow ion implantation into selected regions
- SiO_2 can block ion implantation in other areas

IC Fabrication: Ion Implantation



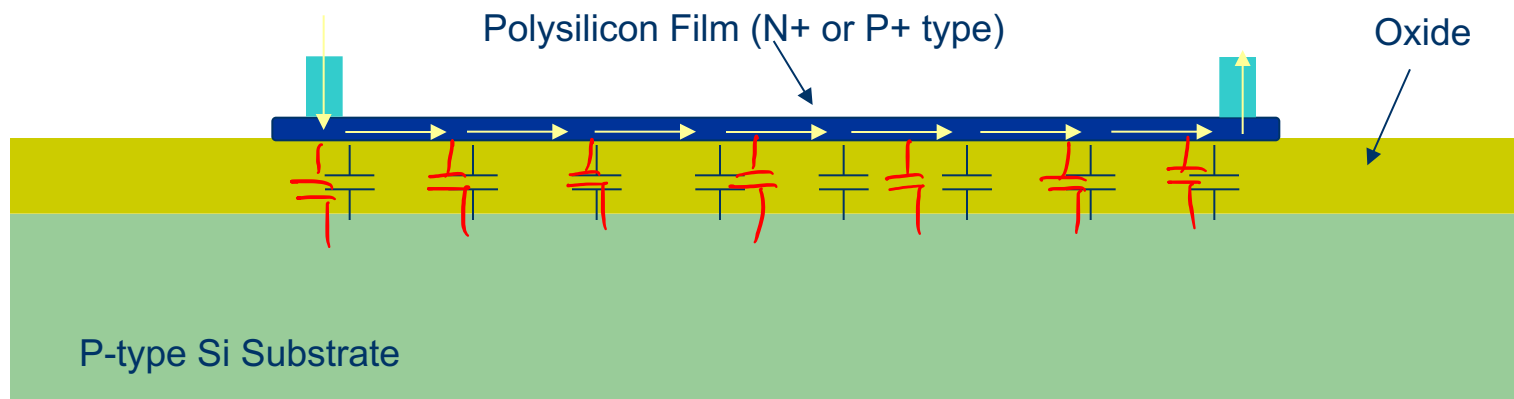
- Si substrate (p-type)
- Grow oxide (thermally)
- Add photoresist
- Expose (visible or UV source)
- Etch (chemical such as HF)
- Ion implantation (inject dopants)
- Diffuse (increase temperature and allow dopants to diffuse)

“Diffusion” Resistor



- Using ion implantation/diffusion, the thickness and dopant concentration of resistor is set by process
- Shape of the resistor is set by design (layout)
- Metal contacts are connected to ends of the resistor
- Resistor is capacitively isolation from substrate
 - Reverse Bias PN Junction!

Poly Film Resistor



- To lower the capacitive parasitics, we should build the resistor further away from substrate
- We can deposit a thin film of “poly” Si (heavily doped) material on top of the oxide
- The poly will have a certain resistance (say 10 Ohms/sq)

Ohm's Law

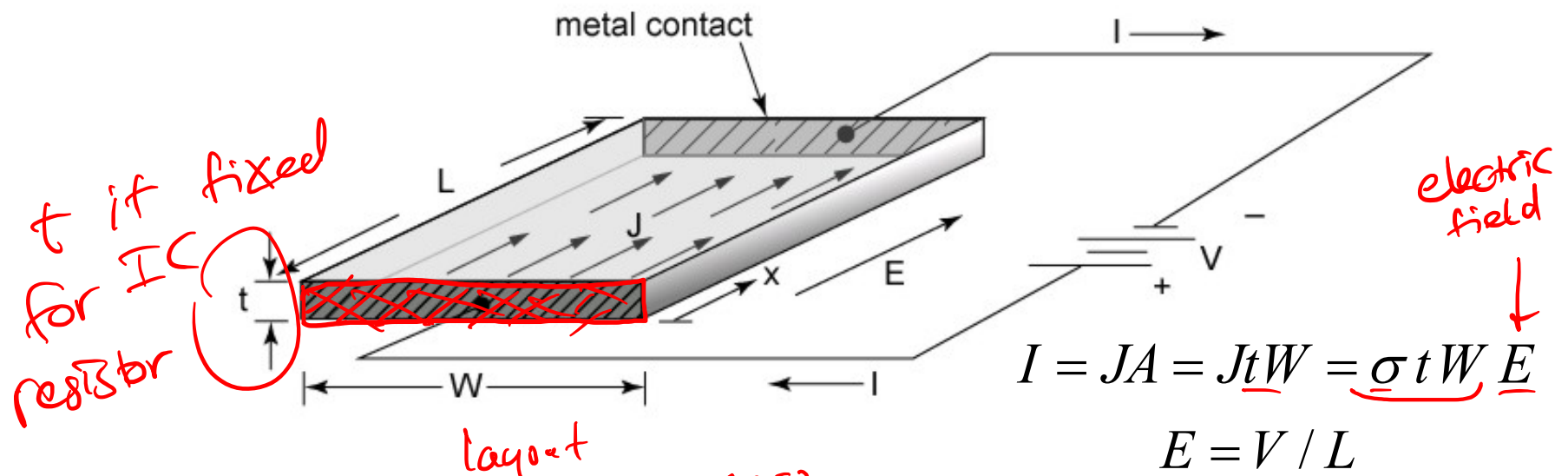
- Current I in terms of J_n
- Voltage V in terms of electric field

$V = IR$

$I = JA = JtW$

current density

$A = t \cdot w$



$I = JA = JtW = \sigma tW E$

$E = V / L$

- Result for R

$\frac{1}{G} = R = \left(\frac{L}{W} \right) \left(\frac{1}{\sigma t} \right)$

$R = \left(\frac{L}{W} \right) \left[\frac{\rho}{t} \right]$

layout

process

R_{\square}

$I = JA = JtW = \frac{\sigma tW}{L} V$

length

G

Sheet Resistance (R_s)

- IC resistors have a specified thickness – not under the control of the *circuit* designer
- Eliminate t by absorbing it into a new parameter: the *sheet resistance* (R_s)

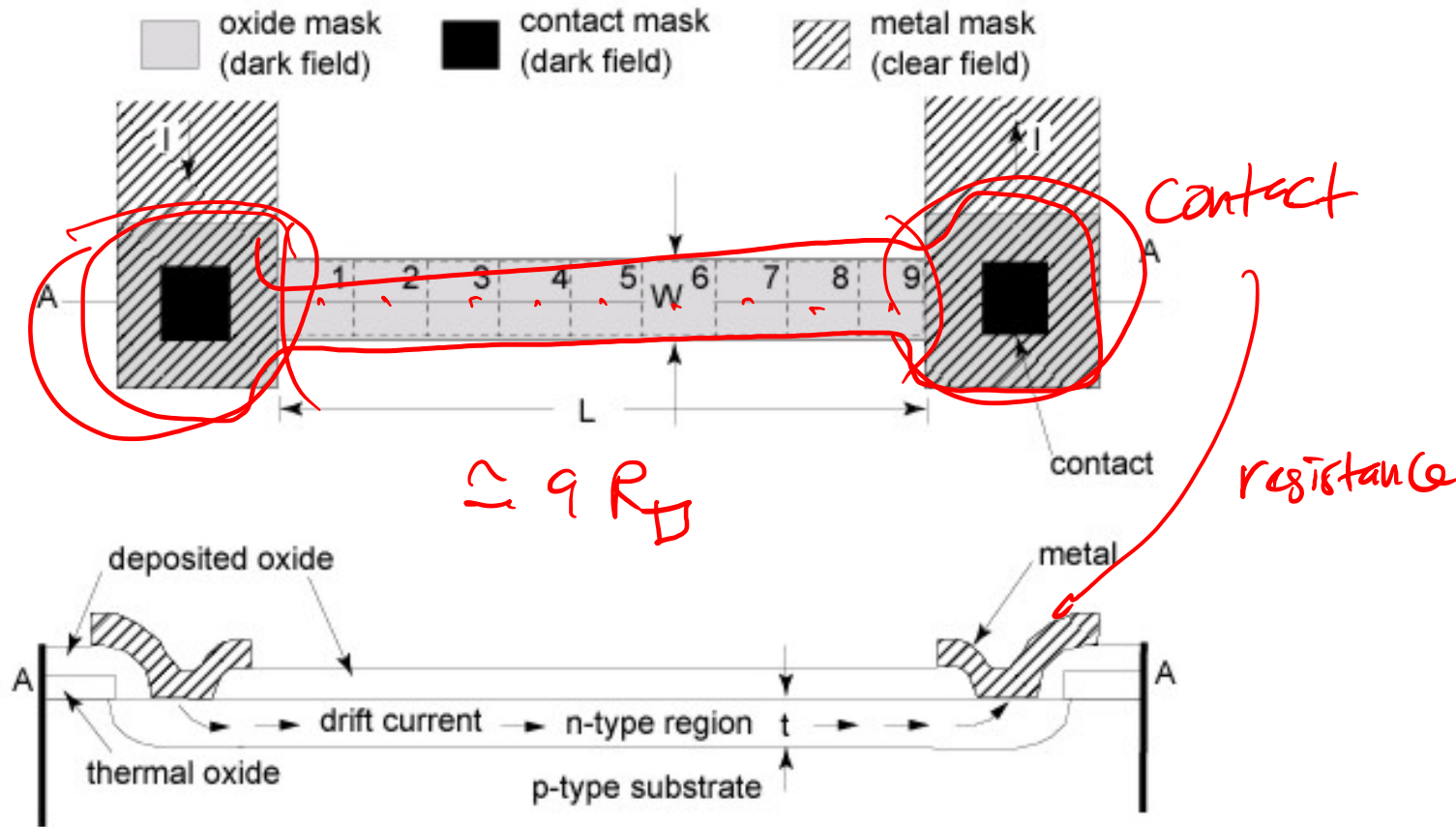
$$R = \frac{\rho L}{Wt} = \left(\frac{\rho}{t} \right) \left(\frac{L}{W} \right) = R_{sq} \left(\frac{L}{W} \right)$$

AKA R_{\square}
 R_s
 (sheet resistance)

↑
 “Number of Squares”

Using Sheet Resistance (R_s)

- Ion-implanted (or “diffused”) IC resistor



Idealizations

- Why does current density J_n “turn”?
- What is the thickness of the resistor?
- What is the effect of the contact regions?

