Module 2.2:
IC Resistors and Capacitors

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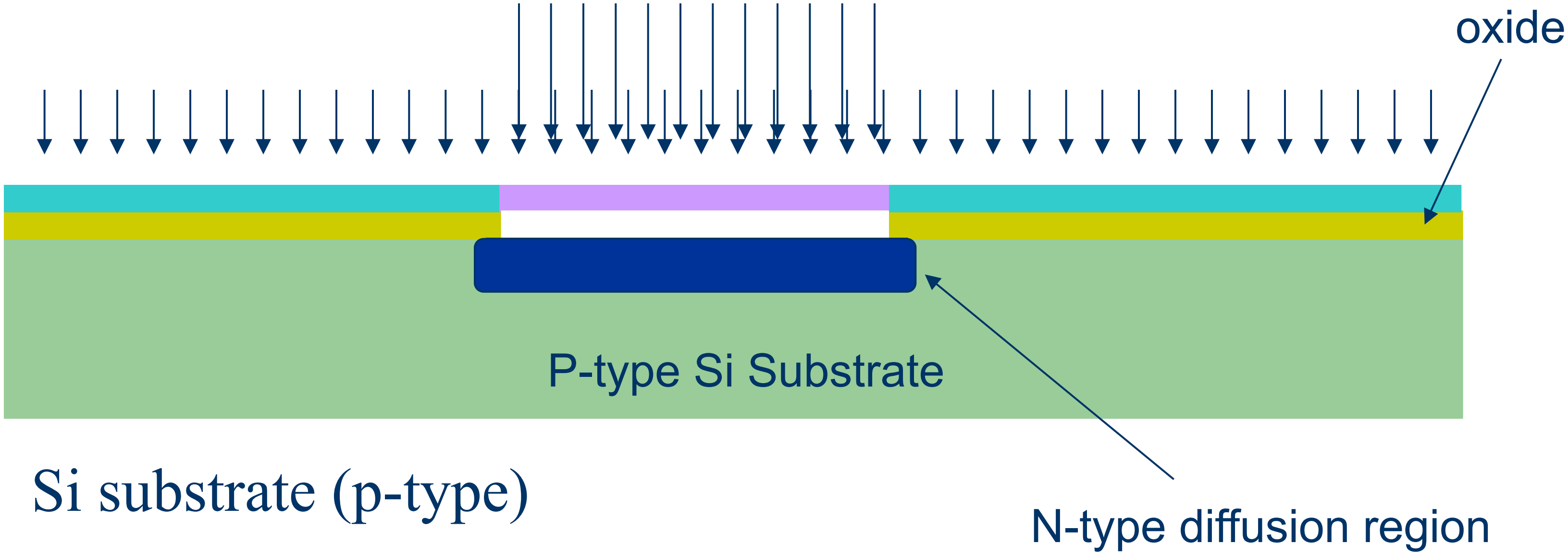
IC Fabrication: Si Substrate

- Pure Si crystal is starting material (wafer)
- The Si wafer is extremely pure (~1 part in a billion impurities)
- Why so pure?
  - Si density is about 5 10^22 atoms/cm^3
  - Desire intentional doping from 10^14 – 10^18
  - Want unintentional dopants to be about 1-2 orders of magnitude less dense ~ 10^12
- Si wafers are polished to about 700 μm thick (mirror finish)
- The Si forms the substrate for the IC

IC Fabrication: Oxide

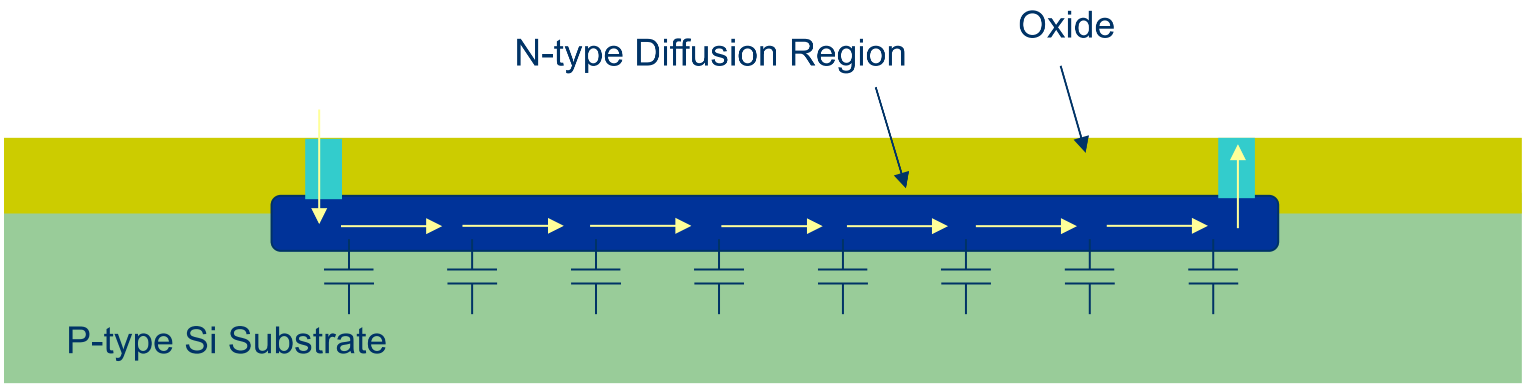
- Si has a native oxide: SiO_2
- SiO_2 (Quartz) is extremely stable and very convenient for fabrication
- It's an insulators so it can be used for house interconnection
- It can also be used for selective doping
- SiO_2 windows are etched using photolithography
- These openings allow ion implantation into selected regions
- SiO_2 can block ion implantation in other areas

IC Fabrication: Ion Implantation



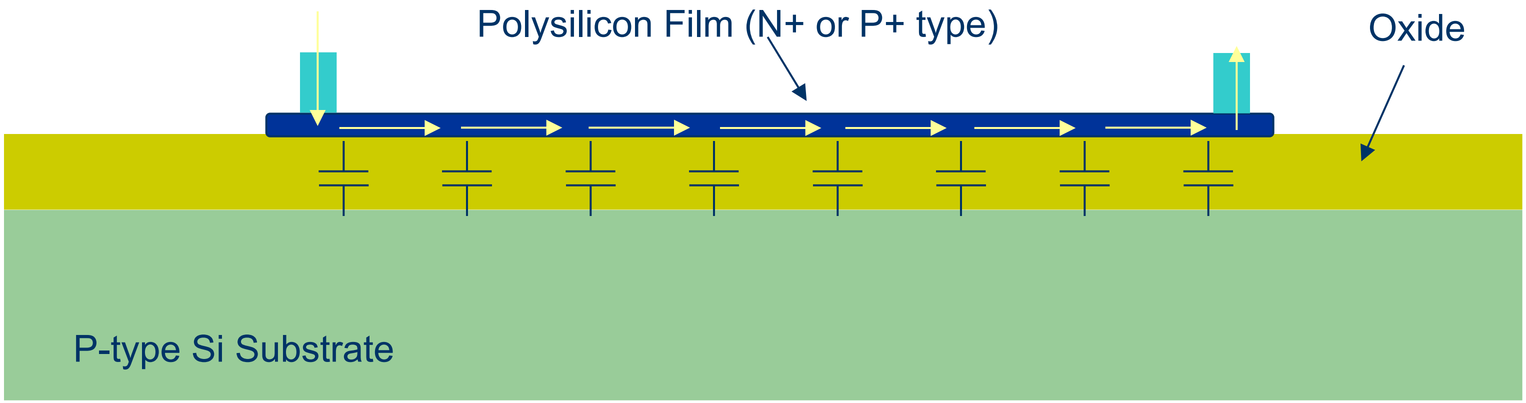
- Si substrate (p-type)
- Grow oxide (thermally)
- Add photoresist
- Expose (visible or UV source)
- Etch (chemical such as HF)
- Ion implantation (inject dopants)
- Diffuse (increase temperature and allow dopants to diffuse)

"Diffusion" Resistor



- Using ion implantation/diffusion, the thickness and dopant concentration of resistor is set by process
- Shape of the resistor is set by design (layout)
- Metal contacts are connected to ends of the resistor
- Resistor is capacitively isolation from substrate
  - Reverse Bias PN Junction!

Poly Film Resistor



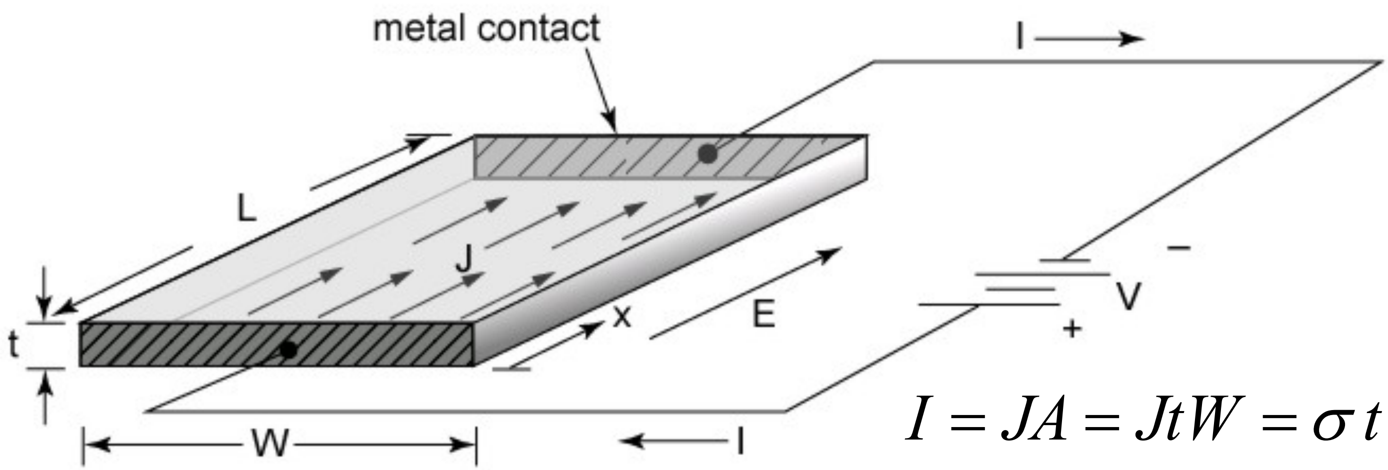
- To lower the capacitive parasitics, we should build the resistor further away from substrate
- We can deposit a thin film of "poly" Si (heavily doped) material on top of the oxide
- The poly will have a certain resistance (say 10 Ohms/sq)

Ohm's Law

- Current I in terms of J_n
- Voltage V in terms of electric field

$$V = IR$$

$$I = JA = JtW$$



$$I = JA = JtW = \sigma t W E$$

$$E = V / L$$

$$I = JA = JtW = \frac{\sigma t W}{L} V$$

– Result for R

$$R = \frac{L}{W} \frac{1}{\sigma t} \qquad R = \frac{L}{W} \frac{\rho}{t}$$

Sheet Resistance (R_s)

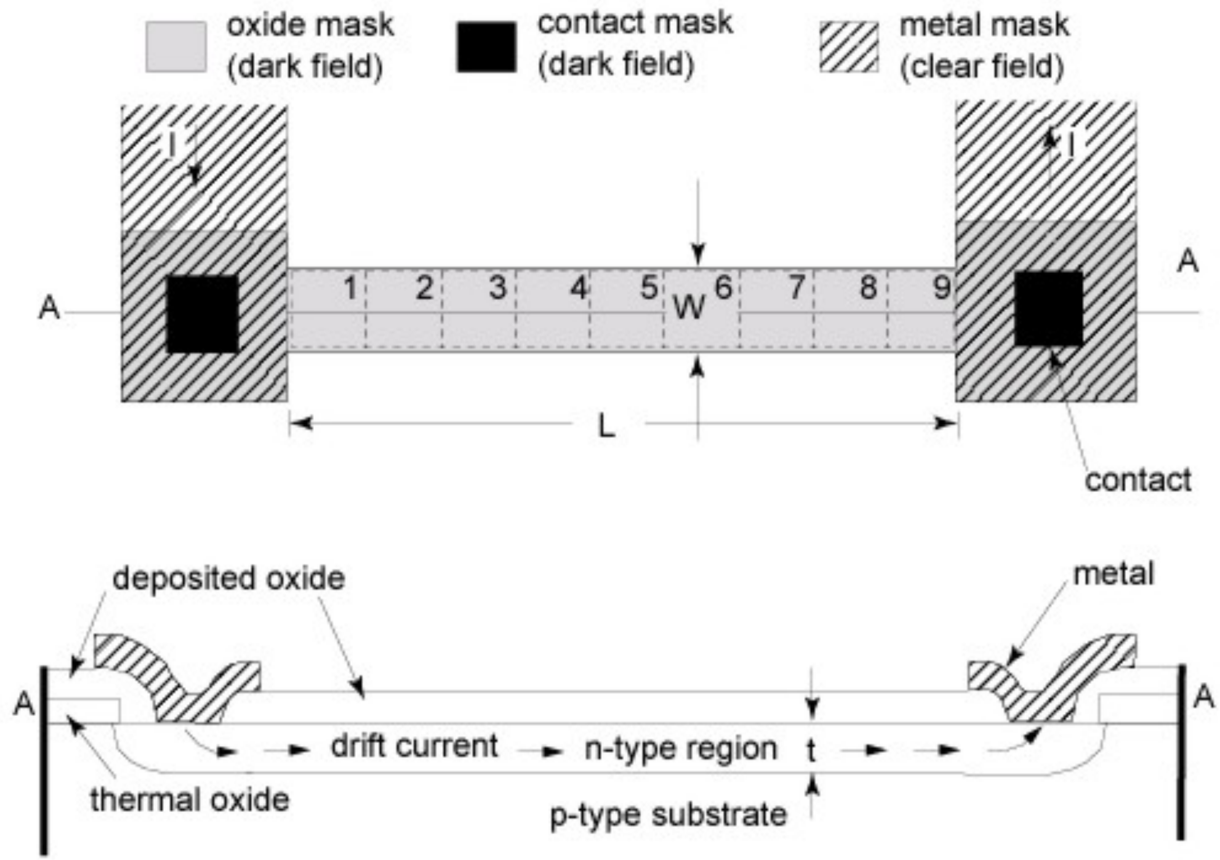
- IC resistors have a specified thickness – not under the control of the *circuit* designer
- Eliminate t by absorbing it into a new parameter: the *sheet resistance* (R_s)

$$R = \frac{\rho L}{Wt} = \left(\frac{\rho}{t}\right)\left(\frac{L}{W}\right) = R_{sq}\left(\frac{L}{W}\right)$$

"Number of Squares"

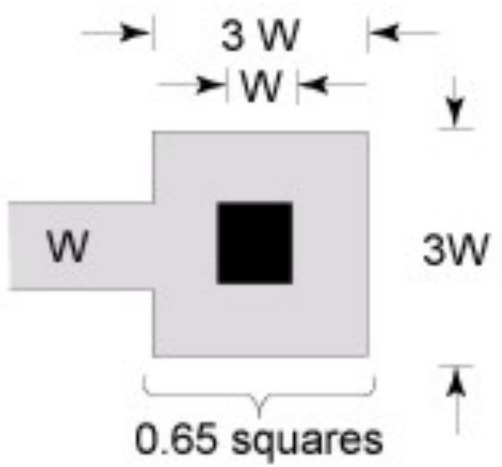
Using Sheet Resistance (R_s)

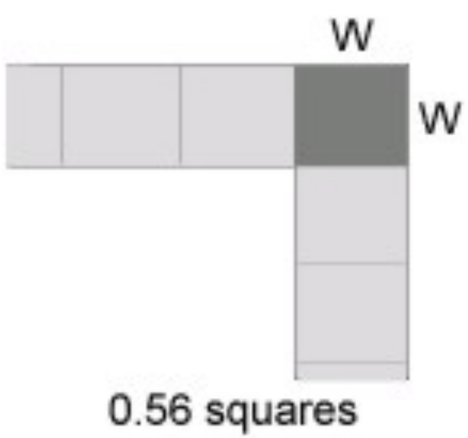
- Ion-implanted (or “diffused”) IC resistor



Idealizations

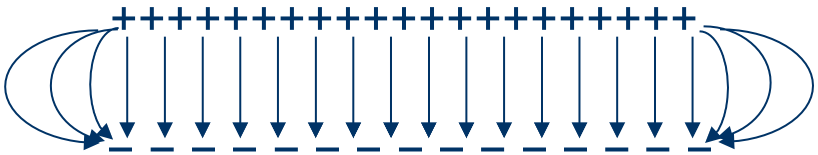
- Why does current density J_n "turn"?
- What is the thickness of the resistor?
- What is the effect of the contact regions?





Electrostatics Review (1)

- Electric field go from positive charge to negative charge (by convention)



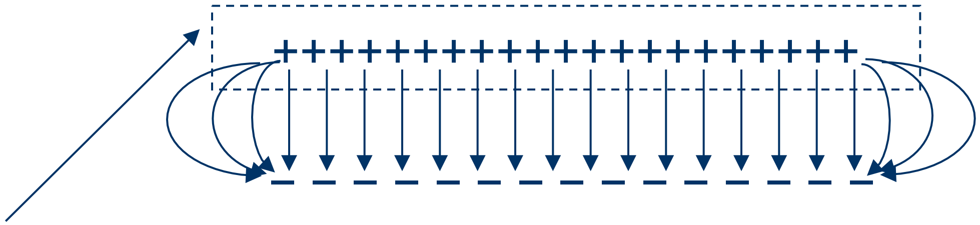
- Electric field lines *diverge* on charge

$$\nabla \cdot E = \frac{\rho}{\varepsilon}$$

- In words, if the electric field changes magnitude, there has to be charge involved!
- Result: In a charge free region, the electric field must be constant!

Electrostatics Review (2)

- Gauss' Law equivalently says that if there is a *net* electric field leaving a region, there has to be positive charge in that region:



Electric Fields are Leaving This Box!

$$\oint E \cdot dS = \frac{Q}{\varepsilon}$$

Recall:

$$\oint_V \nabla \cdot E \, dV = \oint_V \frac{\rho}{\varepsilon} dV = Q / \varepsilon \longrightarrow \oint_V \nabla \cdot E \, dV = \oint_S E \cdot dS = \frac{Q}{\varepsilon}$$

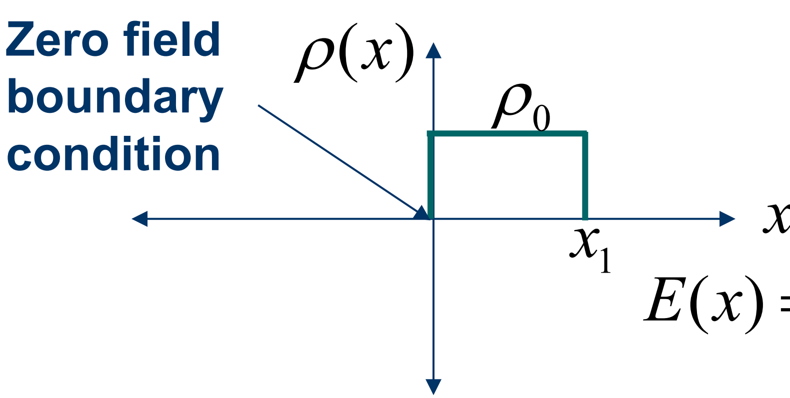
Electrostatics in 1D

- Everything simplifies in 1-D

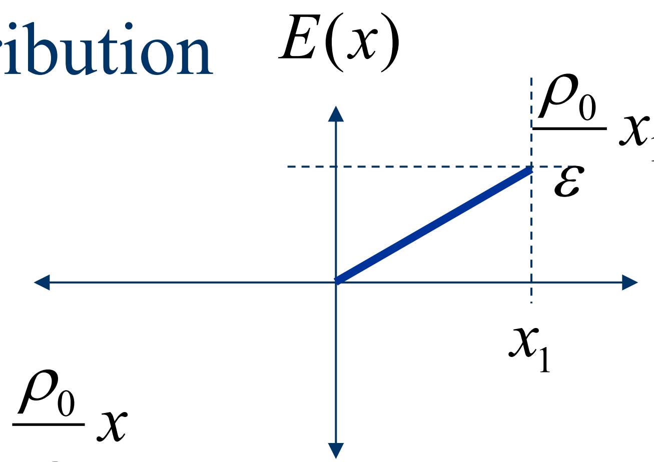
$$\nabla \cdot E = \frac{dE}{dx} = \frac{\rho}{\varepsilon} \qquad\qquad dE = \frac{\rho}{\varepsilon}dx$$

$$E(x) = E(x_0) + \int_{x_0}^{x} \frac{\rho(x')}{\varepsilon}dx'$$

- Consider a uniform charge distribution



$$E(x) = \int_{0}^{x} \frac{\rho(x')}{\varepsilon}dx' = \frac{\rho_0}{\varepsilon}x$$



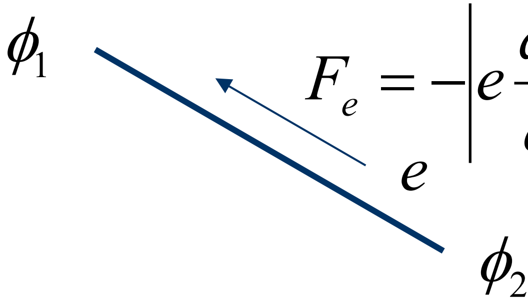
Electrostatic Potential

- The electric field (force) is related to the potential (energy):

$$E = -\frac{d\phi}{dx}$$

- Negative sign says that field lines go from high potential points to lower potential points (negative slope)
- Note: An electron should “float” to a high potential point:

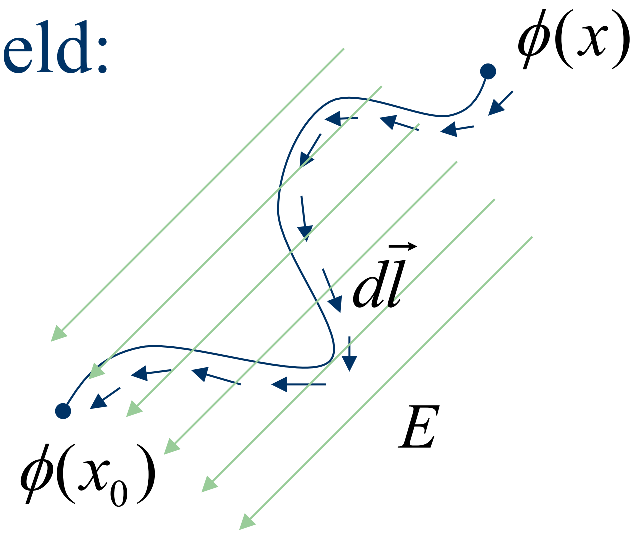
$$F_e = qE = -e\frac{d\phi}{dx}$$



$$F_e = -\left| e\frac{d\phi}{dx} \right|$$

More Potential

- Integrating this basic relation, we have that the potential is the integral of the field:



$$\phi(x)-\phi(x_0)=-\int_C E\cdot d\vec{l}$$

- In 1D, this is a simple integral:

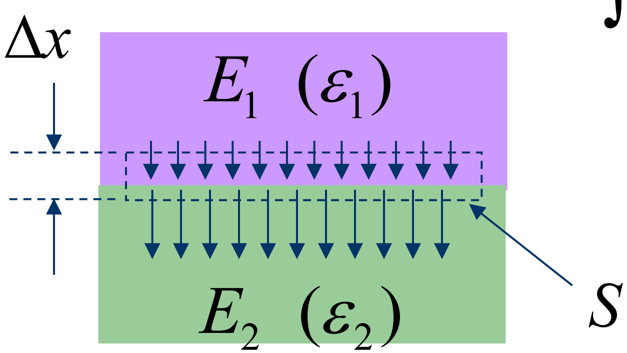
$$\phi(x)-\phi(x_0)=-\int_{x_0}^{x} E(x')dx'$$

- Going the other way, we have Poisson's equation in 1D:

$$\frac{d^2\phi(x)}{dx^2}=-\frac{\rho(x)}{\varepsilon}$$

Boundary Conditions

- Potential must be a continuous function. If not, the fields (forces) would be infinite
- Electric fields need not be continuous. We have already seen that the electric fields diverge on charges. In fact, across an interface we have:



$$\oint \varepsilon E \cdot dS = -\varepsilon_1 E_1 S + \varepsilon_2 E_2 S = Q_{inside}$$

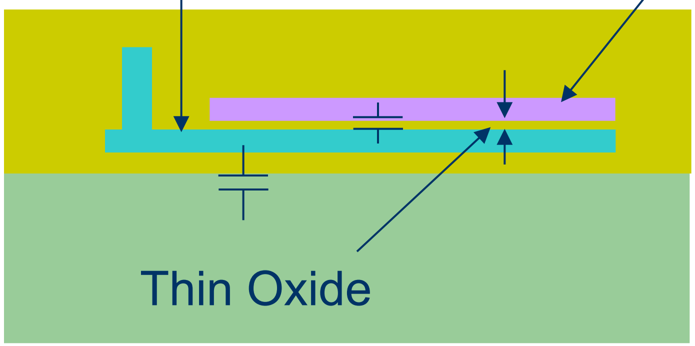
$$Q_{inside} \xrightarrow[\Delta x \to 0]{} 0$$

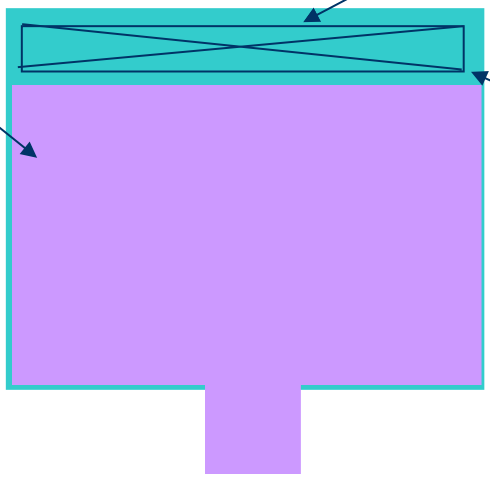
$$-\varepsilon_1 E_1 S + \varepsilon_2 E_2 S = 0$$

$$\frac{E_1}{E_2} = \frac{\varepsilon_2}{\varepsilon_1}$$

- Field discontiuity implies charge density at surface!

IC MIM Capacitor

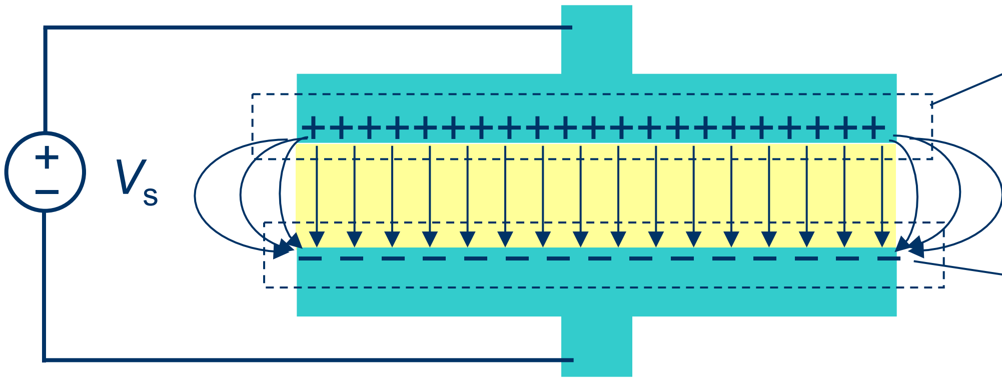




$$Q = CV$$

- By forming a thin oxide and metal (or polysilicon) plates, a capacitor is formed
- Contacts are made to top and bottom plate
- Parasitic capacitance exists between bottom plate and substrate

Review of Capacitors



$$\oint E \cdot dS = \frac{Q}{\varepsilon}$$

$$\oint E \cdot dS = -\frac{Q}{\varepsilon}$$

$$\int E \cdot dl = E_0 t_{ox} = V_s \longrightarrow E_0 = \frac{V_s}{t_{ox}}$$

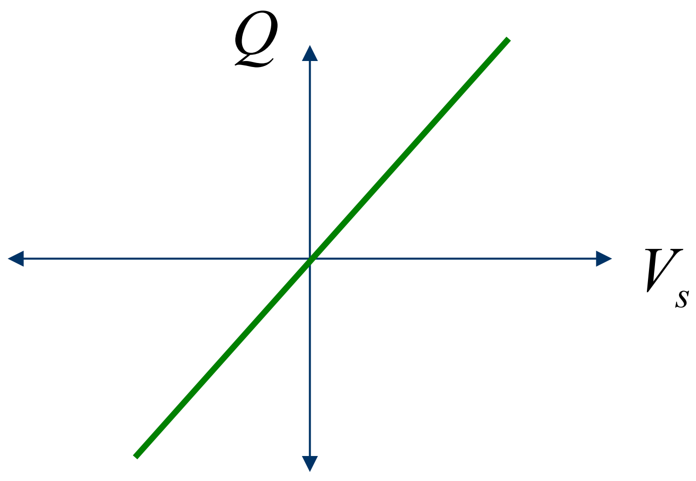
$$\oint E \cdot dS = E_0 A = \frac{Q}{\varepsilon} \longrightarrow \frac{V_s}{t_{ox}} A = \frac{Q}{\varepsilon}$$

$$Q = CV_s$$

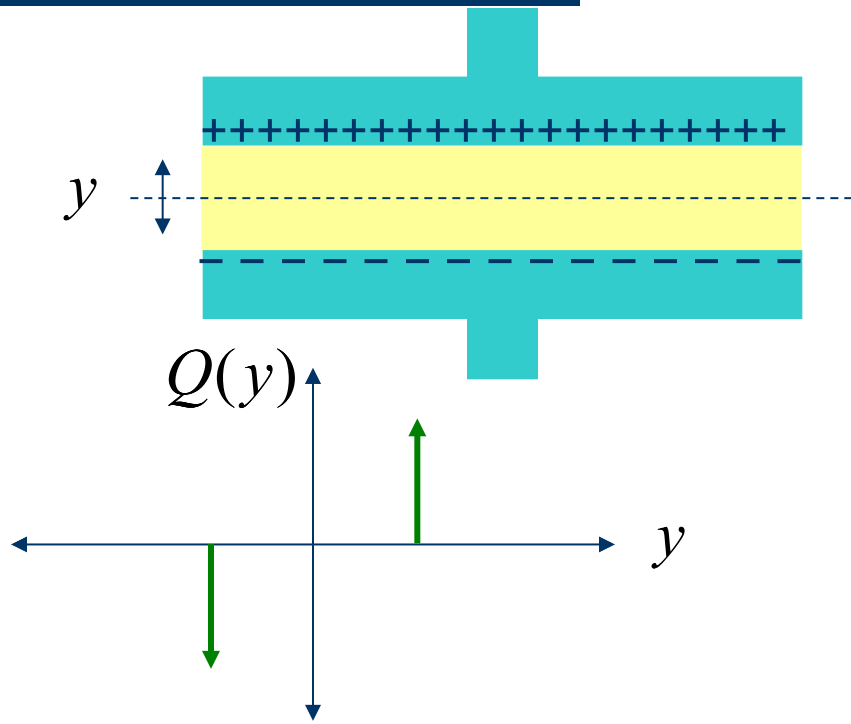
$$C = \frac{A\varepsilon}{t_{ox}}$$

- For an ideal metal, all charge must be at surface
- Gauss' law: Surface integral of electric field over closed surface equals charge inside volume

Capacitor Q-V Relation

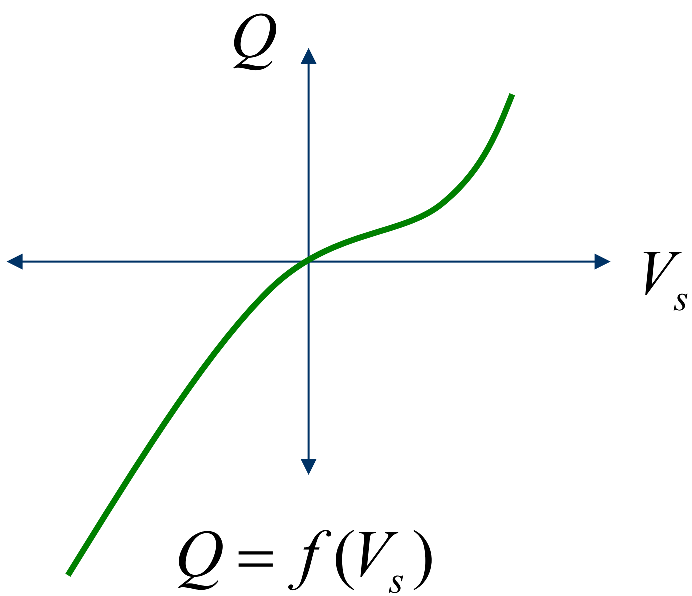


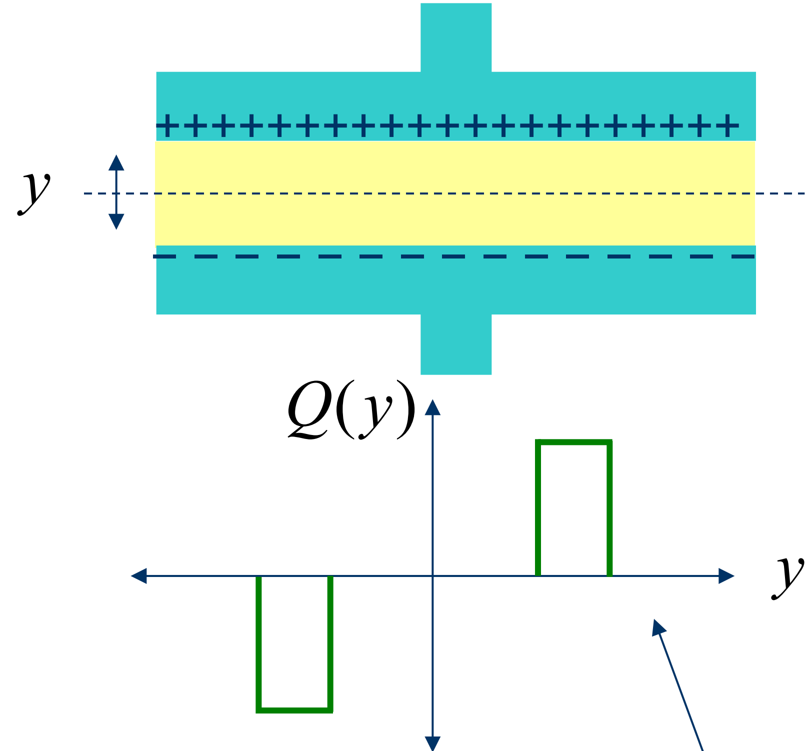
$$Q = CV_s$$



- *Total* charge is linearly related to voltage
- Charge density is a delta function at surface (for perfect metals)

A Non-Linear Capacitor





- We'll soon meet capacitors that have a non-linear Q-V relationship
- If plates are not ideal metal, the charge density can penetrate into surface

What's the Capacitance?

- For a non-linear capacitor, we have

$$Q = f(V_s) \neq CV_s$$

- We can't identify a capacitance
- Imagine we apply a small signal on top of a bias voltage:

$$Q = f(V_s + v_s) \approx f(V_s) + \left.\frac{df(V)}{dV}\right|_{V=V_s} v_s$$

Constant charge

- The incremental charge is therefore:

$$Q = Q_0 + q \approx f(V_s) + \left.\frac{df(V)}{dV}\right|_{V=V_s} v_s$$

Small Signal Capacitance

- Break the equation for total charge into two terms:

Incremental Charge

$$Q = Q_0 + q \approx f(V_s) + \left.\frac{df(V)}{dV}\right|_{V=V_s} v_s$$

Constant Charge

$$q = \left.\frac{df(V)}{dV}\right|_{V=V_s} v_s = C\, v_s$$

$$C \equiv \left.\frac{df(V)}{dV}\right|_{V=V_s}$$

Example of Non-Linear Capacitor

- We'll see that for a PN junction, the charge is a function of the reverse bias:

$$Q_j(V) = -\underbrace{qN_a x_p}_{\text{Constants}} \sqrt{1 - \frac{V}{\phi_b}}$$

Charge At N Side of Junction

Constants

Voltage Across NP Junction

- Small signal capacitance:

$$C_j(V) = \frac{dQ_j}{dV} = \frac{qN_a x_p}{2\phi_b} \frac{1}{\sqrt{1 - \frac{V}{\phi_b}}} = \frac{C_{j0}}{\sqrt{1 - \frac{V}{\phi_b}}}$$