Mixed Signal Techniques for RF Transceivers

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Outline

• RF Receivers: A Mixed-Signal Perspective
• Discrete-Time RF Receivers
• Sigma-Delta A/D Converters
  – Intro to Sigma-Delta Modulation
  – Sigma-Delta Converters in RF Receivers
• Mixed-Signal Techniques in RF Transmitter
Wireless Communication System

Retrieve original information

Challenge:
• Maintaining SNR
• Large blocker signals

A Direct-Conversion Receiver

- **Mix – Amplify – Filter** → A/D Conversion

- Virtually all RF receiver today has an A/D
  - Complex modulation schemes to achieve spectral efficiency
  - Needs digital circuit to perform complex demodulation algorithm
RF Receiver: A Mixed-Signal Perspective

- A receiver **pre-conditions** an RF signal for A/D conversion

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Deriving Requirements

- System specifications for receiver is derived from the **blocking mask** and the choice of **A/D converters**
UMTS Blocker Mask

GSM Blocker Mask
Narrow-band signals

GSM 900 Blocking Profile
A/D Converters Specifications

Sufficient Condition

- **Nyquist Criterion**
  - $F_s = 2RF_{BW}$
  - Doesn’t have to be at DC!
    (Beware of noise folding)

- **Dynamic-range budgeting**
  - $SNR_{\text{min}}$ for successful decoding
  - Peak-to-average power ratio
  - Margin for other ‘stuff’
    (intermods, leftover blocker signals, etc)

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A/D Converters Specifications

The Full Picture

- Desired signal is not in isolation
- Blocker signals will fold down due to a sampling operation (aliasing)
- Adjacent channels are especially hard to filter out
A/D Converters Specifications

Increasing Sampling Rate

- Blocker B is no longer aliased
- Dynamic-range margin is allocated for blocker power, not for desired signal

A/D Converters Specifications

- Multiple stages of filters are needed in an RF receiver to eliminate aliases
- Increase A/D sampling-rate:
  - Relax anti-aliasing filter requirements
  - Potentially an increase in A/D dynamic-range
  - Increase in A/D power consumption
A/D FOM Survey

- What is achievable?
- 1ps(RMS) jitter seems to be the empirical limit
- 10x power for 20dB improvement in SNDR
- Trend deviate for high-res converters

Pre-condition RF Signals: Summary

- Blockers are **BAD**:  
  - Large magnitude will saturate circuits  
  - It will alias down within A/D converter

- Role of baseband filters:  
  - Limit dynamic range, filter out large blockers  
    - Make life easier for succeeding blocks  
  - It serves as an **anti-alias filter** for the A/D

- Better A/D → Less filter stages  
  - Power optimization between filters and A/D
Example: CDMA Baseband Filter

![Graph of response vs frequency for a CDMA Baseband Filter](V. Aparin, ISSCC 2005)

CDMA BB Filter: Implementation

![Diagram of CDMA BB Filter implementation](V. Aparin, ISSCC 2005)
CDMA BB Filter: Mixer + 1 pole

GSM BB Filter
Discrete-Time Filters

- **Advantages**
  - Well-defined corner frequencies (Cap matching)
  - Corner frequencies are tunable (switch in/out caps)
  - Superior linearity

- **Disadvantages**
  - Sampled-data system → Aliasing
  - Operating speed is limited by OTA settling
  - Power consumption
Sampling Mixer

Single-balanced mixer with capacitive load

\[ v_{\text{out}}[n] = \frac{q_{\text{in}}[n]}{C_H} + v_{\text{out}}[n-1] \]

\[ q_{\text{in}}[n] = G_m \cdot \int_{nT_{\text{LO}}}^{nT_{\text{LO}}+\frac{2\Delta \omega}{n}} V_{R_f}(\tau) \cdot d\tau \]
Sampling Mixer: Recap

- **Output of a mixer is *discrete-time***
  - Needs to evaluate at the right time-instants
  - Slightly more complicated for double-balanced

- **Mixer is a *sampler***
  - Aliasing still happens with period of $f_{LO}$
  - Nulls on even harmonics due to nature of windowed-sampling
  - No need for another sample-and-hold amplifiers!
### Lossy Integrator

**Well-controlled corner frequency**

\[ q_H[n] = \alpha \cdot q_H[n-1] + q_{in}[n] \]

\[ \frac{Q_H(z)}{Q_{in}(z)} = \frac{1}{1 - \alpha z^{-1}} \]

\[ \alpha = \frac{C_H}{C_H + C_R} \]

\( \alpha \) controls corner-frequency

\[ G_c = \frac{\frac{C_m T_{LO}}{2}}{V_{in} = 2 \text{conv. gain at DC}} \cdot \frac{\pi}{2} \cdot \frac{1}{1 - \alpha_1} \cdot \frac{1}{C_m} \]

### Higher-Order IIR Filtering

\[ \alpha = \frac{C_H}{C_H + C_R} \]

\[ \beta = \frac{C_R}{C_H + C_R} = 1 - \alpha \]

\[ \frac{1}{1 - \alpha_1 z^{-1}} \]
Sample-Rate Down-conversion

\[ V_{\text{HR}}(t) \rightarrow G_{\text{HR}} \]

\[ \frac{1+z^{-1}}{1+\alpha z^{-1}} \]

Moving-Average Filters

‘Ideal’ Anti-alias filtering

Downsample-by-four

FIR: \( H(z) = 0.25[1+z^{-1}+z^2+z^{-3}] \)

Nulls exactly at potential aliases (assuming narrow-band signals)
Sample-Rate Down-conversion (2)

Discrete-Time Filter in RF Rx: Summary

- **Mixer = Sample-and-Hold**
  - Main reason this technique makes sense in RF Rx

- **Moving-average filter**
  - Exactly what is needed prior to sample-rate reduction

- **Passive switched-capacitor circuits**
  - No limitation on OTA BW

- **Retain all the advantage of SC filters**
  - Limited pole placement due to passive nature
  - Good for low-pass filters, not for band-pass filters
TI DRP – Discrete-Time Rx

MA Filter

1st Integrator

2nd Integrator

Downsample by 8

Feedback (cancellation):
- DC offset
- IM2

R.B. Staszewski, JSSC Dec 2004
UCLA Software-Defined Rx

- Same idea: Use moving-average sampler as anti-alias filter prior to downsampling
- Need higher rejection on MA filter nulls
  - Use a triangle window, instead of a rectangular
  - Sinc² frequency response

R. Bagheri, ISSCC 2006

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UCLA Software-Defined Rx

R. Bagheri, ISSCC 2006
A/D Selection for RF Receivers

- Sufficient conditions
  - Nyquist → fs = 2xBW
  - DR = SNR_{min} + PAR + \textit{margin}

- Use higher sampling-rate A/D
  - Less aliasing, treat blockers as signal
  - Allocate \textit{margin} for blockers

- Focus today: \(\Sigma\Delta\) A/D converter
  - High sampling-rate
  - High dynamic-range (where it matters)

ADC Resolution vs. Speed

B. Kim, ISSCC 2006
Why $\Sigma \Delta$ A/D Converters in RF Receivers

- ‘Free’ anti-alias filtering
  - Actually blockers are filtered in the digital domain
- High resolution possible with low-resolution components
- Very good power efficiency (FOM)

A $\Delta \Sigma$ ADC System

- The $\Delta \Sigma$ modulator encodes (modulates) its input in such a way that the quantization noise present in the output is *shaped*
- The decimation filter removes this noise
In general, filters in the $\Sigma\Delta$ loop shape *quantization noise*, not the signal.
**ΣΔ A/D Converters in an RF Receiver**

- A sigma-delta A/D is well-suited for an RF receiver:
  - **Oversampling** reduces aliasing
  - Low quantization noise only around signal of interest

**Arbitrary Signal Bandwidth**

- Signal bandwidth is never explicitly defined in the analog domain
  - Large bandwidth $\rightarrow$ more quantization noise
- Final signal selection is performed in the digital domain
  - Digital filters are cheap and easily reprogrammable
ΣΔ #1: ΣΔ A/D for GSM/WCDMA

- Second-order CT SD
- Low power, small area
- Reconfigurable between GSM/WCDMA by changing clock-rate
- Most of DR is allocated for blockers

M. Vaidpour, VLSI 2008

ΣΔ #2: Bandpass ΣΔ A/D

90dB @ 50mW, 333kHz BW, 10-300MHz f_input

R. Schreier, ISSCC 2002
### ΣΔ #3: Pipelined A/D Replacement

- Integrated PLL for low jitter
- 20MHz BW, 76 dB DR
  - 122 fJ/conv.step (w/o PLL)
  - 354 fJ/conv.step (w. PLL)
- Performance on par with state-of-art pipelined A/D converter
  - Anti-aliasing is free

![Diagram](image.png)

G. Mitteregger, ISCC December 2006

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### ΣΔ-Based Receiver Architecture

- It’s an RF-to-digital converter
- Direct-conversion mixer
- Sample the output of mixer at f_{LO}
  - No aliasing
  - Very high oversampling ratio (OSR)
- Simple loop filter:
  - Only MOS switches, no linear amplifiers

![Diagram](image2.png)
Second Order $\Sigma\Delta$ Modulator

- Passive, switched-capacitor loop-filter, feedback-compensated modulator
- A 1-bit quantizer and DAC is used to ensure excellent linearity


ΣΔ Modulator Design

$C_{H1} = 10 \text{ pF}$
$C_{H2} = 10 \text{ pF}$
$C_R = 100 \text{ fF}$
$f_{LO} = 2 \text{ GHz}$

STF is flat across the band by design

<table>
<thead>
<tr>
<th>Bandwidth (MHz)</th>
<th>SNR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>84</td>
</tr>
<tr>
<td>4</td>
<td>80</td>
</tr>
<tr>
<td>8</td>
<td>74</td>
</tr>
<tr>
<td>20</td>
<td>61</td>
</tr>
</tbody>
</table>
GM Design: Minimizing Distortion

- Input-limited
  - Distortion due to V-to-I conversion
- Output-limited
  - Distortion due to excessive voltage swing
- Bias-point optimization

\[ \Sigma \Delta \text{FB} + \text{output load impedance} \]

\[ \Sigma \Delta \text{A/D: Summary} \]

- **Oversampling**
  - Spreads quantization noise over wider bandwidth
  - Less aliasing
- **Quantization-Noise Shaping**
  - Push quantization noise away from desired BW
  - High SNR only around a narrow BW

- Enclose filters within an A→D→A feedback loop
  - Contrast with filters followed by an A/D
  - Process error signal (<< than desired signal)
Main idea: Replace PAs with DACs
- Power efficiency (switching PAs)
- Digital pre-distortion, correction, calibration, etc...

Problems:
- High-speed, high-resolution
- Reconstruction filter

Techniques
- Sigma-Delta
- Polar Modulation

A ΔΣ DAC System

Mathematically similar to an ADC system
The modulator is digital and drives a low-resolution DAC, whose output is then filtered by an analog filter to attenuate the out-of-band noise. We will concentrate on ADCs.
RF DACs

- Cartesian $\rightarrow$ Polar
  - Phase-modulation in PLL
  - Amplitude-modulation in PA
- Use $\Sigma\Delta$ modulation to get good linearity out of small numbers of large switching elements
- Use matching network as reconstruction filter

J. Stauth, CICC 2008

TI DRP: All-Digital PLL

In 130nm, min gate cap is $\sim 38$ aF $\approx 23$kHz @ 2.4GHz

Use $\Sigma\Delta$ for finer resolution

R.B. Staszewski, ISSCC 2005
TI DRP: ‘Digital’ PA

The DPA can be thought of as an RF DAC, where “A” is RF “amplitude”

6-bit (64x) resolution + 8-bit ΣΔ dithering

R.B. Staszewski, ISSCC 2005

All-Digital TX

Digital corrections

R.B. Staszewski, ISSCC 2005
Summary

• Boundary between ‘RF’ and ‘Mixed-signal’ is diminishing in RF Transceiver design (0-5GHz)

• Lots of system optimization ‘tricks’ that uses a combination of RF and mixed-signal techniques
  – Transceiver design is no longer: RF designer + baseband designer + A/D designer

• Trend towards digital closer to the antenna

Extra Slides
RF DACs

S. Luschas, JSSC, Sept 2004

ΣΔ #4: ΣΔ A/D for UMTS

Feedforward Compensation

70dB @ 3.3mW, 2MHz BW

R. Schreier, ISSCC 2002