Problem Set 5
Due Friday Nov. 28, 2014

For simulations, use the transistor model card from the PTM 65nm node (http://ptm.asu.edu/latest.html). In particular, use the BSIM4 model cards released on Feb. 22, 2006 (http://ptm.asu.edu/modelcard/2006/65nm_bulk.pm).

1. Design a power amplifier with a gain of 10 dB to deliver 500mW biased in Class A and Class AB mode. Plot the efficiency and output power versus the input power. Plot the DC current versus input power in both cases. What is the linearity at 1-dB gain compression?

2. Design a Class C amplifier meeting the same specs and plot the same data.

3. Add a matching second stage to increase the gain to 20 dB for your Class AB design.

4. Now design a switching power amplifier class (Class D, D^-1, E/F, S, or other) to deliver 500mW meeting the same gain spec. How much better is the efficiency?

5. Devise a scheme to introduce amplitude modulation for your switching power amplifier. Try envelope modulation or another scheme. You may use an ideal voltage or current source to simplify this test. For a two-tone modulation, what is the IM3 you can achieve with this scheme for peak power (or a small back-off such as 1-dB).