An SDR Front-End Receiver
242B Class Project
Version: 9/4/2014

Background

A Software Defined Radio (SDR) is a universal radio that can operate in any frequency band using any modulation scheme. One way to build such a radio is to connect an analog-to-digital converter (ADC) to an antenna and clock it at twice the highest frequency of interest. For example, to receive all signals from DC to 5 GHz, an ADC clocked at 10 GHz would do the job. In practice this is impractical because the signals appearing at the input of the ADC would cover a very large dynamic range, from about -100 dBm (the desired sensitivity of the receiver) to about 0 dBm, a strong signal picked up from a nearby transmitter. 100 dB of dynamic range would require an effective resolution of about 17-bits. (Even if it were feasible to build such a ADC, this translates into a power consumption of about 600W, calculated from a FOM = 459 fJ/conv step for the best published 10 GHz ADC.)

One way to relax the dynamic range of the ADC is to insert an LNA/mixer pair to down-convert the input spectrum into an IF frequency that is more amenable to sampling. For example, if the highest signal bandwidth is 100 MHz, then we can do a direct conversion receiver with a bandwidth of 100 MHz. The trouble is that even in a 100 MHz bandwidth, we still must contend with the same dynamic range, but at least the sampling frequency has been reduced to 200 MHz. To alleviate the dynamic range, a programmable filter could knock off the largest interfering signals by programming the bandwidth of the filter to attenuate all of the out-of-channel signals, but this is not an SDR but rather a traditional radio.

Another option is to put a programmable gain amplifier behind the mixer so that a given reduced dynamic range for the ADC, say 70-dB, can be moved up and down to cover the entire 100-dB. In this scenario, a weak signal of -100 dBm would still be recovered but the maximum signal would be limited to -30 dBm. If a 0 dBm blocker is present, the sensitivity increases to -70 dBm. A 70-dB dynamic range ADC with a sampling frequency of 200 MHz can be realized in modern technology.

Project Specifications

Your goal is to design an I/Q LNA/mixer that covers the RF bandwidth from 600 MHz to 6 GHz (most modern mobile bands plus WiFi), and has an IF bandwidth of 80 MHz. Assume an ideal baseband PGA can be programmed with a voltage gain that varies from 0-dB to 30-dB in 1-dB steps. The PGA presents an input capacitance of 200fF that you must drive. The PGA has a noise figure of 25 dB measured in a 50 ohm system.
Your front-end should be capable of receiving a signal as weak as -100 dBm with an SNR = 8 dB when the IF bandwidth is reduced to 1 MHz and other signals in the band are no larger than -40 dBm. Note that the IF bandwidth is reduced digitally using digital signal processing. Your goal is to ensure that the noise floor of your system meets these specifications. If you prefer, you may use a non-zero IF frequency (to avoid flicker noise), but then you must provide for image rejection. Keep in mind that if your system is zero-IF, you should simulate the DSB NF, whereas the SSB NF applies for a non-zero IF. In any given scenario, the effective SNR (due to noise or distortion) should be at least 8 dB.

Your receiver should also be capable of working with a signal as weak as -70 dBm when accompanied by strong jammer of 0-dBm within the same 80 MHz bandwidth. In any given scenario, the effective SNR (due to noise or distortion) should be at least 8 dB.

Your mixer should be fully differential, but the LNA can be single-ended, differential, or balanced. If you opt for a balanced or differential topology, assume the balun has a loss of 2-dB to interface with the antenna. Make sure you account for this loss in your sensitivity calculations.

You may use inductors in your design with a Q < 10, and ideal capacitors and resistors. For simplicity you can assume that your components match perfectly, so ignore IP2 specifications. Matching is also important for image rejection, but for simplicity we’ll assume you can tune the image rejection to provide the needed balance. In reality, a good image rejection scheme is very challenging.

For your mixers, be sure to design an LO buffer, as the LO signal is a differential voltage of fixed amplitude 100mV, and it can only drive 10 fF of capacitance.

**Technology**

If you have access to a commercial foundry with a 65nm node, please use that technology. Otherwise use the PTM 65nm node (http://ptm.asu.edu/latest.html). Use the BSIM4 model cards released on Feb. 22, 2006 (http://ptm.asu.edu/modelcard/2006/65nm_bulk.pm).

Your supply voltage is limited to 1.2V.

**Project Goals**

Minimize power consumption first and foremost, and area second (number of inductors and size of capacitors is the primary limit for area). Make sure you meet the specifications. If you cannot meet the specifications, come as close as possible.