Low power Radio Circuits

EE 142 Guest Lecture
Alyosha Molnar
Overview: Smart Dust Radio

Goal: A radio for sensor nodes which contain: sensors, ADC, μP and ~1kB RAM

- **Cost:** <$1, so few off-chip components:
  - Battery (3V Li coin cell)
  - Crystal (for network sync)
  - Antenna
  - High-Q inductor
  - 0.25μm

- **Performance:**
  - range ≤10m
  - data rate: ~100kb/s
  - <1% duty cycle
  - Battery life ~5yrs

- **Low power:** 1mW
  - Stack circuits to reuse current
  - Drive RF gates from high-Q LC oscillator
Top level

Bias stacking: current from oscillator is distributed to other blocks.

Transmitter: drives ~200µW signal to antenna.

Receiver: detects, down-converts and demodulates RF signals from antenna.

900MHz RF oscillator: tunes out all RF gates. Sets minimum current. 

Frequency control: sets channel, FSK modulation.

VDD = 2.7-3.6V

Vmid = 1.9V

Frequency control:

FSK Demod

Bits

Count

N

Bits

FSK Demod
Oscillator

- Cross-coupled inverters form a negative resistance.
- Tuning:
  - 902MHz-928MHz
  - ± 5% for process
  - ± 2.5% for inductor
- L = 17nH, Q = 30
- Swing = 1Vpeak
- Ibias = 200-300μA
Simulations (unloaded)

- Output Spectrum
- Phase noise
- Transient output
- Tail voltage (with IC)
Capacitor array

Made up of:

- Three 4-bit binary arrays of inversion capacitors
- An extra MSB
- A 4-bit DAC driving a near-minimum PFET varactor

<table>
<thead>
<tr>
<th>array</th>
<th>min step (MHz)</th>
<th>range (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>varactor</td>
<td>0.01</td>
<td>0.1</td>
</tr>
<tr>
<td>min cap</td>
<td>0.07</td>
<td>0.99</td>
</tr>
<tr>
<td>mid cap</td>
<td>0.89</td>
<td>12.29</td>
</tr>
<tr>
<td>max cap</td>
<td>11.69</td>
<td>142.14</td>
</tr>
</tbody>
</table>

Inversion cap: (Q*Con/Coff) is about 6x better than a normal switch plus capacitor.
Oscillator results

- Tuning from 820MHz to 960MHz
- LSB precision of 2.6 kHz
- Phase noise @ 1MHz = -107dBc
- PN rolls off @ 40dB/dec below 1MHz, 20dB/dec above.
- Noise is bias dominated.
- Oscillator starts to squegg for Ibias below 200μA (220μW)
Bias stacking: current from oscillator is distributed to other blocks.

900MHz RF oscillator:
- Tunes out all RF gates
- Sets minimum current

VDD = 2.7-3.6V

V_{mid} = 1.9V

Frequency control:
- Sets channel, FSK modulation

Transmitter:
- Drives ~200\mu W signal to antenna

Receiver:
- Detects, down-converts and demodulates RF signals from antenna
Frequency control loop (FLL)

- Have Crystal oscillator for network synchrony.
- RF Oscillator control is digital.
  - Crystal samples continuously running counter.
  - Subtracting successive samples gives $F_{RF}/F_{ref}$.
- Early counter stages set power, so
  - Use some custom logic.
  - divide-by-8 before counter
Divider design
Ring Divider Simulation

- Four stages with ~1ns delay set by input.
- Extra inverter incorporating reset capability.
- Fails by dividing by 9 (extra inverter causes cyclic slip).
Divider/FLL results

- FLL works
  - Accurately sets frequency
  - Stabilizes Frequency under bias perturbations
- Divider fails at low currents by under counting.
- Requires ~ 55µW
Top level

Bias stacking: current from oscillator is distributed to other blocks.

900MHz RF oscillator:
- Tunes out all RF gates
- Sets minimum current

Frequency control:
- Sets channel, FSK modulation

$V_{DD} = 2.7-3.6V$

Receiver: detects, down-converts and demodulates RF signals from antenna

Transmitter: drives ~200μW signal to antenna
Transmitter

- Transmitter is just a buffering of the oscillator.
- Want to transmit 100-300uW
- Simple antennas have impedance of ~100 ohms.
- For low cost, impedance matching is limited to a series inductor (can be part of the antenna).
- This implies the driver must source a 1mA, 200mV rms signal from a 3V supply: this will be inefficient!
- So stack two amplifiers and reuse bias.
Transmitter design

\[ I_{\text{bias}} = 300 \mu \text{A}, \]
\[ V_{\text{mid}} = 1.6 \text{ V} \]
\[ \rightarrow 2.4 \text{ k}\Omega \text{ vs } \sim 200 \Omega \]
Transmitter design

$V_{DD}$

$V_{mid}$

$I_{push-pull} = 600 \mu A$, $V_{stack} = 1.6 \text{ V}$

$\Rightarrow 1.2 \text{ k} \Omega \text{ vs } \sim 200 \Omega$
Transmitter design

\[ I_{\text{combo}} = 1200\mu A, \]
\[ V_{\text{stack}} = 0.8 \text{ V} \]
\[ \Rightarrow 300 \Omega \text{ vs } \sim 200 \Omega \]
Need to set up bias levels for four transistors of antenna driver

Varying supply is taken up by current source at the middle:

Voltage delivered through 60kΩ minimum width resistors
Transmitter Results

- Peak efficiency of 20% when radiating 300µW into 50Ω. (implies PA efficiency of >40%)
- Can radiate 1mW if reconfigured (efficiency~15%)
Top level

900MHz RF oscillator:
Tunes out all RF gates
Sets minimum current

VDD = 2.7-3.6V

Frequency control:
sets channel, FSK modulation

Vmid = 1.9V

Bias stacking:
current from oscillator is distributed to other blocks

900MHz RF oscillator:
Tunes out all RF gates
Sets minimum current

FLL

FSK Demod

Bits

Receiver: detects, down-converts and demodulates RF signals from antenna

IF = 1.8 MHz

Transmitter: drives ~200µW signal to antenna

RF = 900 MHz

FSK Demod

Bits
**Receiver Overview**

- **Architecture:**
  - Low power dictates Direct conversion or low IF.
  - Direct conversion suffers from DC offset, IP2, flicker noise
- **Low IF receiver**
  - Generate IF from LO.
  - No image rejection
- **Sensitivity:** $\sim -90\text{dBm}$
  - Want high gain up front
  - NF set by LNA, so spend most bias current in LNA
- **Interference**
  - Mostly out-of-band (cell phones etc)
  - No SAW filter up front
  - So use linear, passive mixer, followed by filtering

[Diagram of receiver components]

- LNA
- Mixer
- IF chain
- Baseband
- FSK Demod
- Rx bits
Rx Front End

- Resistively biased inverter as LNA.
  - $\text{Av} = \frac{2Gm_{\text{LNA}}}{(\omega_{\text{LO}}C_{\text{par}})}$ (20dB)
  - NF ~ 9dB
Rx Front End

- Resistively biased inverter as LNA.
  - $Av = \frac{2Gm_{\text{LNA}}}{\omega_{\text{LO}}C_{\text{par}}}$ (20dB)
  - NF ~9dB
- Passive mixer dissipates little power
  - $Vout$: 1-pole LPF at $2F_{\text{LO}}C_p/C_L$
Rx Front End

• Resistively biased inverter as LNA.
  – \( Av = \frac{2Gm_{LNA}}{\omega_{LO}C_{\text{par}}} \) (20dB)
  – NF \( \sim 9dB \)

• Passive mixer dissipates little power
  – Vout: 1-pole LPF at \( 2F_{LO}C_p/C_L \)
  – LPF shunts RF signals through switches.
  – \( P_{OBC} = -22dBm \)
Cool mixer/filter effect

\[ V_0(k + 1) = V_0(k) \left( \frac{C_L - C_P}{C_L + C_P} \right) \]

\[ i = A \sin(\omega_{LO} t + \Delta \omega k T) \]

\[ \frac{V_0}{A} = \frac{4A}{C_L \omega_{LO}} \left( j\Delta \omega + \frac{2C_P}{TC_L} - \frac{1}{2R_L C_L} \right) \]

\[ V_i \approx V_0 \sin(\omega_{LO} t) \]
Rx Front End

- Resistively biased inverter as LNA.
  - \( Av = \frac{2Gm_{LNA}}{\omega_{LO}C_{par}} \) (20dB)
  - NF ~9dB

- Passive mixer dissipates little power
  - Vout: 1-pole LPF at \( 2F_{LO}C_p/C_L \)
  - LPF shunts RF signals through switches.
  - \( P_{OBC} = -22\text{dBm} \)
• IF amplifier: CMOS with common-mode feedback.
• 26dB gain, loaded by IF mixer.
• 5-bit, differential current DAC cancels LO self-mixing.
IF mixer

- Switches sample to capacitors
  - Get S-C pole
  - Shunts DC at amplifier by 20dB.
IF mixer

- Switches sample to capacitors
  - Get S-C pole
  - Shunts DC at amplifier by 20dB.

- **IF from divided LO:**
  - I/Q phase split
IF mixer

- Switches sample to capacitors
  - Get S-C pole
  - Shunts DC at amplifier by 20dB.

- IF from divided LO:
  - I/Q phase split

- Use harmonic suppression:
  - Cancel 3rd, 5th harmonics by recombining 45° split signals
IF mixer

- Switches sample to capacitors
  - Get S-C pole
  - Shunts DC at amplifier by 20dB.
- IF from divided LO:
  - I/Q phase split
- Use harmonic suppression:
  - Cancel 3\textsuperscript{rd}, 5\textsuperscript{th} harmonics by recombining 45° split signals
  - 8 samples
- **IF mixer**

  - Switches sample to capacitors
    - Get S-C pole
    - Shunts DC at amplifier by 20dB.

  - **IF from divided LO:**
    - I/Q phase split

  **Use harmonic suppression:**
  - Cancel 3\(^{rd}\), 5\(^{th}\) harmonics by recombining 45° split signals
  - 8 samples
  - Weight, sum samples
IF mixer simulations

DC is rejected by 23dB

3rd harmonic mixing is suppressed by 20dB
Baseband

Wanted to demonstrate full bits-to-bits communication, so need an FSK demodulator.

- Additional gain and filtering is needed
- Simple Sallen-key filters provide 2 poles.
- Switched-cap amplifiers reject DC, add 12dB gain
- Flip-flop based demodulator clocks in ones/zeros
Receiver Results: sensitivity

- NF ~12dB
- Sensitivity ~ -93dBm
  - From 50Ω+14nH
  - BER ~10^{-3}, no error correction
- BW = 300kHz
- IF = 1.8MHz
Receiver Results: Interference

- Wide band 4dB desense: -12dBm
- Close-in desense a mix of compression, phase noise
- 3rd, 5th harmonic interference reduced by 40dB.
Top Level
Power summary

<table>
<thead>
<tr>
<th></th>
<th>tx, nom</th>
<th>tx, low</th>
<th>rx nom</th>
<th>rx low</th>
</tr>
</thead>
<tbody>
<tr>
<td>osc</td>
<td>480</td>
<td>319</td>
<td>336</td>
<td>161</td>
</tr>
<tr>
<td>Tx</td>
<td>630</td>
<td>464</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>bias</td>
<td>60</td>
<td>54</td>
<td>90</td>
<td>81</td>
</tr>
<tr>
<td>divider</td>
<td>90</td>
<td>80</td>
<td>90</td>
<td>80</td>
</tr>
<tr>
<td>counter</td>
<td>23</td>
<td>23</td>
<td>23</td>
<td>23</td>
</tr>
<tr>
<td>Ina</td>
<td>0</td>
<td>0</td>
<td>378</td>
<td>134</td>
</tr>
<tr>
<td>IF</td>
<td>0</td>
<td>0</td>
<td>90</td>
<td>52</td>
</tr>
<tr>
<td>bb</td>
<td>0</td>
<td>0</td>
<td>54</td>
<td>48</td>
</tr>
<tr>
<td>demod</td>
<td>0</td>
<td>0</td>
<td>75</td>
<td>75</td>
</tr>
<tr>
<td>total</td>
<td>1283</td>
<td>940</td>
<td>1136</td>
<td>654</td>
</tr>
<tr>
<td>Pout</td>
<td>250</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>sense, dBm</td>
<td></td>
<td>-93</td>
<td>-84</td>
<td></td>
</tr>
</tbody>
</table>

All powers in $\mu$W
Link Testing

- Two chips communicating through the air:
  - 20 kbps
  - 16 meters through 2 concrete walls
  - Nominal power
    (1.2mW RX, 1.3mW TX)
  - 100 kbps at shorter range
  - Battery, antenna, crystal oscillator inductor, tuning inductor
Conclusions

• Ultra-low power, very low cost radios demonstrated:
  – < 1.3 mW for both Receive and transmit
  – Only 4 off-chip components needed (< $1)
  – Purely digital interface.
  – Showed communication of 20kbps @ 16meters indoors.