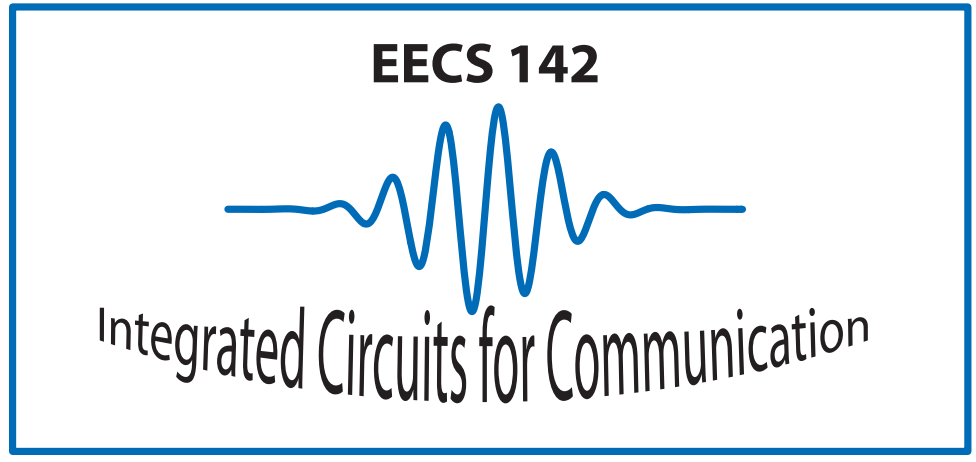

Lecture 14: MOSFET LNA Design

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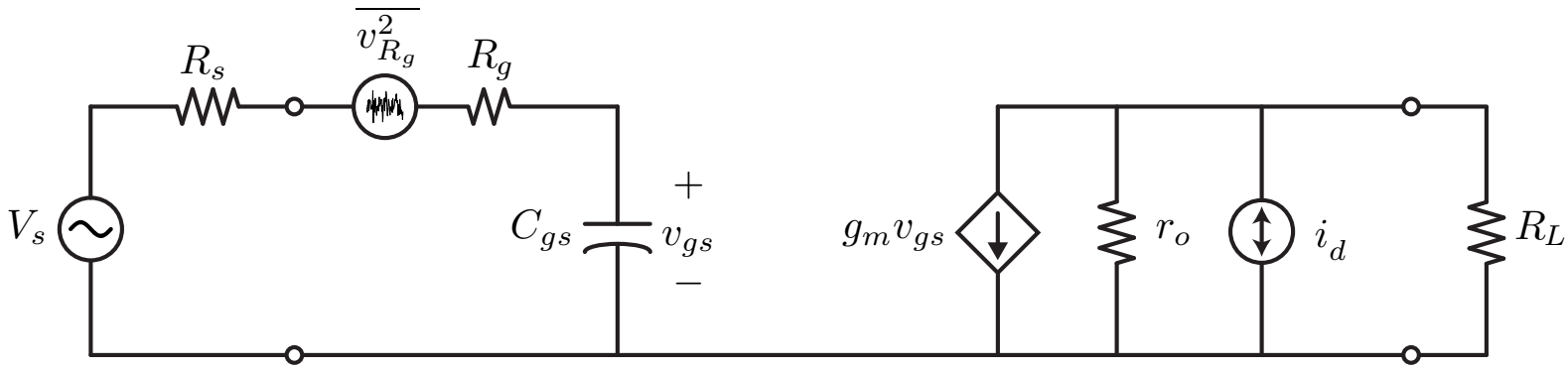
MOS Amplifier Noise Figure



- Let's recalculate the MOS amp noise figure (quickly). Note that the current gain of the MOS amp is given by

$$i_o = g_m v_1 = g_m \frac{v_s}{R_s + R_g + \frac{1}{j\omega C_{gs}}} \left(\frac{1}{j\omega C_{gs}} \right)$$

$$= v_s \frac{g_m}{1 + j\omega C_{gs}(R_s + R_g)} \approx v_s \frac{g_m}{j\omega C_{gs}(R_s + R_g)}$$

Noise Figure by Current Gain

- This can be rewritten as $i_o = G_m v_s$, where

$$G_m = -j\frac{\omega_T}{\omega}\frac{1}{R_s + R_g}$$

- This facilitates the noise calculations since the total noise is given by

$$\overline{i_{o,T}^2} = G_m^2(\overline{v_g^2} + \overline{v_s^2}) + \overline{i_d^2}$$

- And the noise figure is easily computed

$$F = 1 + \frac{\overline{v_g^2}}{\overline{v_s^2}} + \frac{\overline{i_d^2}}{G_m^2\overline{v_s^2}}$$

Expression for F (again)

- Substitution of the the various noise sources leads to

$$F = 1 + \frac{R_g}{R_s} + \frac{\left(\frac{\gamma}{\alpha}\right) g_m}{R_s} \left(\frac{\omega}{\omega_T}\right)^2 (R_s + R_g)^2$$

- Assume that $R_s \gg R_g$ to get

$$F = 1 + \frac{R_g}{R_s} + \left(\frac{\gamma}{\alpha}\right) \left(\frac{\omega}{\omega_T}\right)^2 g_m R_s$$

- It's important to note that this expression contains both the channel noise and the gate induced noise. If we assume that $R_g = R_{poly} + \frac{1}{5g_m}$, and the noise is *independent* from the drain thermal noise, we get a very good approximation to the actual noise without using correlated noise sources.

Minimum Noise for MOS Amp

- Let's find the optimal value of R_s

$$\frac{\partial F}{\partial R_s} = -\frac{R_g}{R_s^2} + \left(\frac{\gamma}{\alpha}\right)\left(\frac{\omega}{\omega_T}\right)^2 g_m = 0$$

- or

$$\frac{R_g}{R_s^2} = \left(\frac{\gamma}{\alpha}\right)\left(\frac{\omega}{\omega_T}\right)^2 g_m$$

$$R_{s,opt} = R_s = \sqrt{R_g}\left(\frac{\gamma}{\alpha}\right)\left(\frac{\omega}{\omega_T}\right)^2 g_m = \left(\frac{\omega_T}{\omega}\right)^2 \sqrt{\frac{R_g}{\left(\frac{\gamma}{\alpha}\right) g_m}}$$

- We now have (after simplification)

$$F_{min} = 1 + 2\left(\frac{\omega}{\omega_T}\right)\sqrt{g_m R_g \left(\frac{\gamma}{\alpha}\right)}$$

MOS Amp Example

- Let's find $R_{s,opt}$ for a typical amplifier. Say $f_T = 75\,\mathrm{GHz}$, $f = 5\,\mathrm{GHz}$, and $\left(\frac{\gamma}{\alpha}\right) = 2$. Also suppose that by proper layout R_{poly} is very small. The intrinsic gate resistance is given by

$$R_g = R_{poly} + \frac{1}{5g_m} \approx= \frac{1}{5g_m}$$

- To make the noise contribution from this term 0.1 requires that

$$\frac{R_g}{R_s} = 0.1 \qquad \frac{1}{5g_m R_s} = 0.1$$

$$5g_m R_s = 10 \qquad g_m = \frac{10}{5 \times 50\,\Omega} = \frac{1}{25}\,\mathrm{S} = 40\,\mathrm{mS}$$

MOS Amp Continued

- Note that for $V_{gs} - V_T = 200\,\mathrm{mV}$, the required current is fairly hefty

$$g_m = \frac{2I_{ds}}{V_{gs} - V_T} = 40\,\mathrm{mS}$$

$$I_{ds} = 40\,\mathrm{mS} \times 200\,\mathrm{mV} \times \frac{1}{2} = 4\,\mathrm{mA}$$

- The optimum source resistance is given by

$$R_{s,opt} = \frac{f_T}{f}\sqrt{\frac{R_g}{\left(\frac{\gamma}{\alpha}\right) g_m}} = 15\sqrt{\frac{5 \cdot 25}{2}} \approx 119\Omega$$

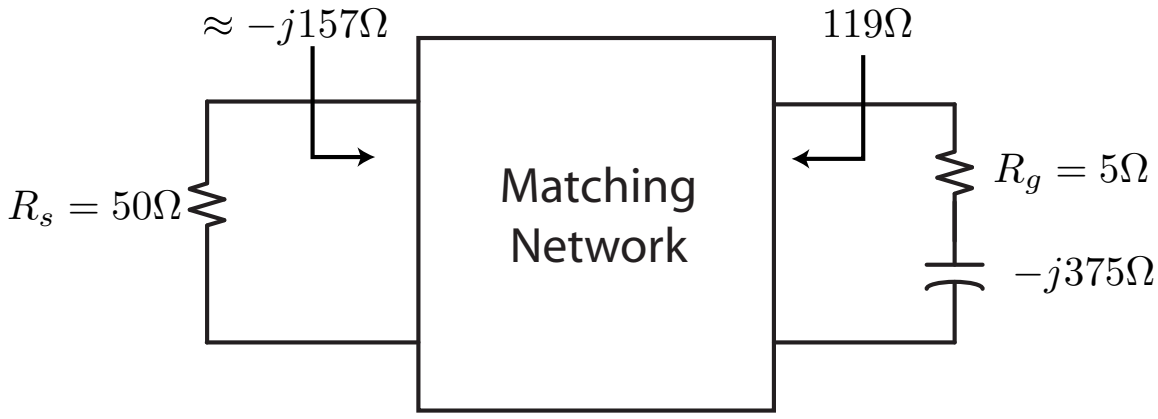
$$F_{min} = 1 + 2\frac{f}{f_T}\sqrt{g_m R_g \left(\frac{\gamma}{\alpha}\right)} = 1 + \frac{2}{15}\sqrt{5 \times 2/25} = 1.08$$

MOS Amp Continued

- This is a very low noise figure of $.35\,\mathrm{dB}$!!
- In practice, though, it'll be difficult to get this low of a noise figure and get useful gain with the simple common source. Let's see why.
- Note that $C_{gs} \approx g_m/\omega_T = 85\,\mathrm{fF}$. The input impedance of the FET is given by

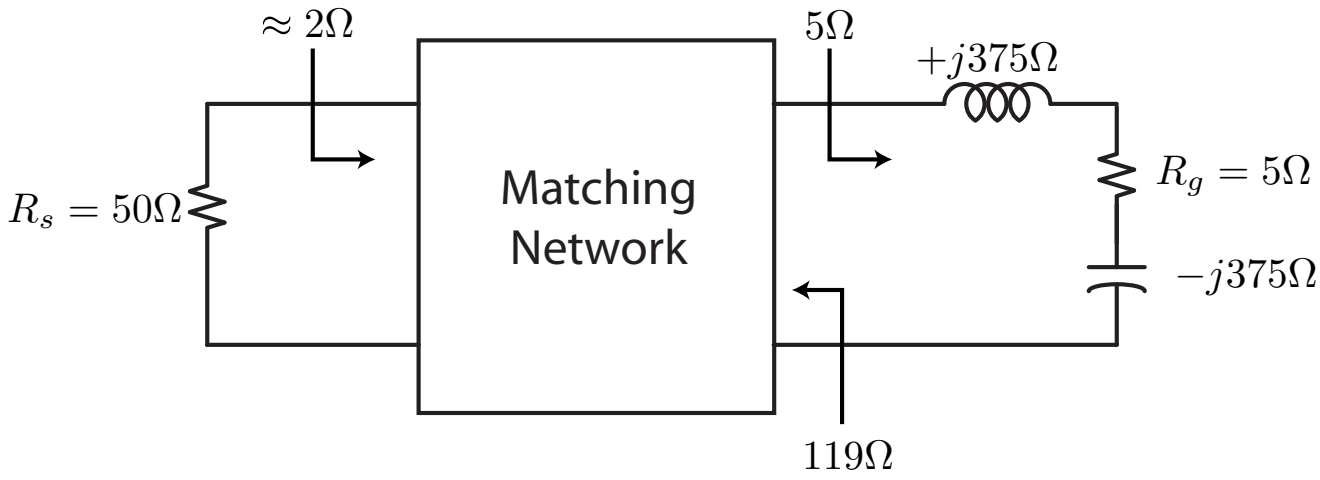
$$Z_i = R_g + \frac{1}{j\omega C_{gs}} = R_g - j\frac{\omega_T}{\omega g_m} \approx 5 - j375\Omega$$

Matching Option 1



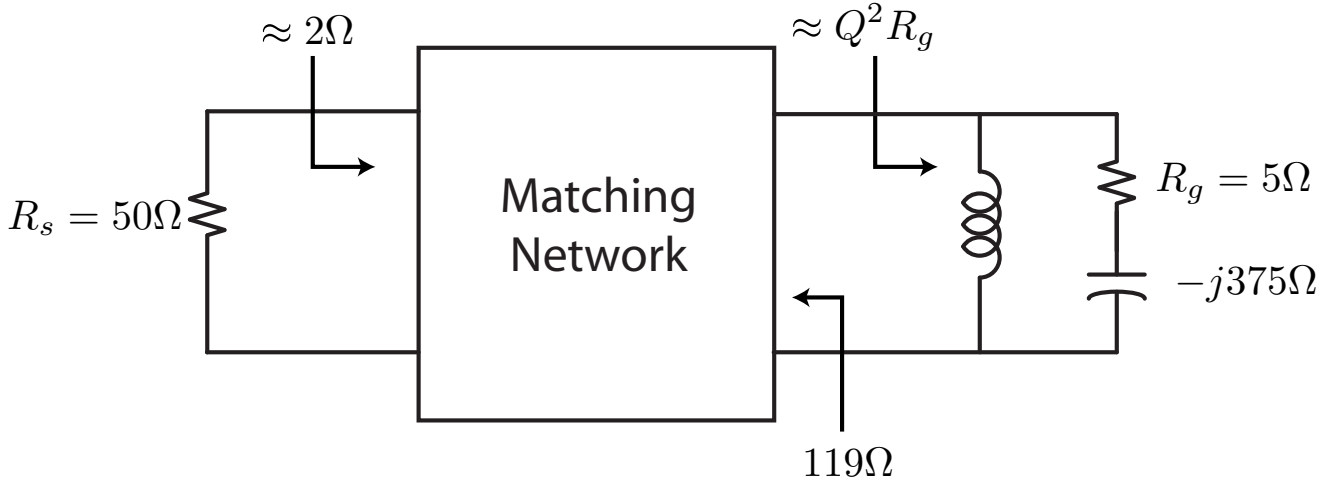
- Don't match the input impedance. Simply use a matching network to multiply the 50Ω source up to 119Ω. This means that the source (antenna) will see a termination that is $m = 119/50 = 2.38$ times smaller, or about 157Ω.
- This is a good for noise but a bad power match.

Matching Option 2



- Use an inductor to tune out the capacitive part of the input. This will add noise due to finite inductor Q. Note that the matching network will match this low 5Ω resistance down to $5\Omega/2.38 \approx 2\Omega$.
- Now the power match is even worse.

Matching Option 3



- Use a shunt inductor to resonate the input impedance. The inductor should be connected to the DC value of V_{gs} and can double as a bias element.

Option 3 (cont)

- But since the gate capacitance is high Q

$$Q = \frac{1}{\omega C_{gs} R_g} \approx \frac{1}{\omega C_{gs} \frac{1}{5 g_m}} = 5 \frac{f_T}{f} = 5 \times 15 = 75$$

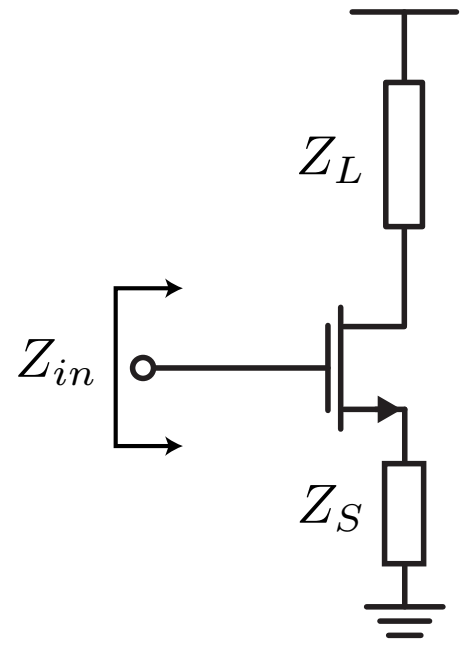
- The input resistance is going to be $Q^2 R_g \approx 28\,\mathrm{k}\Omega$, or too big.
- The matching circuit will bring this "down" to about $12\,\mathrm{k}\Omega$, a very poor match.

Source/Emitter Degeneration

- The voltage at the input of the amplifier is given by

$$v_x = i_x Z_{gs} + (i_x + g_m Z_{gs} i_x) Z_s$$

$$Z_{in} = Z_s + Z_{gs} + \underbrace{g_m Z_{gs} Z_s}_{\text{due to feedback}}$$



- Let's assume that Z_s is reactive (zero noise)

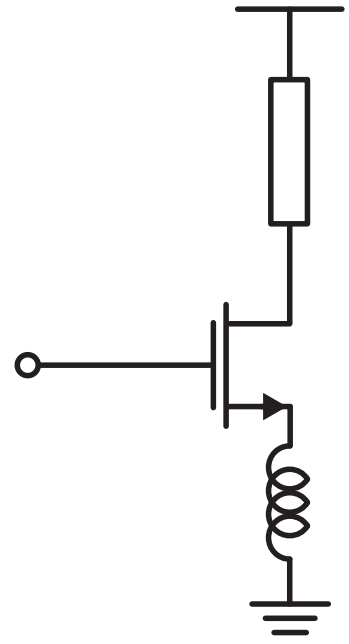
$$g_m Z_{gs} Z_s = g_m \frac{1}{j\omega C_{gs}} jX = \frac{g_m X}{\omega C_{gs}}$$

- which produces a purely passive input resistance if $X > 0$

Inductive Degeneration

- The reactive feedback from an inductor produces a broadband programmable real input impedance that can simplify matching (or even eliminate it altogether).

$$\Re(Z_{in}) = \frac{g_m L}{C_{gs}} \approx \omega_T L$$



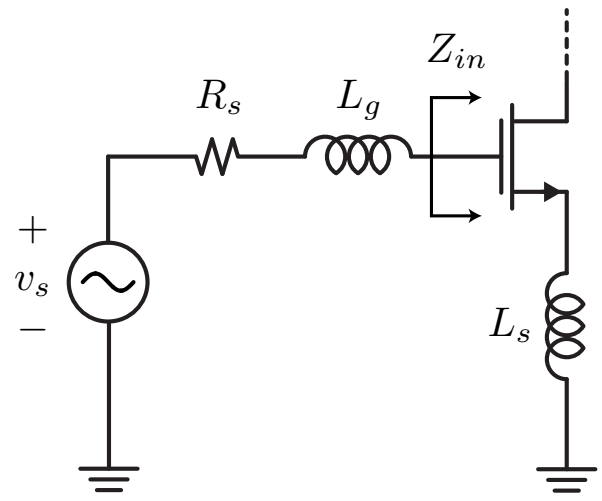
- We thus select L by $L = \frac{R_s}{\omega_T}$
- If this value of L is impractical, we can artificially reduce ω_T by inserting a capacitor in shunt with C_{gs}.

Series Resonant Input

- The input impedance of the FET with inductive degeneration is given by

$$Z_{in} = j\omega L_s + \frac{1}{j\omega C_{gs}} + \omega_T L_s$$

$$= j\omega L_s + \frac{1}{j\omega C_{gs}} + R_s$$



- The input impedance behaves like a series RLC circuit. We need to tune the resonant frequency of the series circuit to align with the operating frequency. This can be done by adding gate inductance L_g

Q Boosting

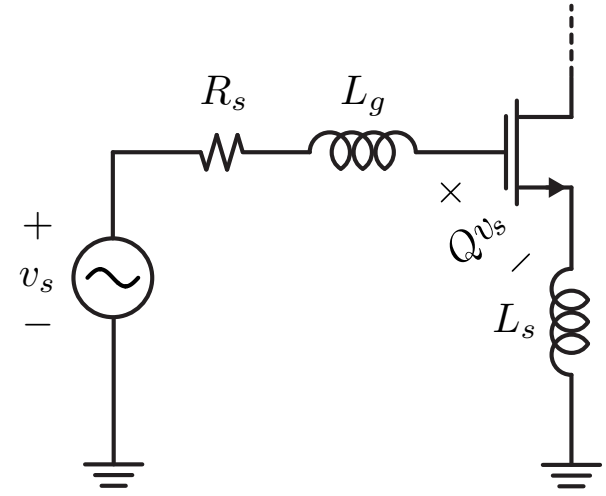
- Recall that in a resonant circuit, the voltage across the reactive elements is Q times larger than the voltage across the resistor.
- At resonance, the voltage across the resistors is simply v_s, so we have

$$v_{gs} = Q \times v_s$$

$$i_d = g_m v_{gs} = Q \times g_m v_s = G_m v_s$$

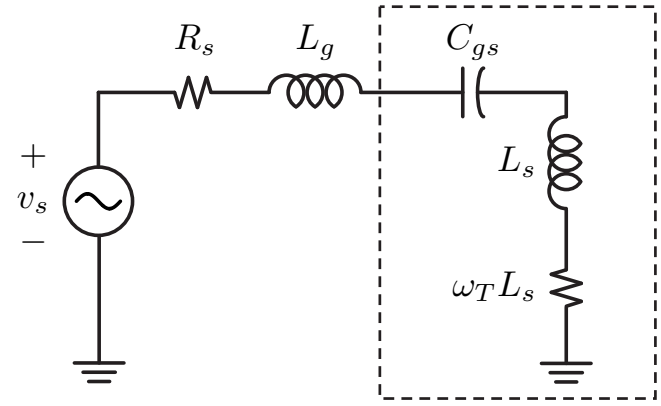
$$Q = \frac{1}{\omega_0 C_{gs} 2R_s}$$

$$G_m = Q g_m = \frac{g_m}{\omega_0 C_{gs} 2R_s} = \left(\frac{\omega_T}{\omega_0}\right) \frac{1}{2R_s}$$

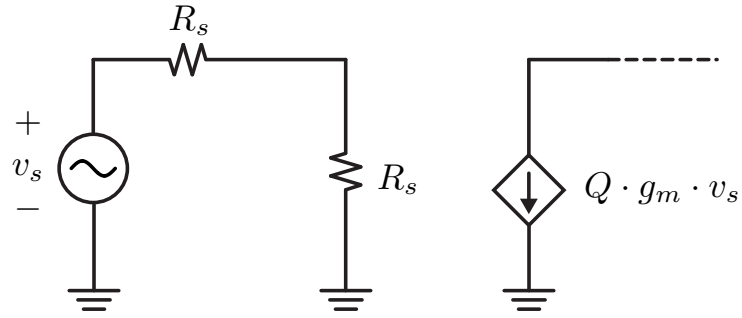


Equivalent Circuit at Resonance

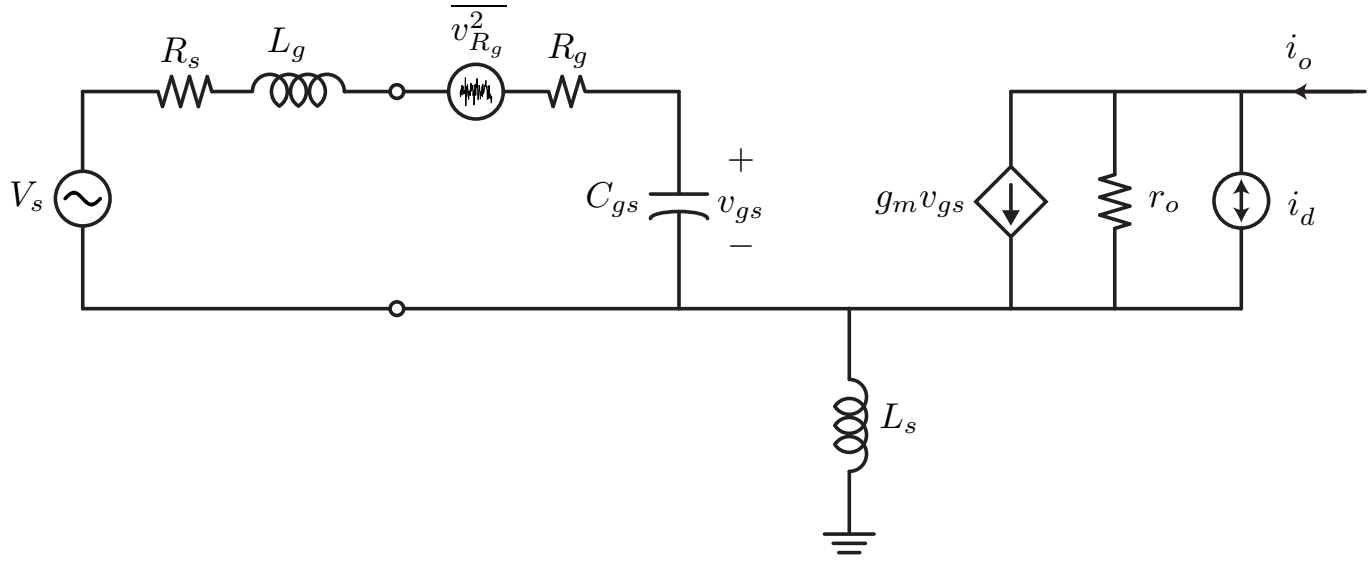
- From the source, the amplifier input (ignoring C_{gd}) is equivalent to the following circuit



- At resonance, the complete circuit is as follows

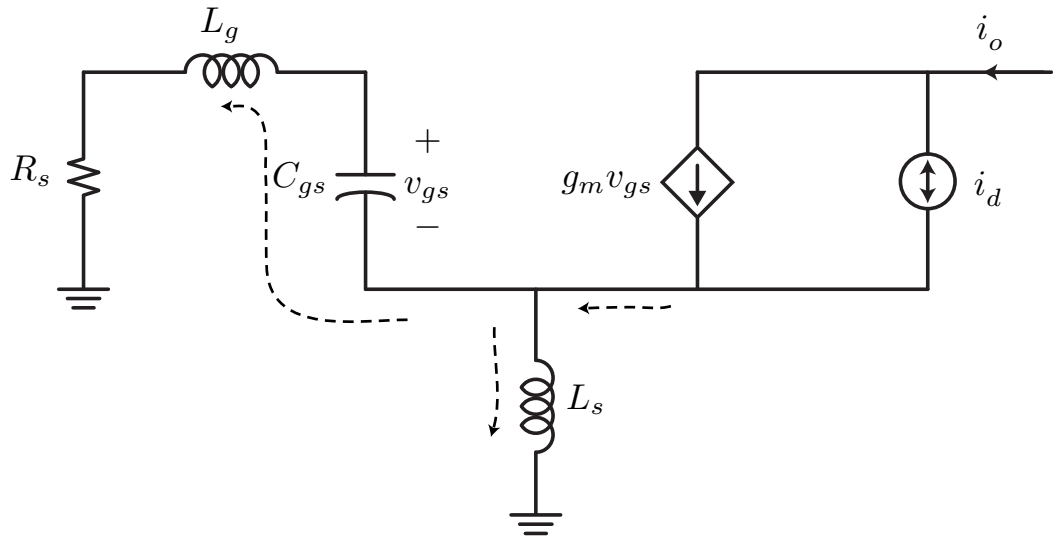


Noise Figure for Inductive Degen



- It's fairly easy to calculate the noise for the case with inductive degeneration. Simply observe that the input generators ($\overline{v_s^2}$ and $\overline{v_g^2}$) see a gain of G_m^2 to the output. The drain noise $\overline{i_d^2}$, though, requires a careful analysis.
- Since $\overline{i_d^2}$ flows partly into the source of the device, it activates the g_m of the transistor which produces a correlated noise in shunt with $\overline{i_d^2}$.

Drain Noise (degen)



- The above equivalent circuit shows that the noise component flowing into the source is given by the current divider

$$v_\pi = -(g_m v_\pi + i_d) \times \frac{j\omega L_s}{j\omega L_s + \frac{1}{j\omega C_{gs}} + j\omega L_g + R_s} \times \frac{1}{j\omega C_{gs}}$$

Drain Noise (degen)

- The denominator simplifies to R_s at resonance, so we have

$$v_\pi = -(g_m v_\pi + i_d) \times \frac{j\omega L_s}{R_s} \frac{1}{j\omega C_{gs}}$$

$$= -(g_m v_\pi + i_d) \times \frac{L_s}{C_{gs} R_s}$$

$$v_\pi \left(1 + \frac{g_m L_s}{C_{gs} R_s}\right) = -i_d \frac{L_s}{C_{gs} R_s}$$

- But $\omega_T L_s = R_s$, so we have

$$2v_\pi = -i_d \frac{L_s}{C_{gs} R_s} \quad \text{or} \quad g_m v_\pi = -\frac{i_d}{2} \frac{g_m L_s}{C_{gs} R_s} = -\frac{i_d}{2}$$

Total Output Noise (degen)

- So we see that only $1/4$ of the drain noise flows into the output! The total output noise is therefore

$$\overline{i_{o,T}^2} = G_m^2(\overline{v_s^2} + \overline{v_g^2}) + \frac{1}{4}\overline{i_d^2}$$

$$F = 1 + \frac{\overline{v_g^2}}{\overline{v_s^2}} + \frac{\overline{i_d^2}}{4\overline{v_s^2}G_m^2}$$

- Substitute as before and we have

$$F = 1 + \frac{R_g}{R_s} + \frac{\left(\frac{\gamma}{\alpha}\right) g_m (2R_s)^2}{4R_s}\left(\frac{\omega}{\omega_t}\right)^2$$

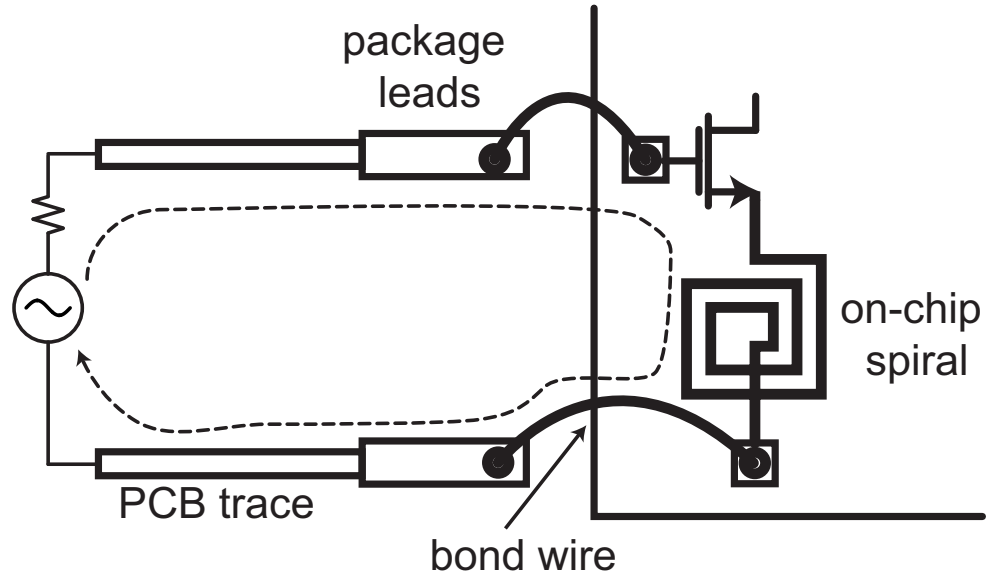
Noise Figure with Degen

- Note that the noise figure is the same as the common source amplifier

$$F = 1 + \frac{R_g}{R_s} + \left(\frac{\gamma}{\alpha}\right) g_m R_s \left(\frac{\omega}{\omega_t}\right)^2$$

- The inductive degeneration did not raise the noise ! So the minimum noise figure F_{min} is the same.
- The advantage is that the input impedance is now real and programmable ($\omega_T L_s$). By proper sizing, it's possible to obtain a noise and power match.

LNA Chip/Package/Board Interface



- Since the LNA needs to interface to the external world, its input network must transition from the Si chip to the package and board environment, which involves “macroscopic” structures such as bondwires and package leads.

Bond Wire Inductance

- One reason inductive degeneration is popular is because we can use package parasitics to our benefit. Some or all of L_s can be absorbed into the loop inductance (or the *partial* inductance of the bondwire)
- These parasitics must be absorbed into the LNA design.
- This requires a good model for the package and bondwires. It should be noted that the inductance of the input loop depends on the arrangement of the bondwires, and hence die size and pad locations.
- Many designs also require ESD protection, which manifests as increased capacitance on the pads.

Package Parasitics

- Recall that a changing flux generates an emf around a circuit loop. Let

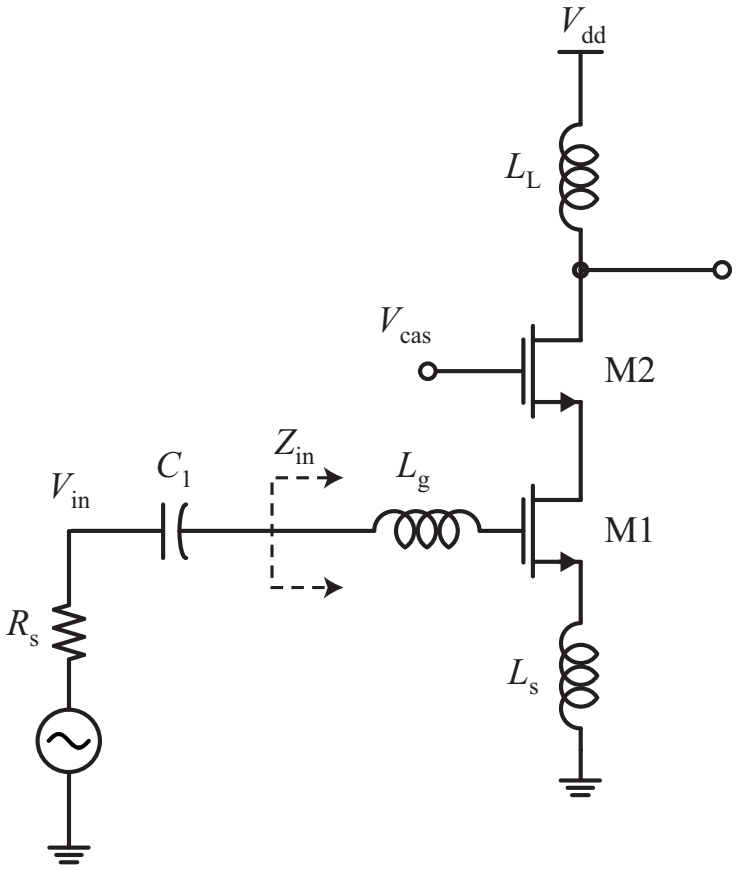
$$L = \frac{\psi}{I}$$

$$v_{emf} = \frac{d\psi}{dt} = L\frac{dI}{dt}$$

- Note that in reality ψ is composed of flux from all the loops in the package, causing undesired mutual coupling to other parts of the circuit

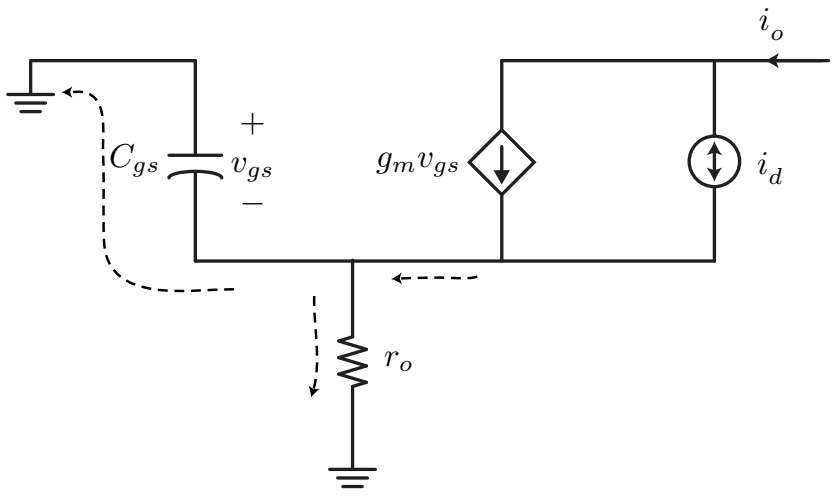
$$v_{emf} = \frac{d(\psi_1 + \psi_2 + \psi_2 + \cdots)}{dt} = L\frac{dI_1}{dt} + M_{12}\frac{dI_2}{dt} + \cdots$$

Cascode LNA



- It's very common to use a cascode device instead of a common source device.
- This simplifies matching since the cascode device is nearly unilateral.
- Let's show that the cascode device adds virtually no noise at low/medium frequencies.

Cascode Noise Contribution



- The noise contribution from the cascode is small due to the degeneration. For simplicity assume the transistor degeneration is r_o. Then most of the drain noise current will flow into C_{gs} at high frequency

$$v_\pi = (g_m v_\pi + i_d)\frac{1}{j\omega C_{gs}}$$

$$v_\pi(j\omega C_{gs} - g_m) = i_d$$

$$g_m v_\pi = \frac{-g_m}{g_m - j\omega C_{gs}} i_d = \frac{-1}{1 - j\frac{\omega}{\omega_T}} i_d \approx -i_d$$

Cascode (cont)

- A similar calculation shows that at low frequency, the noise into r_o produces an output current noise of

$$(i_d + g_m v_\pi) r_o = -v_\pi$$

$$i_d r_o = -v_\pi - g_m r_o v_\pi = -(1 + g_m r_o) v_\pi$$

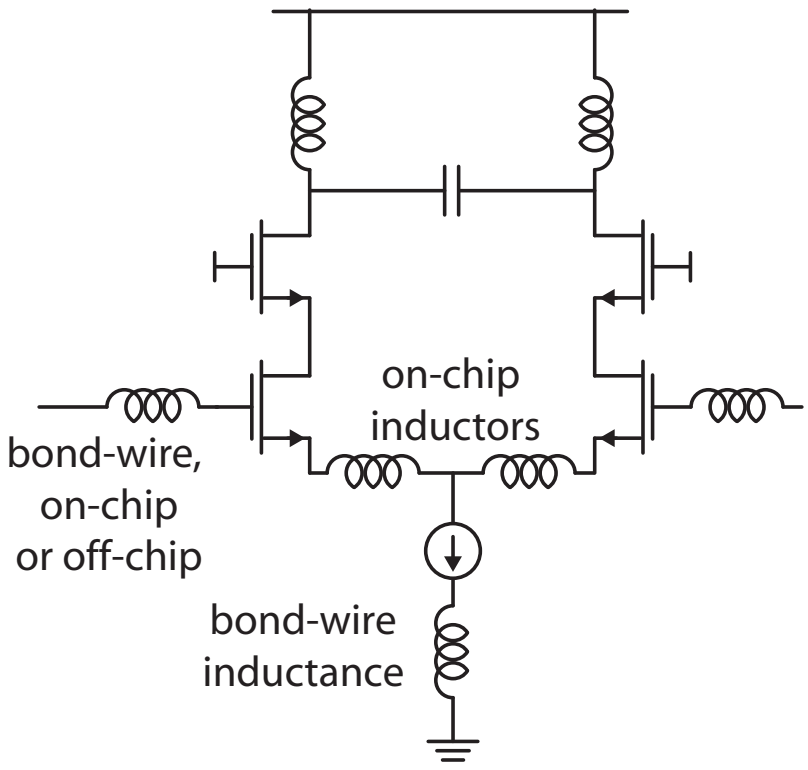
$$v_\pi = \frac{-r_o}{1 + g_m r_o} i_d$$

$$g_m v_\pi = \frac{-g_m r_o}{1 + g_m r_o} i_d \approx -i_d$$

- The total current noise is therefore

$$\left(1 - \frac{-g_m r_o}{1 + g_m r_o}\right) i_d = \left(\frac{1}{1 + g_m r_o}\right) i_d \approx 0$$

Differential LNA Design



- One undesired consequence of the package is that the parasitic inductors vary from part to part and require careful modeling and extra care to correctly implement the LNA.

- The advantage of a differential LNA is that the parasitics are only on the gate side, and not on the source of the transistors. The source inductors are realized with on-chip inductors with tight process tolerances.