

A CMOS Sub-harmonic Mixer for WCDMA

by

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Abstract

This report describes a sub-harmonic mixer for WCDMA applications. The circuit converts a 2 GHz RF signal directly to baseband using a 1 GHz LO frequency. The mixer uses common source MOSFETs with inductive degeneration to convert the input RF voltage to a current. This current is then steered using a switching network composed of triode-region MOSFETs that is driven with the LO and a 90 degree phase-shifted version of the LO. The mixer has a voltage conversion gain of 8dB, a noise figure of 6.4dB, and an IIP₃ of 5.3dBm. The performance has been verified using SpectreRF simulations.

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Chapter 1

Introduction

The current trend in RF communication systems is to produce smaller and less expensive receivers. One way to shrink the receiver is to eliminate as many off chip components as possible. This increased level of integration is also likely to reduce the cost of producing the system. The most common receiver architecture in production today is the superheterodyne receiver [1]. A typical block diagram of this type of receiver is shown in Figure 1.1. In a superheterodyne receiver, the incoming RF signal is amplified and filtered to remove the image signal. This is followed by the first downconversion to the intermediate frequency (IF). Then there is an IF chain which also contains gain and filtering. Finally the IF signal is downconverted again to baseband. The high-Q IF filters and the RF image rejection filter are both very difficult to implement without using off-chip components.

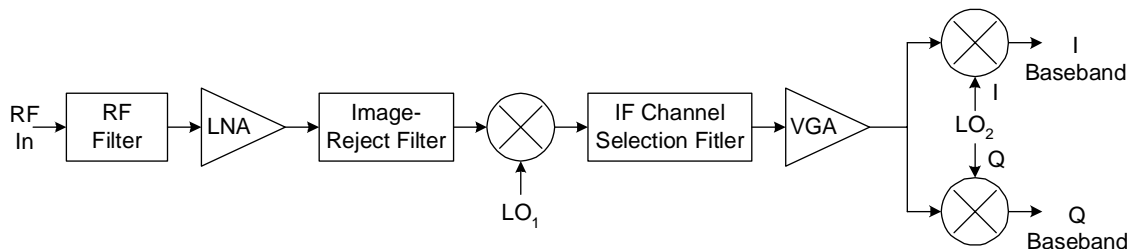


Figure1.1: Superheterodyne Architecture.

An attractive solution to the problems with fully integrating a superheterodyne architecture is to use a direct-conversion receiver instead. A typical block diagram for a direct-conversion receiver is shown in Figure 1.2. In a direct conversion receiver the incoming RF signal is filtered, amplified and then converted directly to baseband. Since

there is no IF signal, the high-Q IF channel selection filters, the IF amplifiers and the second downconversion mixers are not necessary. The image reject filter is not required because without an IF there is no image signal that needs to be removed. Because of these omissions, a direct conversion receiver can easily have a higher level of integration than a superheterodyne scheme. An added benefit of direct conversion is that since there is signal in both sidebands of the mixer, double sideband (DSB) noise figure is the appropriate measure of the signal to noise ratio degradation. A mixer will have a DSB noise figure that is approximately 3dB lower than it would if it were used in a system where single sideband (SSB) noise figure is applicable. This will be explained in more detail in section 2.3.

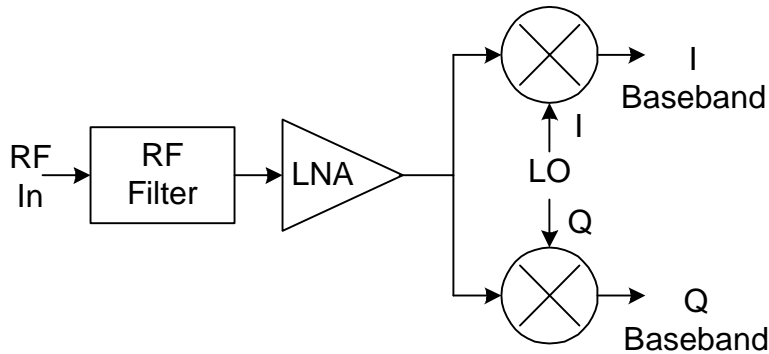


Figure1.2: Direct Conversion Architecture.

While the direct conversion receiver has some advantages over a superheterodyne scheme, it also has some disadvantages that make its implementation a challenge. Since the signal is converted directly to baseband with the first mixing operation, DC offsets, flicker noise and second-order distortion from the mixer will all fall in the signal band. Another problem is LO self-mixing. LO self-mixing occurs when

the LO signal (which has the same frequency as the RF signal) leaks to the input of the mixer by some feedthrough path and then mixes with itself. This self-mixing produces another DC offset.

In order to alleviate the effect of LO self-mixing a sub-harmonic mixer can be used in the receiver. A sub-harmonic mixer uses an LO signal that is a fraction of the desired downconversion frequency. Using a sub-harmonic mixer in a direct conversion receiver will reduce the LO self-mixing problem because the RF and LO frequencies will be different. Any LO signal that leaks to the input of the mixer will be mixed to a frequency outside of the signal band. Another potential advantage of a sub-harmonic mixer is that since the LO is at a lower frequency it may reduce the difficulty of designing the VCO and the LO buffers. To exploit these benefits, this project will focus on the design of a sub-harmonic mixer. The outline of this work is as follows.

Chapter 2: Discussion of the design considerations for a Sub-harmonic mixer for use in a WCDMA direct conversion receiver.

Chapter 3: An overview of possible architectures for the mixer.

Chapter 4: An examination of the chosen architecture.

Chapter 5: A summary of the mixer's performance and conclusions.

Appendix: A full listing of all component values.

Chapter 2

Design Considerations

The design considerations for a sub-harmonic mixer used in a direct conversion receiver are very similar to those for a standard mixer downconverting to an IF. The major differences are in the NF, IIP₂ and the LO leakage specifications. The change in the specifications for NF and IIP₂ are due to the fact that the mixer is being used in a direct-conversion receiver. The differences in the LO leakage requirements are due to direct-conversion and the fact that the mixer is sub-harmonic. The reason for the differences in all of these specifications will be explained in their respective sections of this chapter. The specifications for this project are typical for a direct conversion WCDMA mixer and are listed below:

Source impedance	50 Ω
Baseband Load impedance	800 Ω differential
Channel Bandwidth	2 MHz
Voltage conversion gain	≥ 0 dB
Power conversion gain	≥ -6 dB
DSB NF	≤ 7 dB
IIP ₃	≥ 4 dBm
IIP ₂	≥ 40 dBm
Output P _{-1dB}	≥ 0.8 V _{ppk}
LO input power	-10 dBm
Core current consumption	3 mA
2 · LO leakage to input	-85 dBm

2.1 Input and Output Impedance

In a superheterodyne receiver, there is an off-chip image reject filter between the LNA and the mixer. Since the mixer input is connected to an off-chip component with a typical impedance of 50Ω , it needs to be matched to avoid reflections on the transmission line connecting image reject filter to the mixer. In a direct conversion receiver, there is no image reject filter between the LNA and the mixer, so the mixer is directly connected to the LNA output without going off-chip. This on-chip connection would be much smaller than the wavelength of the input signal. Because of this, reflections are not a problem and matching the input of the mixer is not required. However, since the mixer in this project is being designed without an LNA preceding it, the inputs would have to come from off-chip and the input needs to be matched to the source impedance that will drive it.

The design assumes the input impedance (Z_0) is 50Ω , since this is the source impedance of almost all input sources. The input reflection coefficient (S_{11}) is a good measure of the input match. S_{11} is defined as the ratio of the reflected wave voltage to the incident wave voltage at the input of the mixer and can be calculated using equation 2.1.

$$S_{11} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \quad (2.1a)$$

$$S_{11} (dB) = 20 \cdot \log |S_{11}| \quad (2.1b)$$

For a perfect input match $Z_{in} = Z_0 = 50\Omega$. In most practical cases it is not necessary to have a perfect match. An $S_{11} < -10$ dB, which corresponds to a reflection of less than 10%, is usually sufficient.

The output of the mixer for a direct conversion receiver is at baseband so there is no need to match the output of the mixer to the load impedance. The load impedance of the mixer is the input impedance of the baseband channel selection filter. For this design a typical value of 800Ω differential is assumed.

2.2 Conversion Gain

The conversion gain of a mixer is defined as the ratio of the desired IF or baseband output to the RF input. If the conversion gain is less than 1, it is referred to as a conversion loss. This ratio can be expressed in terms of voltage or power and is usually given in dB:

$$PowerGain(dB) = 10 \cdot \log\left(\frac{P_{out}}{P_{in}}\right) \quad (2.2a)$$

$$VoltageGain(dB) = 20 \cdot \log\left(\frac{V_{out}}{V_{in}}\right) \quad (2.2b)$$

If the input is matched, a simple relation between the two gains is given by:

$$PowerGain(dB) = VoltageGain(dB) - 10 \cdot \log\left(\frac{R_S}{R_L}\right) \quad (2.3)$$

where R_S is the source resistance and R_L is the load resistance.

The conversion gain of a mixer is an important specification because it affects the noise figure and linearity of the overall receiver. When calculating the overall input referred noise figure of the system, the noise from the stages following the mixer will be attenuated by the gain of the mixer or amplified by its loss. The conversion gain of a mixer will affect the overall linearity because the gain or loss will change the signal level presented to the stages following the mixer.

2.3 Noise Figure

The noise figure of a mixer is a measure of how much the signal-to-noise ratio is degraded by the mixer. An equation for noise figure is given as:

$$NF = \frac{SNR_{INPUT}}{SNR_{OUTPUT}} = \frac{N_s + N_a}{N_s} \quad (2.4)$$

where SNR_{INPUT} and SNR_{OUTPUT} are the signal-to-noise ratio at the input and output respectively. N_s is the output noise power due to the source impedance and N_a is the output noise power added by the mixer. A good approximation for Equation 2.4 is given by Equation 2.5 where Vn^2 is an input referred voltage noise source.

$$NF \approx 1 + \frac{Vn^2}{4kTR_s \Delta f} \quad (2.5)$$

Mixer noise figure can be specified as either single-sideband or double-sideband. SSB noise figure (SSB NF) is used for mixers that only contain input signal in one sideband of the input. The other sideband is removed by an image reject filter. DSB noise figure (DSB NF) applies to mixers where the input signal is contained in both input sidebands. DSB noise figure is applicable to direct conversion downconverters and SSB applies to most other mixers. SSB NF assumes the noise coming from the source comes from only one of the input sidebands, while DSB NF assumes it comes from both input sidebands. If the conversion gain is equal for both the RF and image bands, the input referred single sideband noise power is twice as big as the input referred double side band noise power [2]. If we define an input referred voltage noise source from a case where SSB NF was applicable as Vn^2_{SSB} , the same mixer would have a double side band equivalent, Vn^2_{DSB} , that is half as big. We can write:

$$NF_{SSB} = 1 + \frac{Vn^2_{SSB}}{4kTR_s\Delta f} \quad (2.6)$$

$$NF_{DSB} = 1 + \frac{Vn^2_{DSB}}{4kTR_s\Delta f} \quad (2.7)$$

Equations 2.7 can be re-written as:

$$NF_{DSB} = 1 + \frac{Vn^2_{SSB}}{2 * 4kTR_s\Delta f} \quad (2.8)$$

Substituting Equation 2.6 into Equation 2.8 leads to the following relation between SSB and DSB NF:

$$NF_{DSB} = 1 + \frac{1}{2}(NF_{SSB} - 1) \quad (2.9)$$

Expressing this equation in dB results in:

$$NF_{DSB}(dB) = 10 \cdot \log \left(1 + \frac{1}{2} \left(10^{\frac{NF_{SSB}(dB)}{10}} - 1 \right) \right) \quad (2.10)$$

In addition to using DSB NF instead of SSB NF, there is another difference between the NF of a mixer converting to an IF and the NF of a direct conversion mixer, which is the effect of flicker noise. In a superheterodyne receiver, the flicker noise of the mixer is not a major concern since it is usually outside of the IF band. However in a direct conversion receiver flicker noise shows up in band. This causes the noise figure to vary across the output signal band as shown in Figure 2.1. At lower frequencies the signal-to-noise ratio is made worse by flicker noise. The effect on system performance depends on the modulation scheme used as well as the flicker noise corner frequency. For a wide-band spread spectrum modulation scheme like the one used for WCDMA, the spreading operation codes each bit over a pseudorandom sequence [3], which spreads the information across the signal band. Because the information is spread across the signal

band, a WCDMA receiver can tolerate some degradation of the SNR at low frequencies. One good way to get a fair noise figure value is to average the extra low frequency output noise power across the whole signal band. To calculate this average noise figure one needs to know the NF at a low frequency where the flicker noise dominates as well as the NF at a frequency where white noise dominates. Equation 2.4 follows directly from Equation 2.4.

$$NF = 1 + \frac{N_a}{N_s} \quad (2.11)$$

The noise figure as a function of frequency can be written as

$$NF(f) = B + \frac{A}{f} \quad (2.12)$$

where B is the noise figure where white noise is the dominant source and A is a constant with units of Hz that is numerically equal to noise figure at 1Hz. To get the average NF, the total output noise should be integrated across the output band (f_1 to f_2) and then divided by the output noise due to the source integrated across the same band. Assuming that N_s is independent of frequency the average NF, \overline{NF} , can be expressed as

$$\overline{NF} = \frac{\int_{f_1}^{f_2} (N_s + N_a(f)) \cdot df}{\int_{f_1}^{f_2} N_s \cdot df} = \frac{\int_{f_1}^{f_2} NF(f) \cdot df}{f_2 - f_1} \quad (2.14)$$

Substituting Equation 2.12 into 2.14 gives

$$\overline{NF} = B + A \frac{\ln\left(\frac{f_2}{f_1}\right)}{f_2 - f_1} \quad (2.11)$$

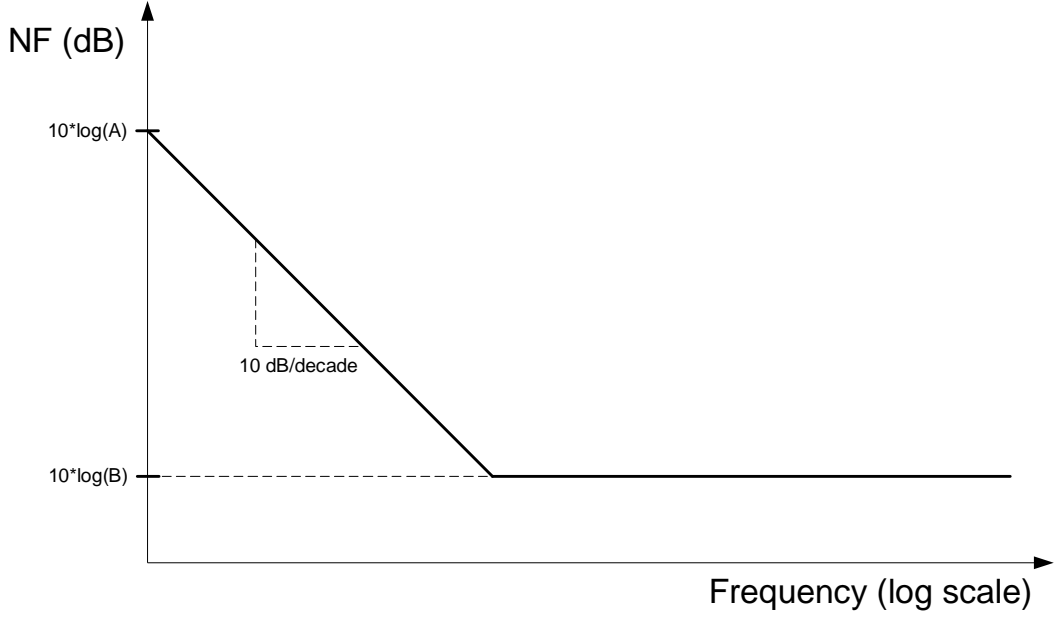


Figure 2.1: Noise figure vs. frequency for a direct conversion mixer.

2.4 Distortion

A mixer performs frequency translation so it is inherently a non-linear circuit. However, it is desirable for a mixer to act very linearly with respect to all nonlinearities except the one giving the desired frequency conversion. In general, a Volterra series for the mixer can be written as:

$$S_o = a_1(\omega_1) \circ S_i + a_2(\omega_1, \omega_2) \circ S_i^2 + a_3(\omega_1, \omega_2, \omega_3) \circ S_i^3 + \dots \quad (2.12)$$

where S_i is the input signal, S_o is the output signal shifted in frequency by the desired conversion and the dot operator, \circ , denotes a complex operator on the magnitude and phase, defined as:

$$X(\omega_1, \omega_2, \dots) \circ e^{j(\omega_1 + \omega_2 + \dots)t} = |X(\omega_1, \omega_2, \dots)| e^{j(\omega_1 + \omega_2 + \dots)t + \angle X(\omega_1, \omega_2, \dots)} \quad (2.13)$$

If S_i contains two tones at $f_1 + f_{LO}$ and $f_2 + f_{LO}$ and the desired downconversion frequency is f_{LO} the desired tones in S_o would be at f_1 and f_2 . The N^{th} order term in the volterra series would produce components at all frequencies described by Equation 2.14.

$$\begin{aligned}
& k \cdot f_1 \pm l \cdot f_2 \\
& \text{where : } k + l = N
\end{aligned}
\tag{2.14}$$

The input-referred N^{th} order intercept point (IIP_N) is used to characterize the distortion performance of a receiver. IIP_N is defined as the input power level where an N^{th} order distortion product's power is equal to the power of desired output. The desired output comes from the first order term in Equation 2.12 so a 1 dB increase in input power results in a 1 dB increase in the output power. The N^{th} order distortion comes from the N^{th} order term in Equation 2.12 so a 1 dB increase in input power results in an N dB increase in output distortion power. Figure 2.2 shows the typical relation between the desired signal level and the N^{th} order distortion level at the output of a mixer. The solid lines are the actual signal power observed at the frequency of interest and the dashed lines represent the ideal behavior of the first and N^{th} order terms of Equation 2.12. At low-power levels, the actual and ideal curves coincide, but as the input power is increased both curves show compression from their ideal values. This compression occurs because the higher order terms in Equation 2.12 produce frequency components at the same frequency as the first and N^{th} order terms. These components are negligible until the input power reaches a certain level. Once this level is reached, the higher order distortion components will affect the slope of the power curves as shown in Figure 2.2. From the geometry of Figure 2.2 it is straightforward to show that:

$$IIP_N = P_{in} + \frac{P_{out1} - P_{outN}}{N - 1}
\tag{2.15}$$

where P_{OUT1} and P_{OUTN} are the measured output power of the desired signal and N^{th} order distortion with an input of P_{in} .

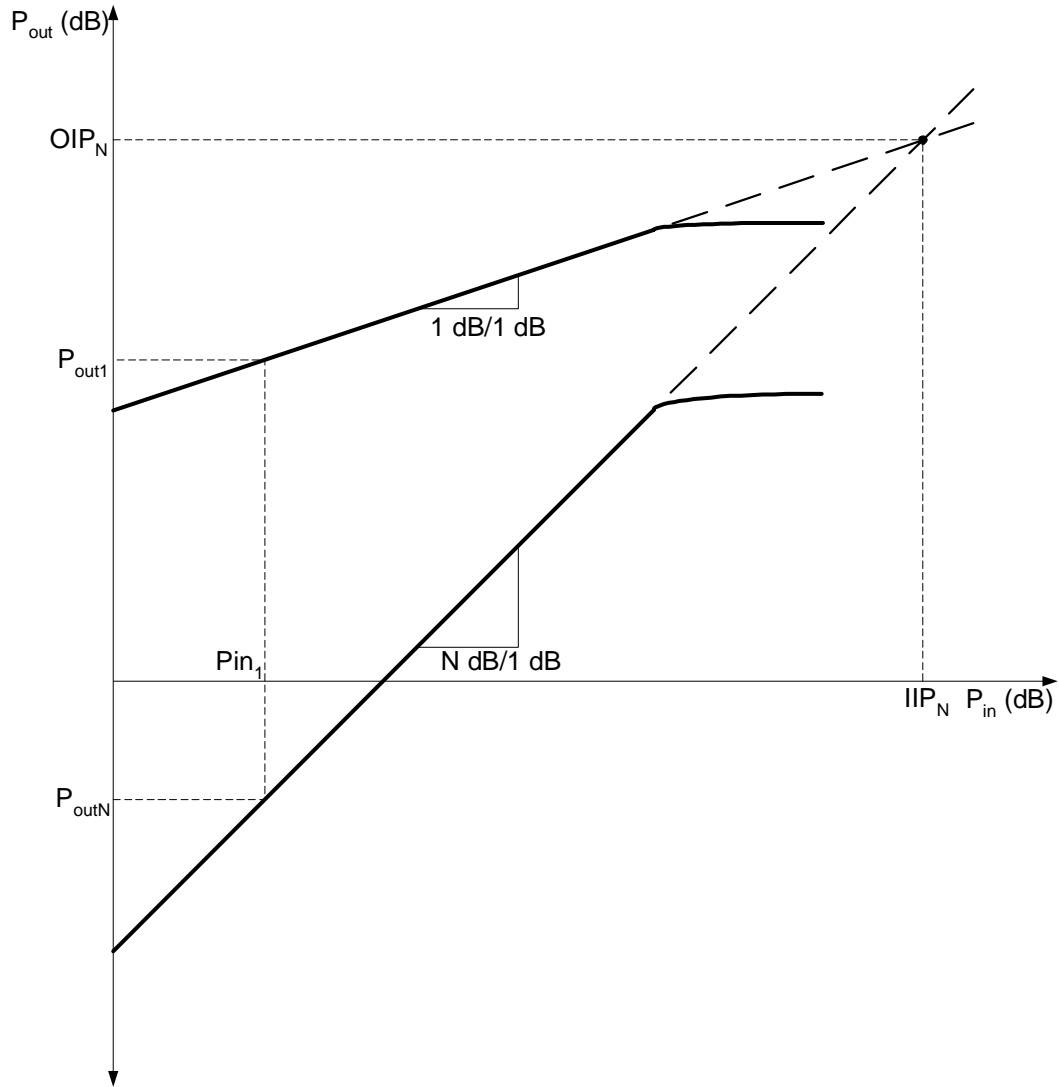


Figure 2.2: First order and Nth order output power vs. input power.

2.4.1 Third-order Intermodulation Distortion

As shown in section 2.4, if two tones are applied to a mixer they will produce distortion at many different frequencies in the mixer's output. Many of these components lie outside the desired signal band and are filtered out at some point in the receiver chain. However, some do appear in the signal band and cannot be filtered. If two input tones, at $f_1 + f_{LO}$ and $f_2 + f_{LO}$, are close in frequency the intermodulation components at $2f_2 - f_1$ and $2f_1 - f_2$ will be close to f_1 and f_2 , making them difficult to filter without also

removing the desired signal. These products are called third-order intermodulation (IM_3) products. Figure 2.3 shows the frequency spectrums at the input and output of a typical mixer including the IM_3 products.

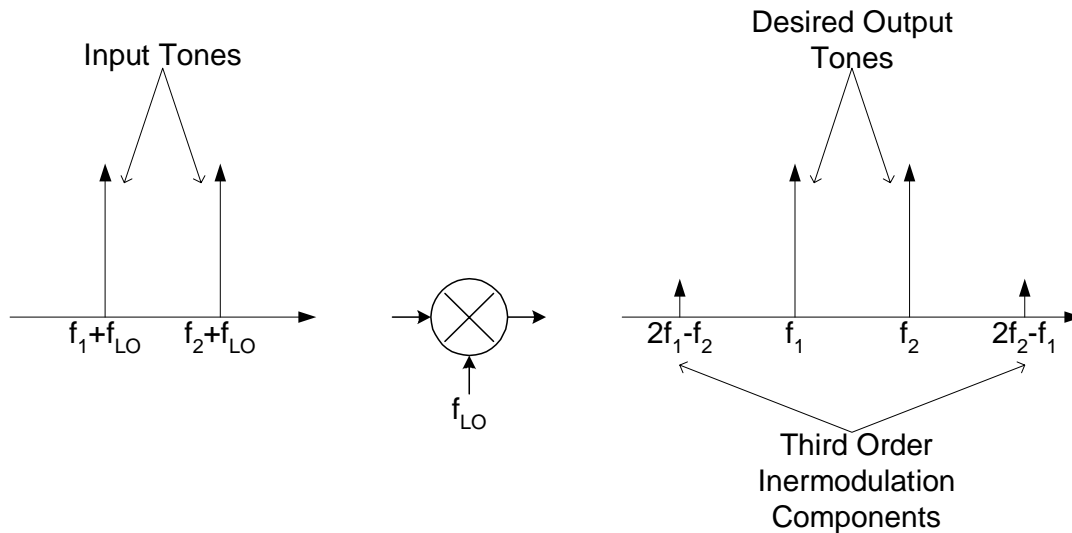


Figure 2.2: Frequency spectrum of a mixer.

2.4.2 Second-order Intermodulation Distortion

Second-order distortion performance is not critical in a mixer that is downconverting its input to an IF, since the second order products are out of the signal band. However, a mixer that is converting directly down to baseband has very stringent IIP_2 requirements. To see why this is true, consider two interferers at $f_1 + f_{LO}$ and $f_2 + f_{LO}$ shown in Figure 2.4. If f_1 and f_2 are approximately equal, their second order intermodulation products at $f_1 - f_2$ and $f_2 - f_1$ lie near DC, which is in the signal band.

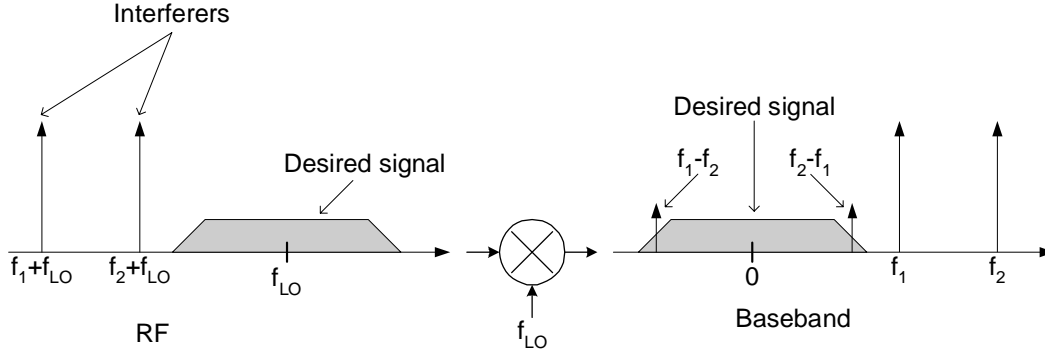


Figure 2.4: Second order distortion in a direct conversion mixer.

2.4.3 1dB Compression Point

It can be seen from Equation 2.14 that all odd-order nonlinearities will contribute signal power to the same frequency as the desired output signal. At low input powers, this added component is insignificant, but as the input power increases, the conversion gain of the mixer will expand or compress depending on whether the non-linearity is in or out of phase with the fundamental component. In most practical mixers, the components are out of phase and the conversion gain undergoes compression. The metric generally used to gauge the gain compression is the 1 dB compression point (P_{-1dB}). This is defined as the input or output signal level where the gain is decreased by 1 dB from its ideal value. Like IIP_3 , P_{-1dB} is used to estimate the largest input that a mixer can handle. However, IIP_3 is specified by extrapolating the first and third order curves from their values with small inputs, while P_{-1dB} is actually measured under large signal input conditions.

It is straightforward to show that if the compression is caused exclusively by third-order nonlinearity the input P_{-1dB} is

$$P_{-1dB} = IIP_3 - 9.6dB \quad (2.16)$$

However, it is often the case that nonlinearities higher than third-order contribute to the gain compression or the supply headroom limits the output signal. Both of these cause 2.16 to be inaccurate [4].

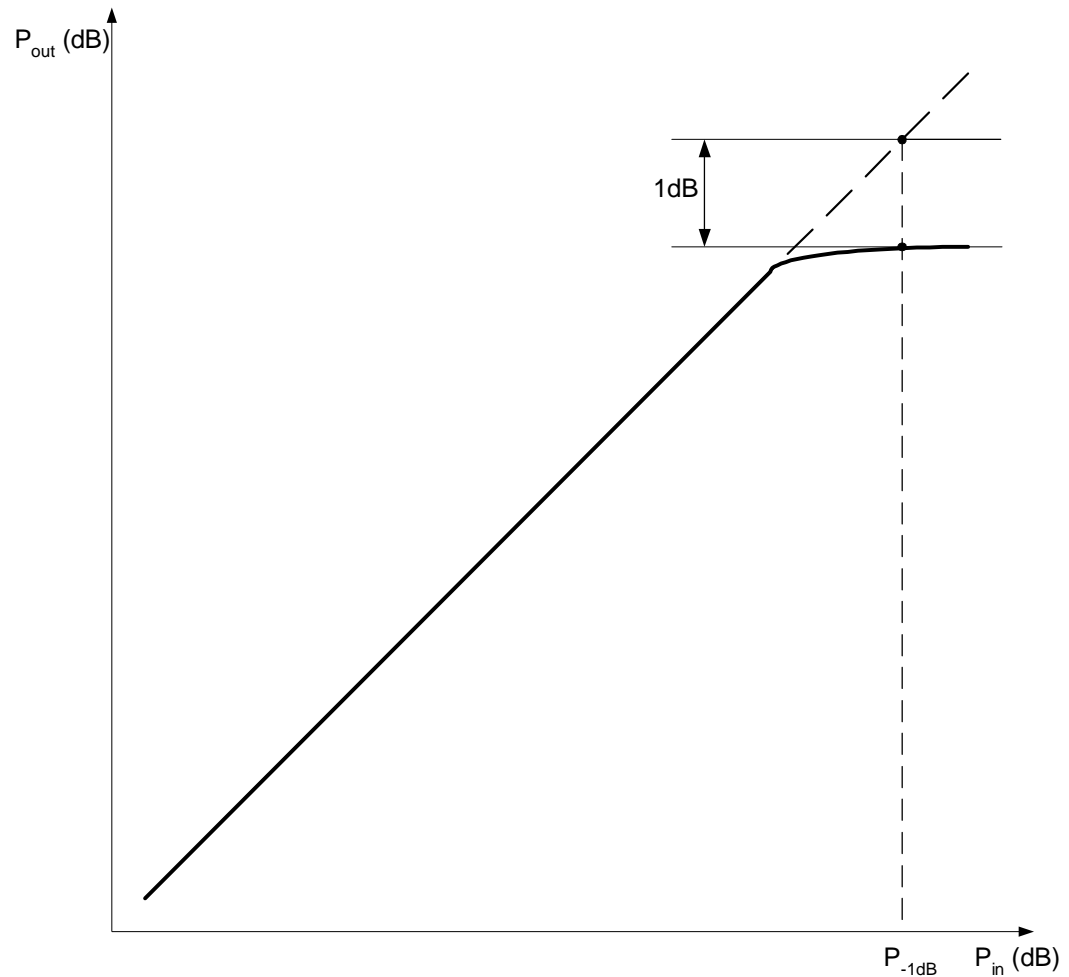


Figure 2.5: Graphical representation of the input P_{-1dB} .

2.5 LO Input Power

In order to operate properly, a mixer must be driven at the LO port by a sufficiently large LO signal. This signal's size is limited by the power delivered by the oscillator generating the LO signal. In most mixers, the LO supplied by the oscillator is

not large enough. Therefore there is usually an LO buffer between the oscillator and the mixer.

2.6 LO Feedthrough

In most receive mixers, it is important to have isolation between the LO and RF ports. Since the LO signal is quite large, a significant amount of it may leak to the mixers input and then leak back to the antenna through the reverse isolation of the LNA. This LO signal at the antenna will radiate out and can interfere with other nearby receivers. This leakage problem is especially problematic for a direct conversion receiver because the LO frequency is in the center of the LNA and antenna passband. A problem caused by LO leakage to the mixer input that is exclusive to direct conversion mixers is LO self-mixing. Any LO leaking to the input of the mixer will mix with itself and create a DC spur at the output. This spur is in the signal band and can be time varying, so it cannot be canceled.

As was mentioned in Chapter 1, LO self-mixing can be alleviated by using a sub-harmonic mixer. Since the LO frequency does not equal the RF frequency any LO leakage to the input will mix to some frequency that is out of band. In addition, because the LO is no longer at the center of the RF passband, using a sub-harmonic mixer also reduces the amount of LO leakage that will make it all the way back to the antenna. Since the signal is downconverted by $2 \cdot \text{LO}$, any LO 2nd harmonic generated by the circuit can leak to the input and cause a problem similar to standard LO self-mixing. Therefore, a sub-harmonic mixer has a specification for $2 \cdot \text{LO}$ feedthrough instead of LO feedthrough.

Chapter 3

Choice of Topology

There are several different ways to implement a sub-harmonic mixer. To select the best topology for this project, the architectures must be compared. The following sections discuss some of the different ways to implement a sub-harmonic mixer and the properties of each as they relate to use in a direct-conversion receiver.

3.1 Standard Mixer

Any standard mixer can be used as a sub-harmonic mixer because mixers perform conversion with multiple harmonics of their LO frequency. The frequencies present at the output are described by:

$$f_{OUT} = f_{RF} \pm n \cdot f_{LO} \quad (3.1)$$

where n is an integer. Figure 3.1 shows a generalized output spectrum of a mixer where, to reduce unnecessary clutter, neither the LO frequency nor its harmonics are shown. If a balanced mixer is used, the tones from $n=0$ and the even integers are not present at the output (these tones are indicated by dashed lines).

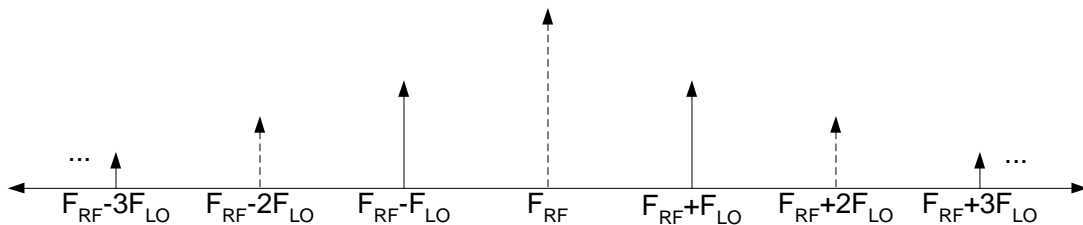


Figure 3.1: Mixer output spectrum.

The major drawback with this architecture is that the fundamental mixing responses ($F_{RF}-F_{LO}$, $F_{RF}+F_{LO}$) are greater than any of the harmonic responses, resulting in a desired conversion gain that is lower than the fundamental conversion gain. This larger fundamental conversion gain will degrade the noise figure. To see why, consider a case

where the desired conversion is from $f_{IF} + 2f_{LO}$ to f_{IF} . Input noise at $f_{IF} + f_{LO}$ will be converted to f_{IF} with a greater gain than the input noise from $f_{IF} + 2f_{LO}$, which severely degrades the noise figure.

3.2 Antiparallel Diode Pair Mixer

The noise problem caused by a circuit with a conversion gain higher than the desired conversion makes it preferable to use a mixer with maximum conversion gain for the desired input band. A topology with no fundamental conversion is the antiparallel diode pair (APDP) (Figure 3.2). To see why there is no fundamental conversion, consider Figure 3.2 [5]. $V_{LO}(t)$, $g_1(t)$ and $g_2(t)$ are plots of the LO voltage and the conductance of diode 1 and diode 2 as functions of time. The sum of $g_1(t)$ and $g_2(t)$ is the conductance of the diode pair. It is clear that the total conductance has only even order harmonics of the LO frequency. Thus frequency conversion with twice the LO frequency has the greatest conversion gain.

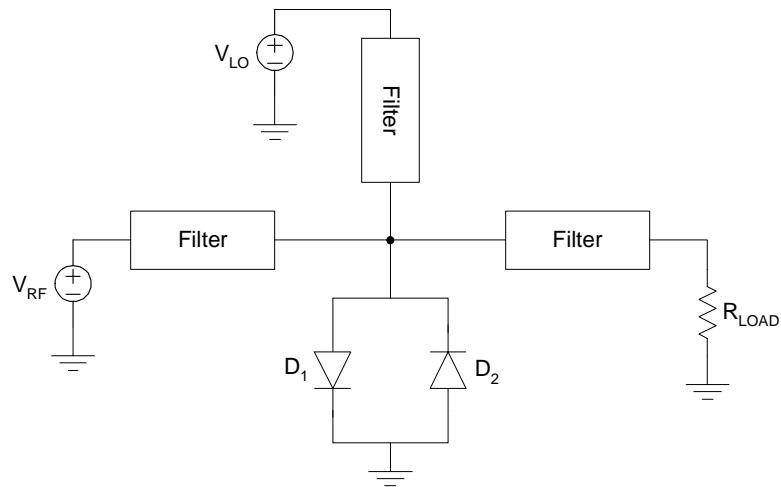


Figure 3.2: Antiparallel diode pair mixer.

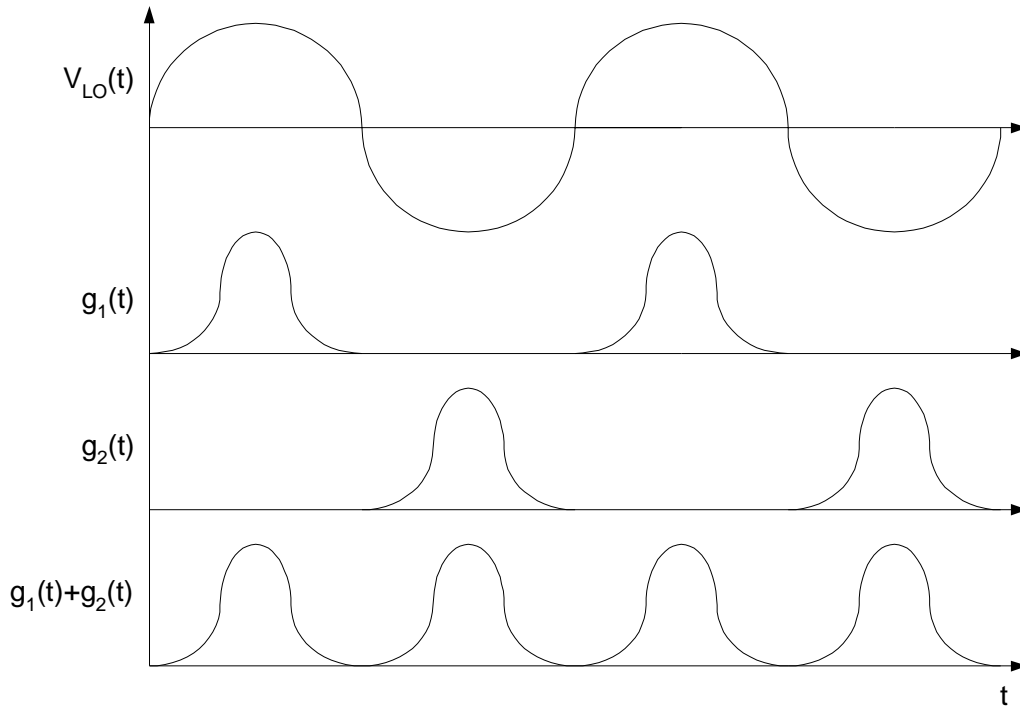


Figure 3.3: Conductance waveforms in an antiparallel diode pair.

The APDP mixer has good linearity performance. However, because it is passive there is a conversion loss, which can be significant. The conversion loss coupled with the shot noise of the diodes causes an APDP mixer to have a fairly high noise figure. Another disadvantage of this type of mixer is that it requires high-quality diodes and thus, is not compatible with a standard CMOS process. The filters required to keep the RF, LO and baseband ports isolated can be troublesome to implement. The RF and LO filters need to be implemented with passive components which are large and may not have a high enough Q to give the required isolation.

3.3 Multi-phase LO mixer

Another way to implement a subharmonic mixer is to use multiple LO signals with the same frequency but phase shifted with respect to each other, and an appropriate switching network. To get a frequency conversion of $N \cdot f_{LO}$, N differential LO signals are

required and they must be phase shifted $180^\circ / N$. Figure 3.4 shows the LO signals and the effective LO signal that the incoming RF signal would be multiplied by for the case where N is equal to 2.

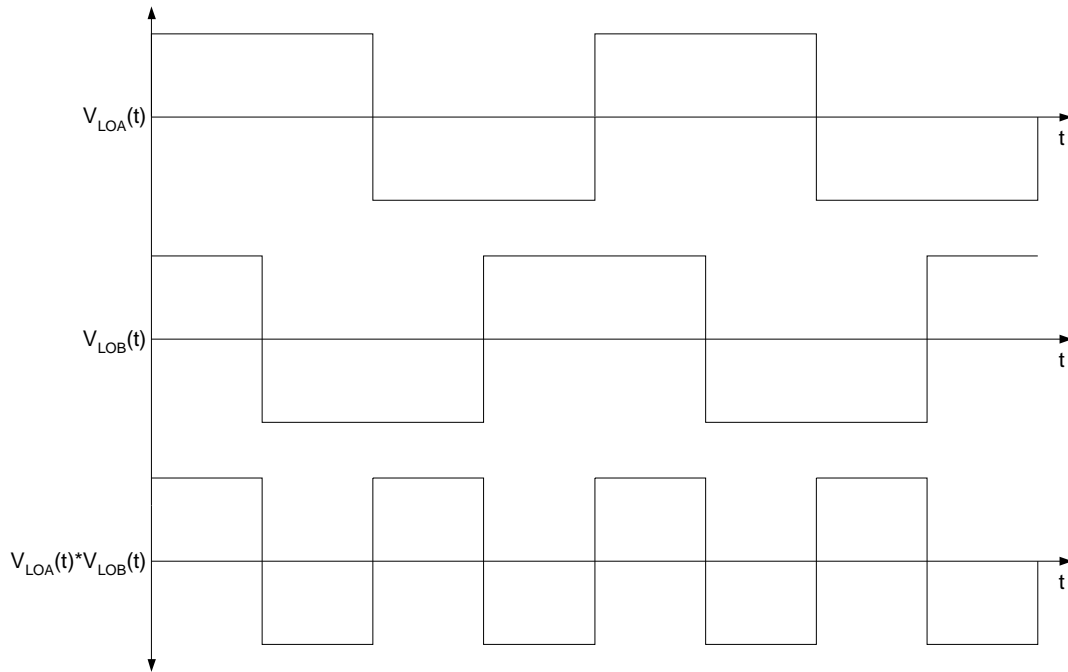


Figure 3.4: LO waveforms for the multi-phase sub-harmonic mixer.

There are two ways to implement the switching network to achieve the desired down-conversion. One way is to use N of the switching network shown in Figure 3.5 connected in series. This switching network is the same as the one used in a double-balanced gilbert mixer. Reference [6] shows another way to implement the switching network. In this scheme there are only two transistors in series between the input and output regardless of N . So for N greater than 2 the latter method would be preferable. For $N=2$ the two methods are almost identical. The architecture in [6], if extended to a double-balanced structure, would have 8 redundant transistors in the switching network when compared to two series switching quads like those of Figure 3.5. Three ways to use the switching network to make a sub-harmonic mixer are discussed below.

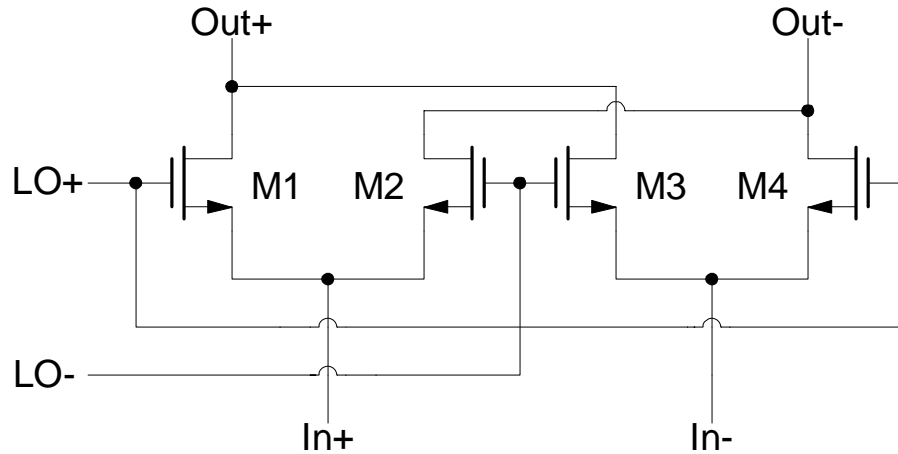


Figure 3.5: A possible switching network.

3.3.1 Passive Multi-phase LO Mixer

One way to make a mixer is to voltage drive the switching network. If this is done, the mixer will operate similarly to a CMOS resistive ring mixer. A detailed analysis of the resistive ring mixer can be found in [7]. A schematic of this type of mixer with $N=2$ is shown in Figure 3.6.

The advantages of this mixer include good linearity, good noise figure and low flicker noise. The reasons for good linearity and noise figure of this mixer are discussed in [7]. This mixer will exhibit low flicker noise because flicker noise is associated with a flow of direct current [8] and the MOS devices have no DC bias current passing through them.

The disadvantages of this mixer are its conversion loss, its need for 2 LO buffers and, depending on the VCO used, the need for a polyphase filter. Since it is passive this mixer has a conversion loss. The fact that it needs two LO signals with different phases causes this mixer to require two LO buffers, which will increase the power consumption of the mixer. Unless a VCO that produces multiple phases is used, this topology will also require a polyphase filter to generate the quadrature LO signals.

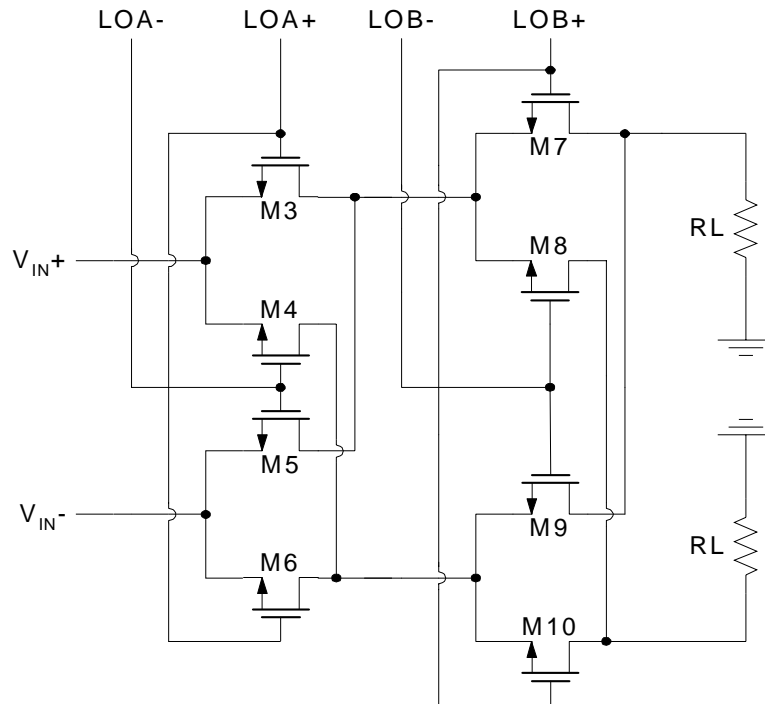


Figure 3.6: Voltage driven CMOS sub-harmonic mixer.

3.3.2 Active Current Commutating Multi-phase LO Mixer

A second way to make a sub-harmonic mixer is to current drive the switching network. A transconductance amplifier can be used to convert the input voltage into a current, which can then be fed into the switching network. If the transconductance amplifier is connected directly to the switching core, the switches will have a DC bias current and will act as common gate current buffers when they are on. A schematic of this type of mixer is shown in Figure 3.7. This topology can also be implemented in bipolar technology [9]. M1 and M2 form the transconductance stage and M3-M10 form the switching cores. The load resistors, RL_+ and RL_- , can be replaced with active loads or some other appropriate load.

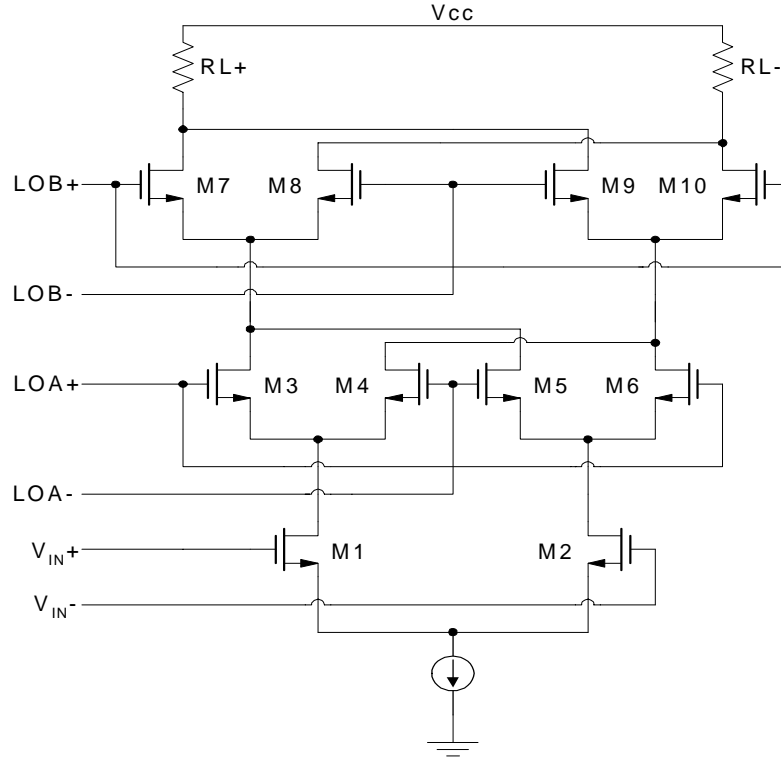


Figure 3.7: Active current commutating sub-harmonic mixer.

The advantages of this type of mixer include its conversion gain, good noise figure and moderate linearity. However, it will need 2 LO buffers and a polyphase filter. Other disadvantages include high flicker noise and restricted DC headroom. The resulting flicker noise in the output band is due to a switch conducting signal and DC bias current, when it is on. There are 3 transistors, a current source and a load between Vdd and ground. The current source may be removed or implemented with a tuned tank to eliminate the voltage drop across the current source. It will still be difficult to bias the three transistors and the load so that there is reasonable swing in the output voltage. This can decrease P_{-1dB} .

3.3.3 Passive Current Commutating Multi-phase LO Mixer

A third way to use the switching network to implement a sub-harmonic mixer is to AC couple a transconductance stage to the core. In this case, the switches act as triode-

region resistors. Unlike the previous case, the core will only commute the signal current. A schematic of this type of mixer is shown in Figure 3.8. Again the load resistors, $RL+$ and $RL-$, can be replaced with active loads or some other appropriate load.

This mixer will have good noise figure, moderate linearity and low flicker noise. Its disadvantages are that it will require 2 LO buffers and possibly polyphase filters. Because of the low flicker noise and the conversion gain this structure is the one best suited to meet the desired specifications.

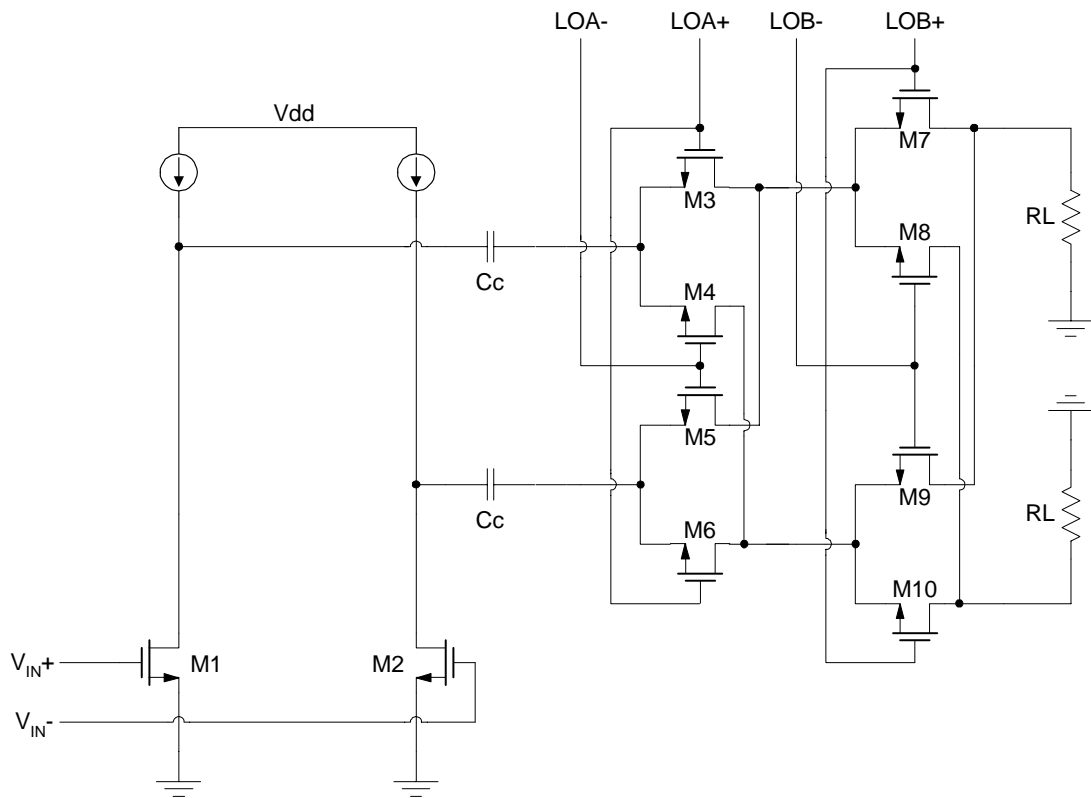


Figure 3.8: Passive current commuting sub-harmonic mixer.

Chapter 4

Analysis and Design

A mixer topology using a transconductor to current drive a switching core made up of passive MOSFET switches was chosen for this project because of its ability to provide a conversion gain and its low level of flicker noise. Since the mixer is being used in a direct-conversion receiver the second-order distortion performance is very crucial. Ideally, differential circuits have no second-order distortion. The rejection of the second order distortion is limited by the matching in the circuit, which can be increased by having a symmetric circuit. The structure shown in Figure 3.7 has an asymmetry. The switching core that is driven by LOA comes first in the signal path, so the circuit is not symmetric. In order to have a symmetric circuit, two separate paths are used in parallel. In one path LOA is encountered first and in the other path LOB is encountered first. Figures 4.1 and 4.2 show the architecture used in this project.

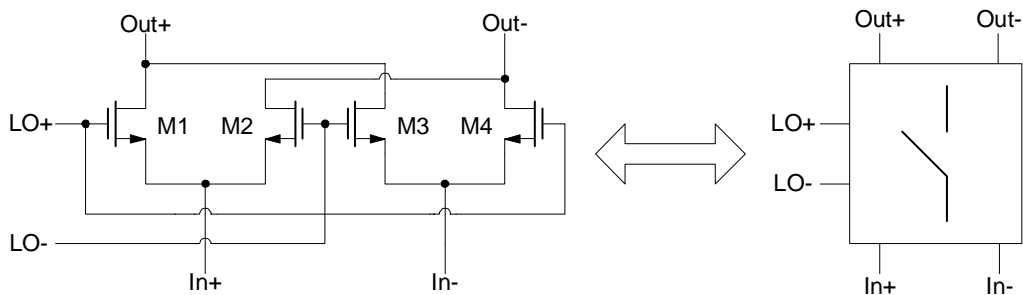


Figure 4.1: Switching core symbol.

Detailed analysis for most of the parameters of interest can be done using the methods in [7]. This analysis is quite complicated and does not result in a closed form solution. Instead, we will focus on what affects the various parameters instead of trying

to calculate them exactly. The analysis will be done separately for the input transconductor and the switching cores, since the former can easily be analyzed using standard techniques while the later requires some modifications because of the time-varying operating point. Analysis of the important specifications follows.

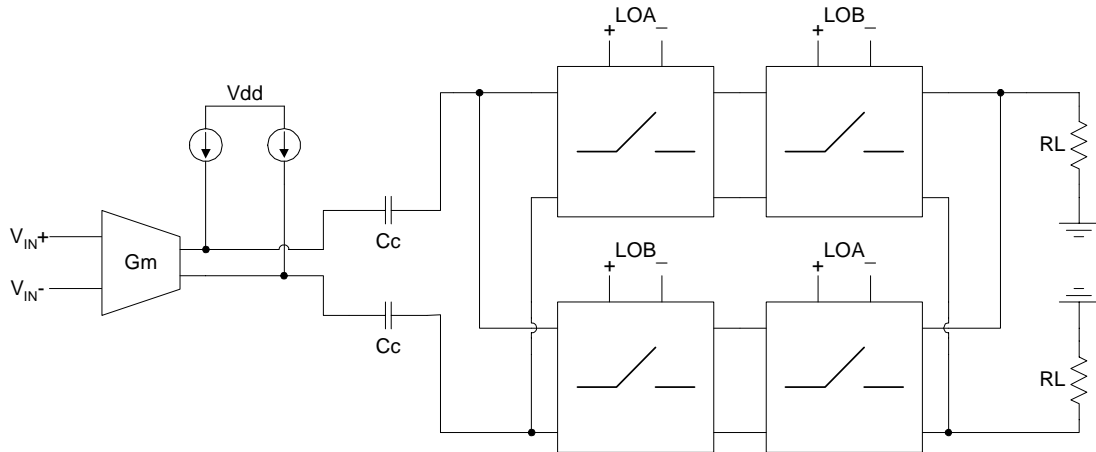


Figure 4.2: Mixer architecture.

4.1 Input Matching

The input transconductor used for this design is shown in Figure 4.3. It is a cascode transconductance stage. The cascode is used to reduce the feedback from the gate-to-drain capacitances of M1 and M2. This reduction improves the stability and the port-to-port isolation of the mixer. The transconductor employs inductive degeneration to improve the linearity and to facilitate input matching. The capacitance (C_A) helps facilitate the input matching, and is used to trade gain for linearity. C_A will be discussed in more detail in sections 4.2, 4.3 and 4.4.

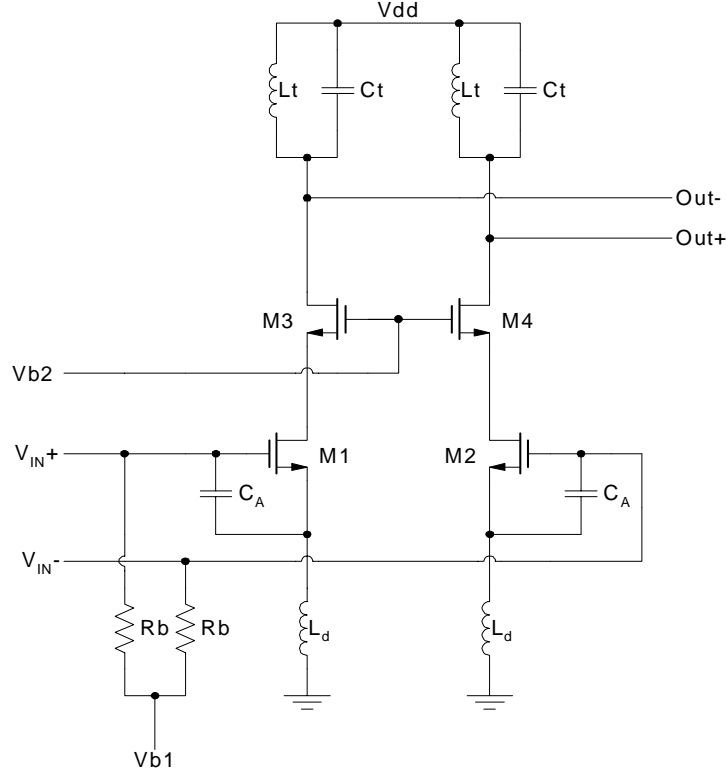


Figure 4.3: Input Transconductor.

As mentioned in Chapter 2, since the mixer is being designed as stand-alone component the input needs to be matched to the source impedance. To design the matching network, first consider the input impedance of the half circuit of the transconductor. Figure 4.4 shows the half circuit and the corresponding small-signal model. The input impedance of the half circuit is

$$Z_{in}(s) = \frac{gm \cdot L_d}{C_{gs} + C_A} + s \cdot L_d + \frac{1}{s \cdot (C_{gs} + C_A)} \quad (4.1)$$

Equation 4.1 shows how C_A assists the impedance matching. With the specified bias and a reasonable degeneration inductor the real part of the input impedance is much larger than the desired value. Therefore, input matching without C_A would require a high-Q

matching network that may have unreasonable component values. This is because the Q of a matching network is approximately equal to the square root of the impedance transformation ratio [10]. Including C_A reduces the real part of the input impedance, which in turn reduces the transformation ratio and the Q required. The rest of the matching network would be implemented off-chip, along with AC coupling caps, C_C . The external matching network consists of an L-match section and a 2:1 balun. A schematic of the off-chip circuitry is shown in Figure 4.5.

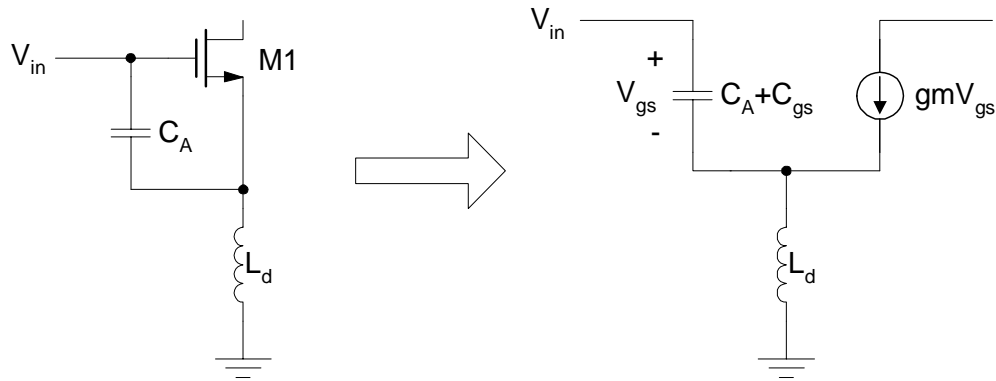


Figure 4.4: Transconductor half-circuit and the corresponding small-signal model.

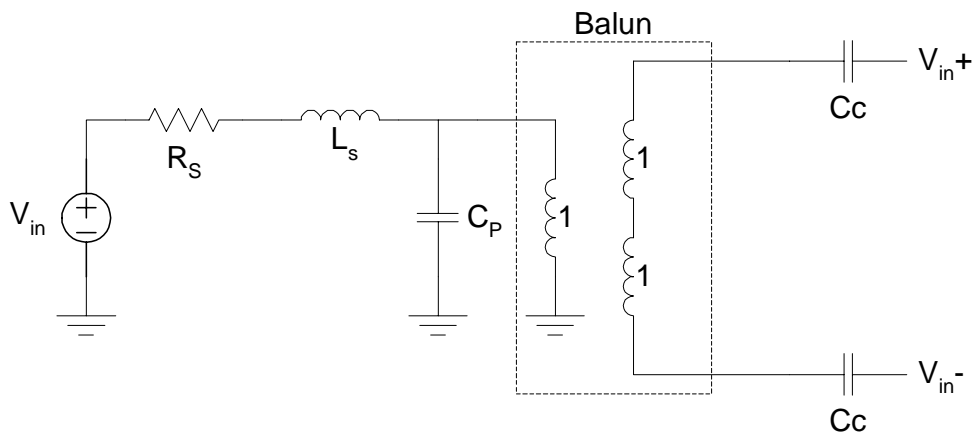


Figure 4.5: Off-chip matching network.

4.2 Conversion Gain

Since a mixer has a time-varying operating point, the conversion gain is significantly more complicated to analyze than the gain of a linear amplifier [7]. The conversion gain of this mixer can be approximated by assuming the MOS switches commute the current with a square wave transfer function. If this is the case and the tank has a high impedance, the voltage conversion gain would be

$$VCG = Gm \cdot \frac{2}{\pi} \cdot R_L \quad (4.2)$$

where Gm is the transconductance of the input stage and $2/\pi$ comes from the square wave switching function.

As shown in Equation 4.2, the effective transconductance of the input stage is important in determining the conversion gain. In general, an increase in Gm will increase the conversion gain. Increasing the bias current or decreasing the degeneration will increase the conversion gain. Increasing the device size will also increase the conversion gain, providing that the increase in parasitic capacitances do not degrade the frequency response.

The capacitance C_A can also be used to affect the conversion gain. It was mentioned in section 4.1 that the Q of the matching network can be decreased by increasing C_A . For an L-match (Figure 4.6) there is a voltage gain from V_A to V_B . Which can be described by

$$\frac{V_B}{V_A} = \frac{Z_{CP} \parallel Z_L}{Z_{CP} \parallel Z_L + Z_{LS}} \quad (4.3)$$

Where Z_{CP} , Z_{LS} , and Z_L are the complex impedances of the capacitor, inductor and load. Since the input is matched, Z_1 is equal to the complex conjugate of Z_2 . This leads to the following equation.

$$Z_2 = Z_{CP} \parallel Z_L = Z_1 = R_S - Z_{LS} \quad (4.4)$$

Substituting 4.4 into 4.3 gives

$$\frac{V_B}{V_A} = \frac{R_S - Z_{LS}}{R_S - Z_{LS} + Z_{LS}} \quad (4.5)$$

Simplifying 4.5 gives

$$\frac{V_B}{V_A} = 1 - \frac{Z_{LS}}{R_S} \quad (4.6)$$

Taking the magnitude of 4.5 leads to

$$\left| \frac{V_B}{V_A} \right| = \sqrt{1 + \left(\frac{Z_{LS}}{R_S} \right)^2} = \sqrt{1 + Q^2} \quad (4.7)$$

where Q is the quality factor of the matching network. Since the small signal output current of a MOSFET is proportional to the small signal gate voltage, this voltage gain will show up as a multiplicative factor in the transconductance of the input stage.

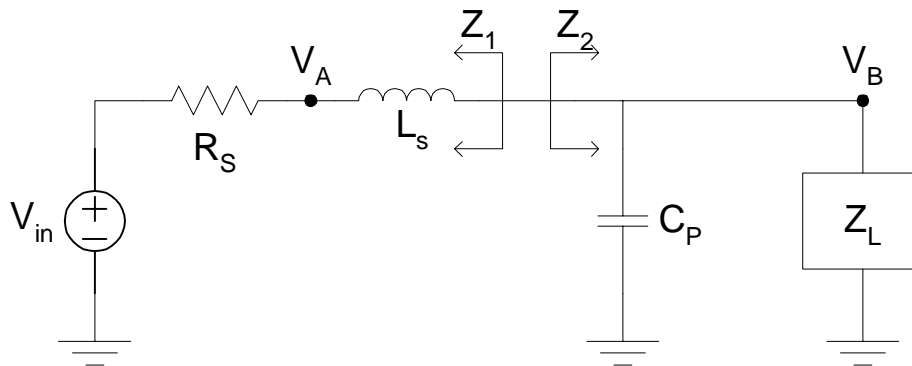


Figure 4.6: L-match network.

Since the switching function is not a perfect square wave and the impedance of the on-chip tank at resonance is not much larger than the load resistance, Equation 4.2 is not a good approximation for the conversion gain. Figure 4.7 is helpful in understanding the conversion gain of the mixer. It represents what the circuit looks like when two switches connect the transconductor to the load and the other switches have a high enough off-resistance to be neglected. R_{S1} and R_{S2} represent the on-resistance of the MOS switches and C_{P1} and C_{P2} represent the parasitic capacitance at each node. If we first consider the idealized case, where the parasitic capacitances don't affect the circuit, and the tank has an infinite impedance at the frequency of interest, the conversion gain would be unaffected by the on resistance of the switches. However, since the tank is implemented with on-chip components, the Q of the inductor will limit the tank impedance at resonance. Also the load resistance is high enough that the parasitic capacitances cannot be neglected. Because of the tank, the signal current will see a current divider formed by Z_T and $Z_{CP1} \parallel Z_1$. The signal current will then see a current divider caused by C_{P2} . The signal current that reaches the load is given by

$$I_L = G_m \cdot \frac{Z_T \parallel Z_{CP1}}{Z_T \parallel Z_{CP1} + Z_1} \cdot \frac{Z_{CP2}}{Z_{CP2} + R_{S2} + R_L} \quad (4.8)$$

where

$$Z_1 = R_{S1} + Z_{CP2} \parallel (R_{S2} + R_L) \quad (4.9)$$

To maximize the conversion gain, the parasitic capacitance C_{P1} due to the switches should be tuned out, at the input frequency, using the tank. The parasitic capacitance, C_{P1} , is the reason a tank was used. If a large resistor or an active device were used to implement the current source, C_{P1} would put a pole, which is lower than the signal

frequency, in the conversion gain. $Z_T || Z_{CP1}$ should be kept as high as possible to ensure that the signal current passing through the tank is minimized. Equation 4.10 shows that the impedance of a parallel tank at resonance increases with both the inductance value and the Q factor.

$$R_p = 2\pi \cdot f \cdot L_T \cdot Q \quad (4.10)$$

This means that a large valued inductance with a reasonable Q should be used in the tank. Another important factor in the conversion gain is to minimize Z_1 while keeping C_{P2} as small as possible. To do this, R_{S1} and R_{S2} should be kept low. R_{S1} and R_{S2} can be described by Equation 4.11.

$$R_{ON} = \frac{1}{Kn \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS})} \quad (4.11)$$

R_{ON} and can be lowered by increasing the device size or by increasing the LO drive. However, increasing the device size increases C_{P1} , C_{P2} and the gate capacitance of the switches. The increase in parasitics can decrease the conversion gain. The increase in gate capacitance will increase the power consumption of the LO buffer for a given LO drive level. Increasing the LO drive will only increase the power consumption of the LO buffer.

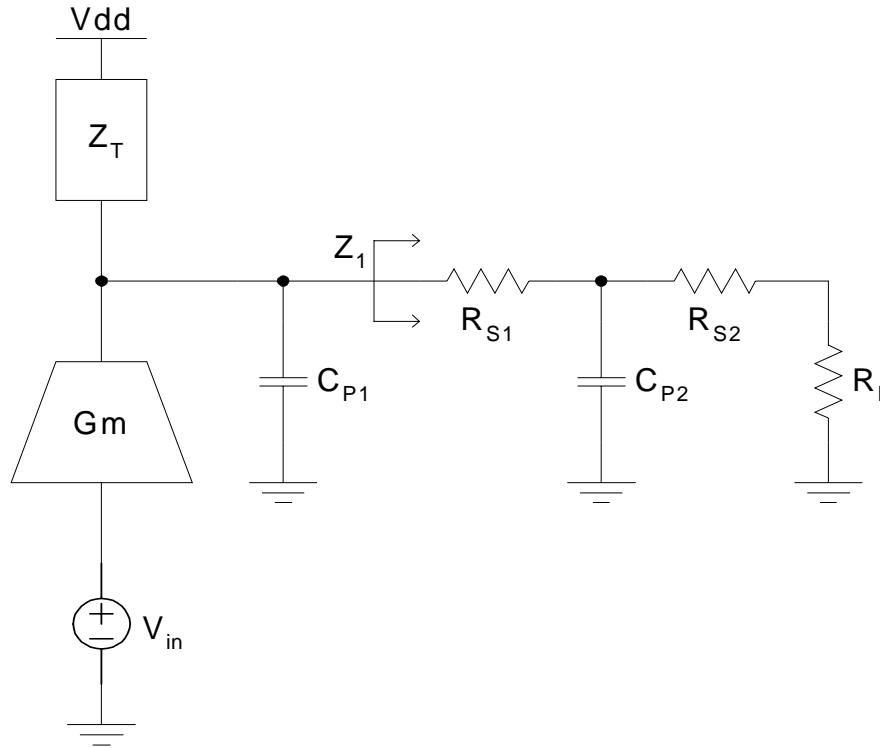


Figure 4.7: Small signal model for the mixer.

4.3 Noise Figure

The noise in the input transconductor can be analyzed using standard linear-time-invariant analysis. This analysis for a matched common source stage, such as the one used in this design, has been done in [4]. The guidelines for minimizing the noise figure given in [4] are a) Maximize the unity gain frequency by choosing small width devices biased at high current density and b) Pick a degeneration inductor that gives a feedback factor ($g_m \cdot \omega \cdot L_d$) approximately equal to 0.5.

The switching core also makes a contribution to the noise figure. For noise analysis, a CMOS device operating in the triode region can be modeled as a resistor equal

to the channel resistance. Neglecting C_{P2} , it can be shown that the noise power at the output due to a switch is given by

$$N_O = 4KT \cdot R_{S1} \cdot \left| \frac{R_L}{R_L + R_{S1} + R_{S2} + Z_T \parallel Z_{CP1}} \right|^2 \quad (4.12)$$

The noise contribution from a switch can be reduced by decreasing its on-resistance. As mentioned in section 4.2, this can be accomplished by increasing either the device size or the LO drive.

The noise figure for two stages that are cascaded can be described by

$$NF_{EQ} = NF_1 + \frac{NF_2 - 1}{G_1} \quad (4.13)$$

where NF_1 and NF_2 are the noise figures of the 2 stages and G_1 is the power gain of the first stage. Equation 4.13 shows that another way to reduce the effect the switching cores have on the noise figure is to increase the gain of the transconductance stage. This increase in gain will lower the noise figure. In section 4.2 it was mentioned that increasing the switch width can decrease the conversion gain because of the parasitic capacitances. This explains why increasing the switch size decreases the noise at the output due to the switches but increases the overall noise figure.

4.4 Distortion

The input transconductor is composed of a pair of differentially driven common source stages with inductive degeneration. The distortion in this stage follows the same trends as a common source stage but the second order terms cancel out. To understand why this is the case, consider that each common source has a power series that relates its output current to the input voltage that is given by

$$i_o = a_1 v_g + a_2 v_g^2 + a_3 v_g^3 + \dots \quad (4.14)$$

where v_g is the AC gate voltage. The input differential voltage, V_i , can be broken up into a bias component, V_I , and an AC component, v_i .

$$V_i = V_I + v_i \quad (4.15)$$

Since the input is being driven differentially the input ac voltage at the gates of M1, v_{g1} , and M2, v_{g2} , can be expressed as

$$v_{g1} = \frac{v_i}{2} \quad (4.16)$$

$$v_{g2} = -\frac{v_i}{2} \quad (4.17)$$

The differential ac output current is the difference between these two power series. This difference results in

$$i_o = i_1 - i_2 = a_1 v_i + \frac{1}{4} a_3 v_i^3 + \dots \quad (4.16)$$

Equation 4.16 shows that the input transistor will have third order distortion components that are one fourth as big as those for a common source transistor.

The distortion performance of the common source transconductance stage has been thoroughly analyzed in [4]. The distortion metric of interest is the third-order input intercept point. It was shown in [4] that for a conjugately matched common source, the IIP_3 can be reduced by either increasing the bias current or by increasing the degeneration.

If the tank impedance was very high at its resonance frequency, all the signal current that comes from the transistor would pass through the switches and the load. If this were the case, the fact that the switch on-resistance changes with signal level

would not effect the amount of signal current passing through the switches, and thus the switching core would have almost no effect on the distortion performance of the mixer. However, since the tank impedance is comparable to the impedance of the switches plus the load impedance, the switching core does produce distortion. The distortion performance of MOSFETs used as passive switches was studied in [7]. It was shown that the third-order distortion comes entirely from second order interaction, and reducing the non-linear voltage drop across the switches would reduce the distortion. For this reason there are two ways to reduce the distortion of the switching core. One of them is to increase the LO drive, which will lower the on resistance of the switches. The other one is to increase the device size. The latter method was shown in to be less effective [7].

Considering the interaction between the two stages, there is another way to reduce the overall distortion of the mixer. If the effective transconductance of the input stage is reduced, the signal current fed into the switches will be reduced for a given input power. This would reduce the voltage drop across the switches and thus increase IIP_3 .

4.5 Mixer Design

The trends for the important specifications were discussed in section 4.1 through 4.4. These trends were used to optimize this mixer design for the desired specifications.

As the LO drive level and the transconductor bias current are increased, conversion gain, noise figure and IIP_3 are all improved. Only power consumption is negatively impacted by these factors. Since there is no performance degradation for increases in LO drive and bias current, they were made as large as possible. The LO drive was chosen to be as close to a rail-to-rail square wave as possible. Since there is an input LO power specification, an LO buffer was designed to amplify the input LO signal

to give the desired LO drive. The transconductance stage was biased with its full current budget.

The most important trade-off in this design, as with most mixers, was between noise figure and distortion. As discussed in section 4.3, the effect of noise due to the switching core has on the overall noise figure can be reduced by increasing the gain of the input stage. This results in an increase in conversion gain. The input stage gain also has an effect on the distortion of the mixer. An increase in input stage gain results in a larger signal current passing through the switches, which in turn increases, the distortion level at the output of the mixer. This shows that changing the input stage gain, and thus the overall conversion gain, is one way to trade noise performance for distortion performance.

The devices used in the input transconductor show significant short channel effects and thus have considerable third order non-linearity. Simulations show that with the chosen bias current, a large degeneration inductance is necessary to achieve the desired distortion performance. The choice of device sizes in the input stage took into account the relationship between G_m and size as well as the relationship between parasitics and size. C_A (Figure 4.3) was selected as an optimum based on the trade off between noise figure and distortion that it allows through its effect on the conversion gain.

For the choice of the device size in the switching core, consider the following. It was mentioned in section 4.2 that a large inductance should be used in the tank in order to allow large impedance when the tank is at resonance. A large inductance means a smaller capacitance is needed for resonance. Since it is not a good idea to have the entire tank capacitance due to the device parasitics [10], the devices should be kept small to

allow for resonance with a reasonable tank capacitance. It was also mentioned in section 4.2 that C_{P2} should be kept small, which also encourages the use of small devices. The limit on how small the devices can be is set by the need to keep the on-resistance low and the desire for good matching between the devices.

4.6 LO Buffer Design

The LO buffer takes the LO input signal and conditions it to give the desired waveform to drive the mixer's switches. As mentioned in sections 4.2, 4.3 and 4.4, the larger the LO amplitude the better the performance of the mixer. Ideally the switches should be driven with as close to a square wave as possible. The buffer is designed to provide an approximately a rail-to-rail square wave signal. The specified LO input power is -10dBm in 50Ω . This corresponds to 100mV peak sine wave. However, the LO input would first drive a polyphase filter in order to give the quadrature LO signals. These filters would introduce some loss in the LO path, so the LO buffer was designed to work with input signals as low as 50mV peak.

This first stage of the LO buffer is shown in Figure 4.8. It consists of a differential pair formed by M1 and M2 with active loads formed by M4-M6. M1A, M3A, M5A and M7A form a replica-bias circuit. M7A is ten times smaller than M7 and M1A, M3A and M7A are all five times smaller than M1, M3 and M7 respectively. M5, M6 and M5A are operating in the triode region and the remaining devices are saturated. Because of the replica bias, M5 and M5A will have the same gate to source voltage. This is a convenient way to set the common-mode voltage at the output of the gain stage. The common-mode points are set to the switching point of the inverters that follow the analog gain stages. A replica of the inverter stages formed by M8 and M9 sets the gate voltage of M5A to be at the inverter's threshold. C_P is used to make the gate of M5A an AC

Each stage is AC coupled to the next so the LO buffer will function properly even if the devices are not perfectly matched. With some finite mismatch in the devices, each gain stage will have an equivalent DC offset at its input. Consider the offset at the input of the first stage. This offset will see the DC gain of the amplifier and show up as a larger offset at the output. If the stages were directly coupled, this offset would be input to the second stage and it would see the gain of the second stage. This can result in a very large DC offset at the output of the second stage. Mismatch simulations show that with direct coupling between the stages it is possible for the offset to be so large that the first inverter stage would not switch states with the input signal. Instead it would have an output that is always stuck at the positive power supply or ground.

Chapter 5

Performance and Conclusions

The mixer discussed in this project was designed to be implemented in a commercially available 0.25 μ m CMOS process from National Semiconductor. It was simulated using SpectreRF. The inductors were designed and simulated with ASITIC [11], [12] and their pi models were used in SpectreRF. The important specifications and the simulation results are summarized in the table below.

	<u>Specification</u>	<u>Simulation</u>
Voltage conversion gain	≥ 0 dB	8 dB
Power conversion gain	≥ -6 dB	2 dB
DSB NF	≤ 7 dB	6.4 dB
IIP ₃	≥ 4 dBm	5.28 dBm
Output P _{-1dB}	≥ 0.8 Vppk	0.96 Vppk
IIP ₂	≥ 40 dBm	61 dBm (1 σ) 46 dBm (3 σ)
2 · LO leakage to input	-85 dBm	-97 dBm (1 σ) -77 dBm (3 σ)
LO input power	-10 dBm	-10 dBm
Core current consumption	3 mA	3 mA
LO buffer current consumption @ 1 GHz		5.1 mA

The following four sections describe some important aspects of the simulations.

5.1 Noise Figure

The noise figure was simulated using SpectreRF's periodic steady state analysis. The noise figure specified above was calculated using Equation 2.11, to include the effect that flicker noise in the output spectrum would have on the receiver. The simulations showed the flicker noise present in the output spectrum was due to the flicker noise of the devices in the switching core. Measurements and theoretical work have shown that devices with switched bias conditions show reduced flicker noise when compared to the standard $1/f$ noise model [13], [14], [15]. SpectreRF uses the standard stationary process model for $1/f$ noise so the quoted noise figure may include flicker noise that would not be present if the mixer were fabricated.

5.2 Mismatch

In order to keep the second order distortion and the $2 \cdot \text{LO-to-RF}$ feed through as low as possible, this mixer is fully differential. If all the elements were perfectly matched, the second order distortion and $2 \cdot \text{LO-to-RF}$ feedthrough would be zero. However, in a real-world circuit there are always mismatches between devices. Therefore some finite amount of the two undesired signals would be present. It is extremely difficult to analyze and simulate these effects because the mismatch among the devices is random. The best way to simulate mismatch is to perform a Monte-Carlo simulation. In this analysis a simulation is run many times while the key parameters are randomly varied in a manner that approximates the real process variations. This was done using foundary specified mismatch parameters. These were a 3% per square root of W·L width mismatch, a 1% per square root W·L threshold mismatch and a 5% mismatch for resistors and capacitors. The simulations for IIP_2 and $2 \cdot \text{Lo}$ feedthrough were done 50 times and the results are shown in Figures 5.1 and 5.2. IIP_2 and $2 \cdot \text{Lo}$ feedthrough values

for 3 standard deviations and 1 standard deviation away from the mean are specified in the table above.

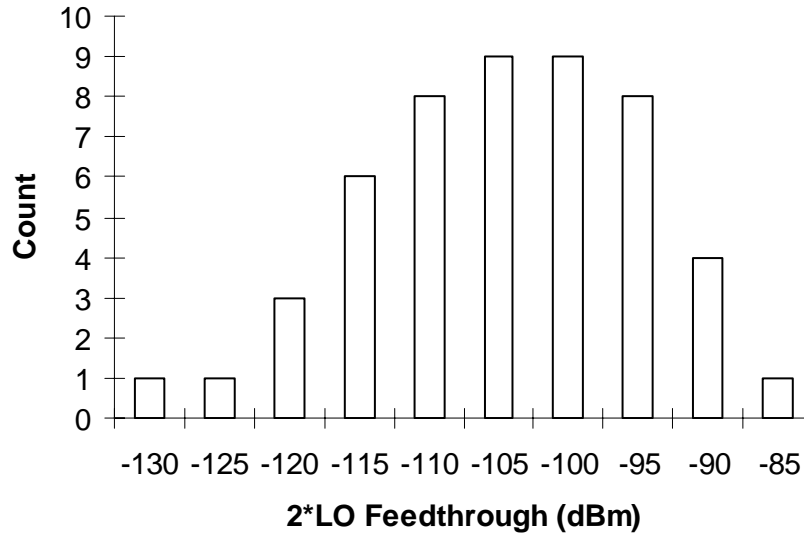


Figure 5.1: Histogram of 2·LO Feedthrough.

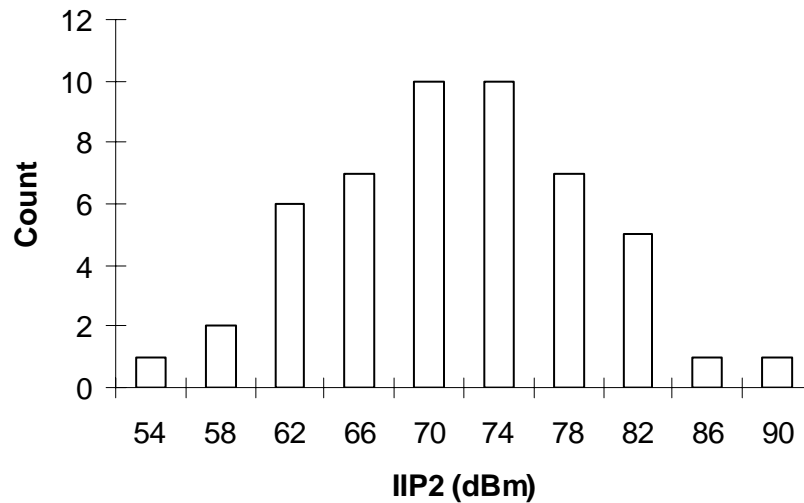


Figure 5.2: Histogram of IIP₂.

5.3 LO Phase

It was mentioned in chapter 3 that the mixer topology used in this project might require a polyphase filter to generate the quadrature LO signals. This filter was not

designed here and was not included in the simulations. To ensure that the mixer would work with a real polyphase filter, the effect of imperfect quadrature was simulated. There was no significant decrease in mixer performance for LO inputs that were out of quadrature by 10° .

5.4 Common Mode Bias

The load used in the simulations was used to model the next stage of the receiver chain. This block would require a common-mode feedback circuit to control its input common-mode bias point. For this mixer, the ideal value of this common-mode point is $V_{dd}/2 - V_{TH}$. This bias point puts the switches in the core on the verge of conduction when the LO input is $V_{dd}/2$. $V_{dd}/2$ is the common-mode output of the LO buffer. This arrangement produces the optimum switching function for the switching cores. In the simulations this optimum bias was set ideally because the common-mode feedback of the following stage was not designed. To ensure that the mixer could operate properly with a real common-mode feedback circuit, the mixer was simulated with different output common-mode points. For common-mode shifts of 100mV from the optimum point, there was very little degradation in the mixer's performance. The conversion gain and noise figure were unchanged. The IIP_3 decreased to 4.77dBm for a 100mV increase in the output common-mode point.

5.5 Conclusions

The mixer designed here achieved all of the desired specifications except for the $2 \cdot LO$ feedthrough. However the $2 \cdot LO$ feedthrough specification was given for a 3σ yield. If a 2σ yield is acceptable then the $2 \cdot LO$ feedthrough is within the desired range. Using this topology, a moderate IIP_3 and a good noise figure were achieved along with a conversion gain. The mixer achieves these specifications with two shortcomings. First

the need for two LO buffers coupled with the significant power consumption of each buffer leads to a high overall power consumption. The second problem is the need for the large inductors with a reasonable Q factor. These inductors require a large area. In this design, the necessary inductors were 250 μ m on each side.

5.6 Future Work

One of the major difficulties in this design was the parasitic capacitance of the switches. This problem could be alleviated if a lower load impedance was used. This could be accomplished by using a transimpedance amplifier (TIA) to drive the load [16]. Since the input impedance of a TIA is low, the signal current would prefer that path to the one consisting of the parasitic capacitances. Since the desired signal is at baseband with a bandwidth of 2MHz, a low frequency op-amp could be used in the amplifier. If a TIA were used, there would be an increase in power consumption. To ensure that the noise and distortion performance of the mixer weren't limited by the TIA it must be designed carefully. This idea was not investigated in depth here but could prove to be beneficial for a mixer of the type presented here.

Appendix

Component Values

Off-chip Components (Figure 4.5)

Ls	5.34nH
Cp	0.42pF
Cc	100pF

Input Transconductor (Figure 4.3)

M1=M2=M3=M4	60 μ m/0.25 μ m
Ld=Lt	8nH
Ct	0.34pF
C _A	100pF
Rb	10k Ω

Switching Cores (Figure 4.1)

M1=M1=M3=M4	10 μ m/0.25 μ m
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LO Buffer Stages 1 and 2 (Figure 4.8)

M1=M2	30 μ m/0.25 μ m
M3 =M4=M5 =M6	20 μ m/0.25 μ m
M7	50 μ m/0.25 μ m
M1A	6 μ m/0.25 μ m
M3A	4 μ m/0.25 μ m
M7A	5 μ m/0.25 μ m
M8	1 μ m/0.25 μ m
M9	3 μ m/0.25 μ m
Cp	1pF
Cc	0.22pF
Rb	10k Ω

LO Buffer Stages 3 and 4 (Figure 4.9)

M1=M2	3 μ m/0.25 μ m
M3=M4	9 μ m/0.25 μ m
M5=M6	10 μ m/0.25 μ m
M7=M8	30 μ m/0.25 μ m
Cc	0.22pF
Rb	10k Ω

Bibliography

- [1] A. Abidi, *Direct-Conversion Radio Trancievers for Digital Communications*, IEEE Journal of Solid-State circuits, Vol. 30, No. 12, December 1995.
- [2] K. L. Fong, *Design and Optimization Techniques for Monolithic RF Downconversion Mixers*, PhD thesis, University of California, Berkeley, 1997.
- [3] A. Parssinen, J. Jussila, J. Ryyanen, L. Sumanen, and K. A. I. Halonen, *A 2-GHz Wide-Band Direct Conversion Reciever for WCDMA Applications*, IEEE Journal of Solid-State circuits, Vol. 34, No. 12, December 2000.
- [4] E. Terrovitis, *Analysis and Design of Current-Commutating CMOS Mixers*, PhD thesis, University of California, Berkeley, 2002.
- [5] S. A. Maas, *Microwave Mixers, Second Edition*, Artech House, 1993.
- [6] K. Lee, J. Park, J-W Lee, S-W Lee, H. K. Huh, D-K Jeong, and W. Kim, *A Single-Chip 2.4-GHz Direct-Conversion CMOS Reciever for Wireless Local Loop using Multiphase Reduced Frequency Conversion Technique*, IEEE Journal of Solid-State circuits, Vol. 36, No. 5, May 2001.
- [7] S. W. Son, *High Dynamic Range CMOS Mixer Design*, PhD thesis, University of California, Berkeley, 2002.

[8] P. Gray and R. Meyer, *Analysis and Design of Analog Integrated Circuits, Third Edition*, Wiley, 1993.

[9] L. Sheng, J. Jensen, and L. Larson, *A Si/SiGe HBT Sub-harmonic Mixer/Downconverter*, IEEE Proceedings of the 1999 Bipolar/BiCMOS Circuits and Technology Meeting.

[10] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 1998.

[11] A. M. Niknejad and R. G. Meyer, *Analysis, Design, and Optimization of Spiral Inductors and Transformers for Si RFIC's*, IEEE Journal of Solid-State circuits, Vol. 33, No. 10, October 1998.

[12] ASITIC: *Analysis of Si Inductors and Transformers for IC's*, <http://www.eecs.berkeley.edu/~niknejad>.

[13] E. A. M. Klumperink, S. L. J. Gierkink, H. Wallinga, and B. Nauta, *Reduction of 1/f Noise in MOSFETs by Switched Bias Techniques*, Proceedings of the 9th IEEE/ProRISC Workshop on Circuits, Systems and Signal Processing, 1998

[14] S. L. J. Gierkink, E. A. M. Klumperink, E. van Tuijl, B. Nauta, *"Switched Biasing" Reduces both MOSFET 1/f Noise and Power Consumption*, Proceedings of the 9th IEEE/ProRISC Workshop on Circuits, Systems and Signal Processing, 1999

[15] S. L. J. Gierkink, E. A. M. Klumperink, A. P. van der Wel, G. Hoogzaad, E. A. J. M. van Tuijl, and B. Nauta, *Intrinsic 1/f Device Noise Reduction and Its Effect on Phase Noise in CMOS Ring Oscillators*, IEEE Journal of Solid-State Circuits, Vol. 34, No. 7, July 1999.

[16] J. Crols and M. S. J. Steyaert, *A 1.5GHz highly Linear CMOS Downconversion Mixer*, IEEE Journal of Solid-State circuits, Vol. 30, No. 7, July 1995.

[17] E. E. Bautista, B. Bastani, and J. Heck, *A High IIP2 Downconversion Mixer Using Dynamic Matching*, IEEE Journal of Solid-State Circuits, Vol. 35, No. 12, December 2000.