

Modeling of Passive Elements with ASITIC

Prof. Ali M. Niknejad

Berkeley Wireless Research Center

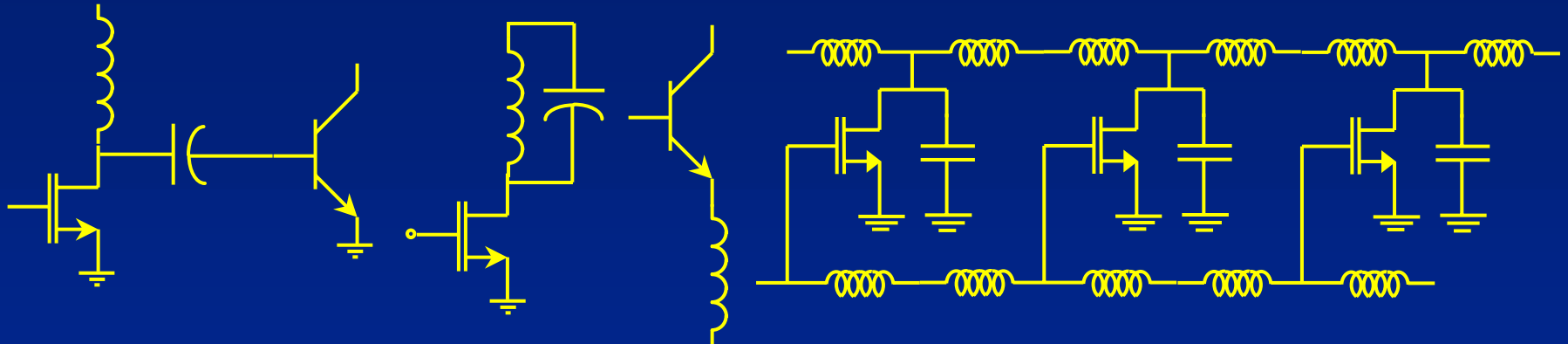
University of California, Berkeley



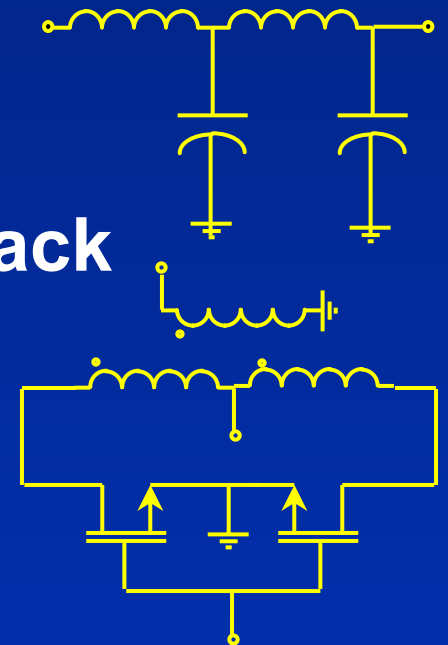
Outline of Presentation

- **ASITIC Overview**
- **Electromagnetic Solution Approach**
- **Partial Inductance Matrix**
- **Eddy Current Losses**
- **Capacitance Matrix**
- **Experimental Validation**
- **Broadband Modeling**
- **Limitations and Future of ASITIC**

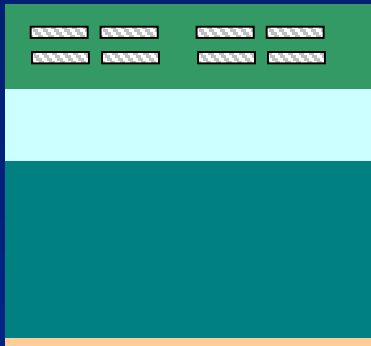
Applications of Passives for RFICs



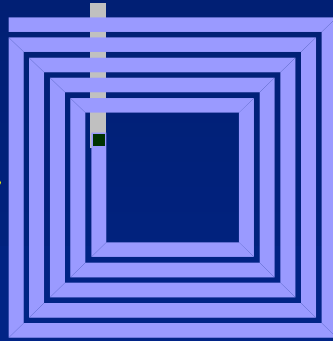
- **Narrow-band impedance matching**
- **Tuned loads (resonant tank)**
- **Low noise degeneration and feedback**
- **Natural/artificial transmission lines**
- **Linear filters (high dynamic range)**
- **Fully differential circuits**
- **Low voltage/low power design**



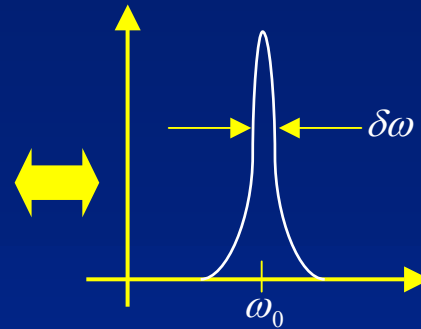
The Goal of ASITIC



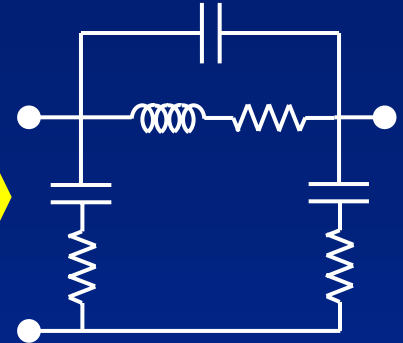
Technology File



Layout



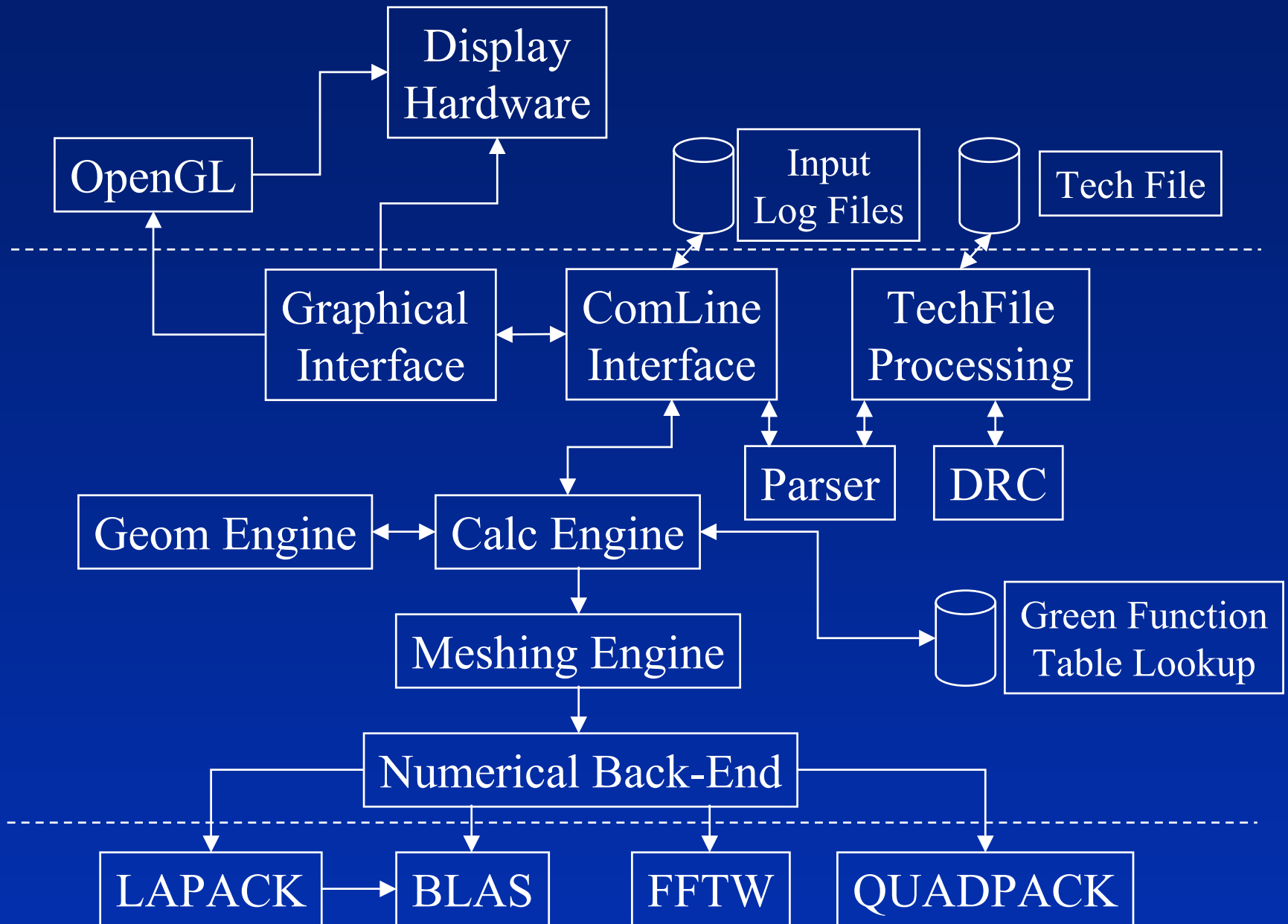
Electrical Specs



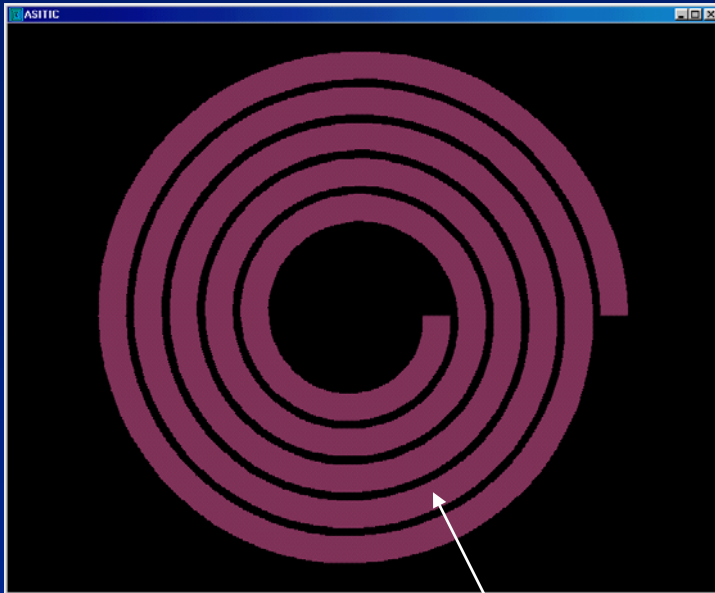
Model

- Solve the *analysis*, *design*, and *modeling* problems
- Achieve *accuracy* over a wide frequency range
- Perform analysis of structures *quickly* for optimization
- Retain *flexibility* to work with arbitrary structures
- Create a *design environment*
- Generate *simple compact models*

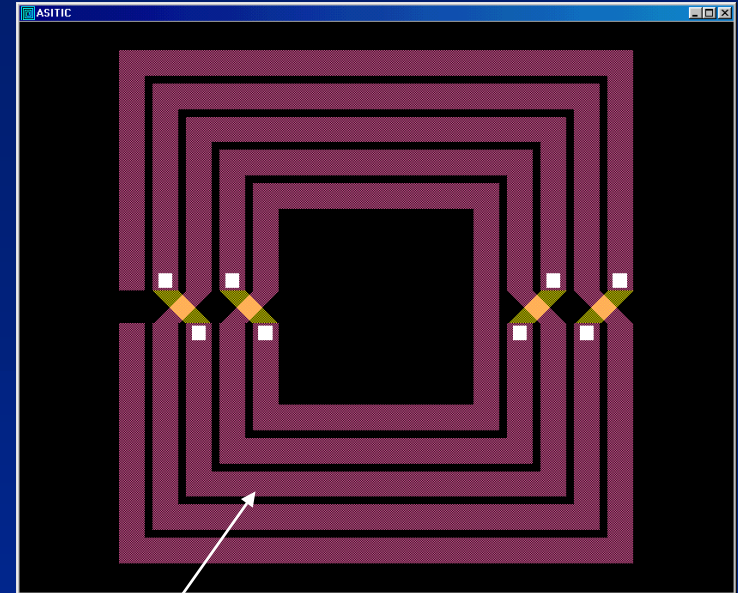
ASITIC Block Diagram



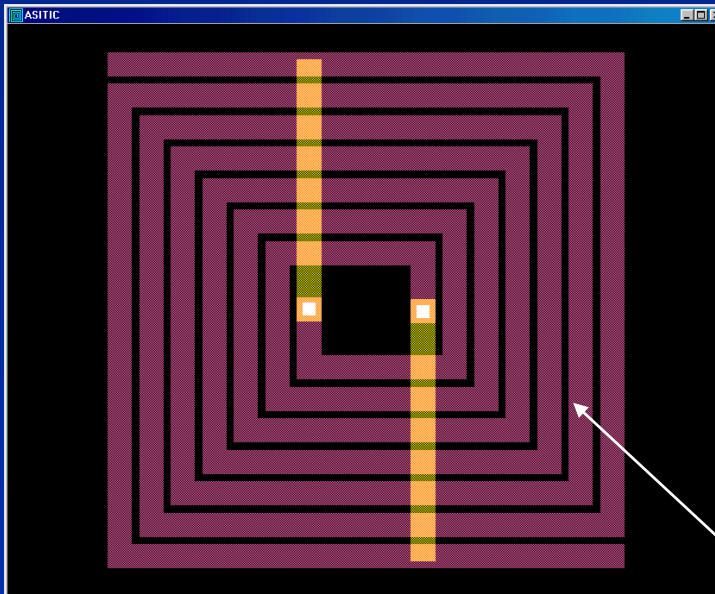
Planar Inductor/Transformer Layout



circular spiral inductor

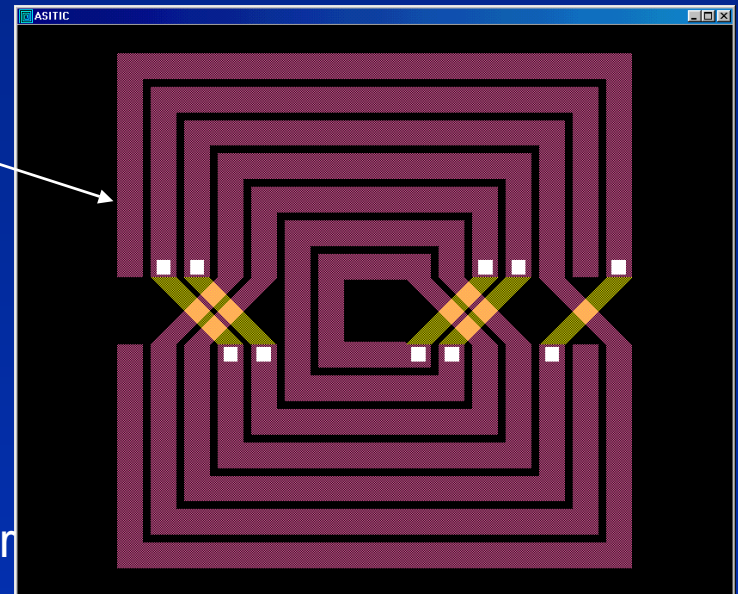


symmetric center-tapped



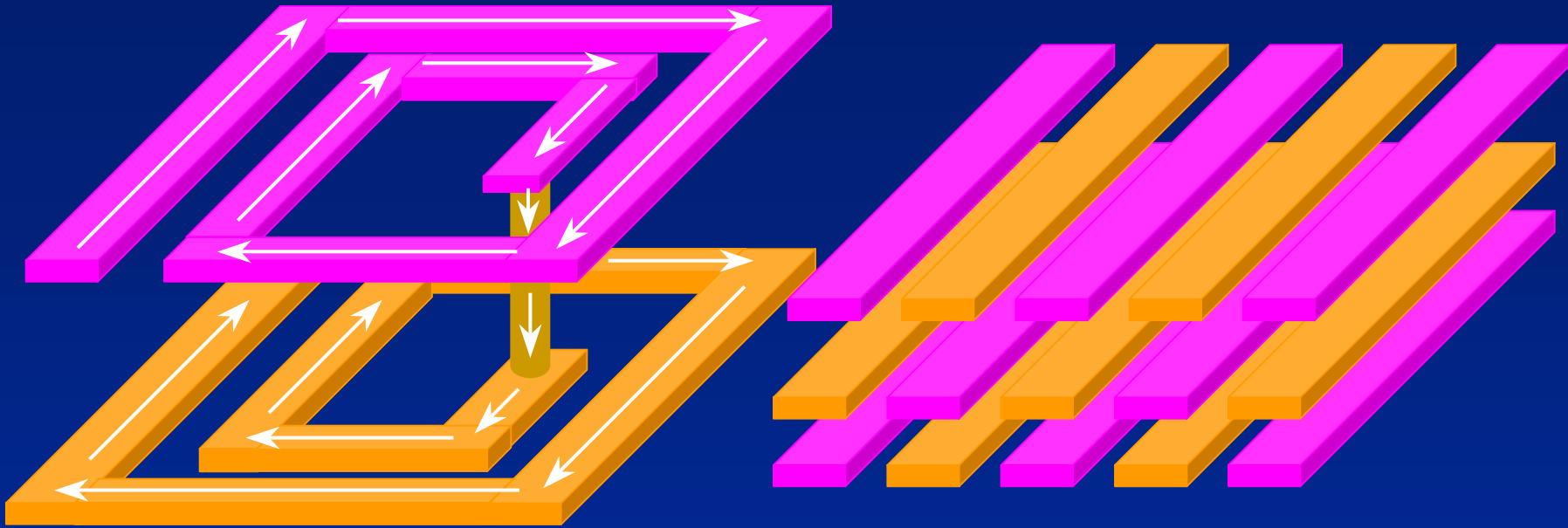
transformer

balun



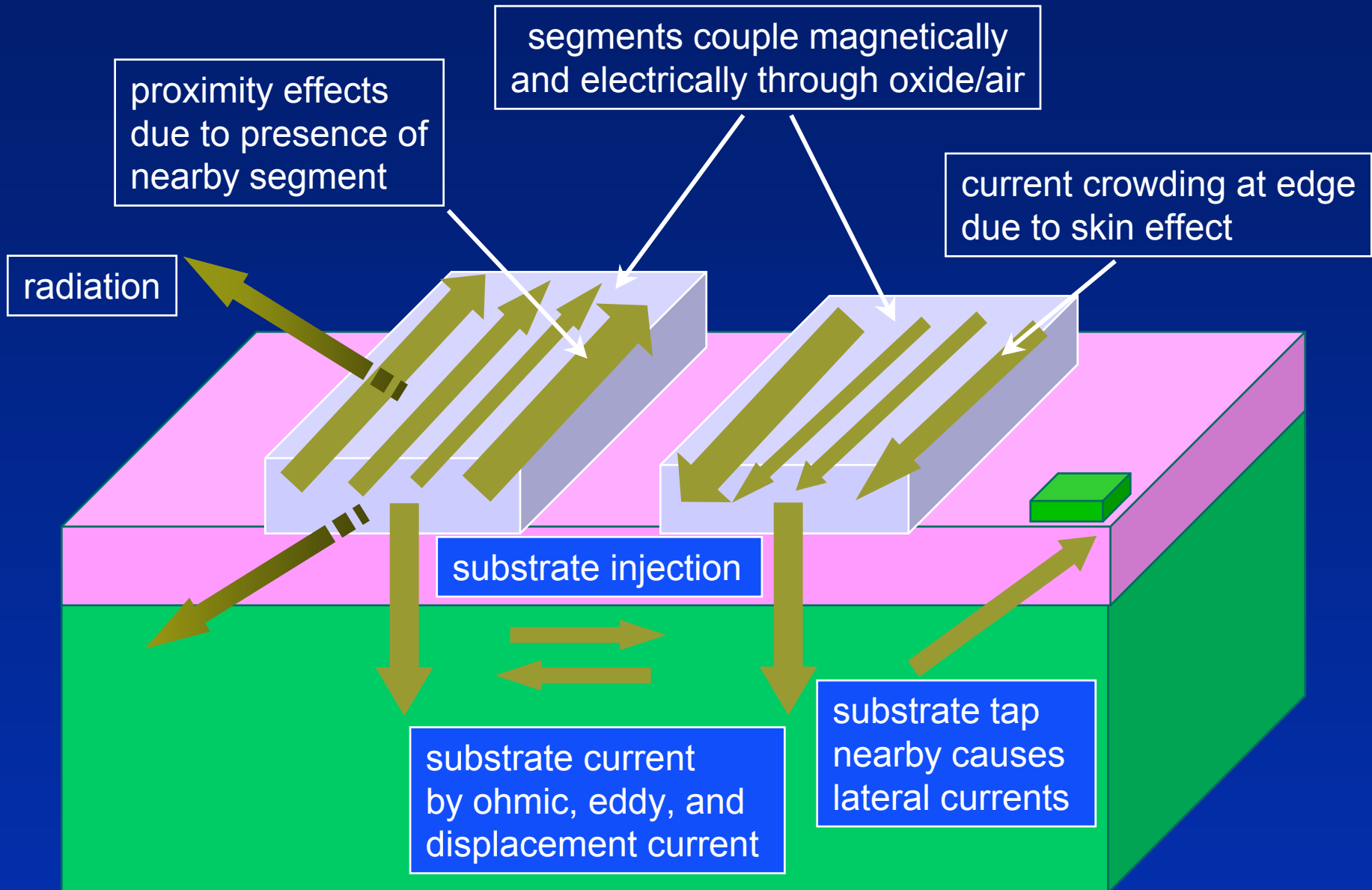
balun

3D Inductor/Transformer/Capacitors

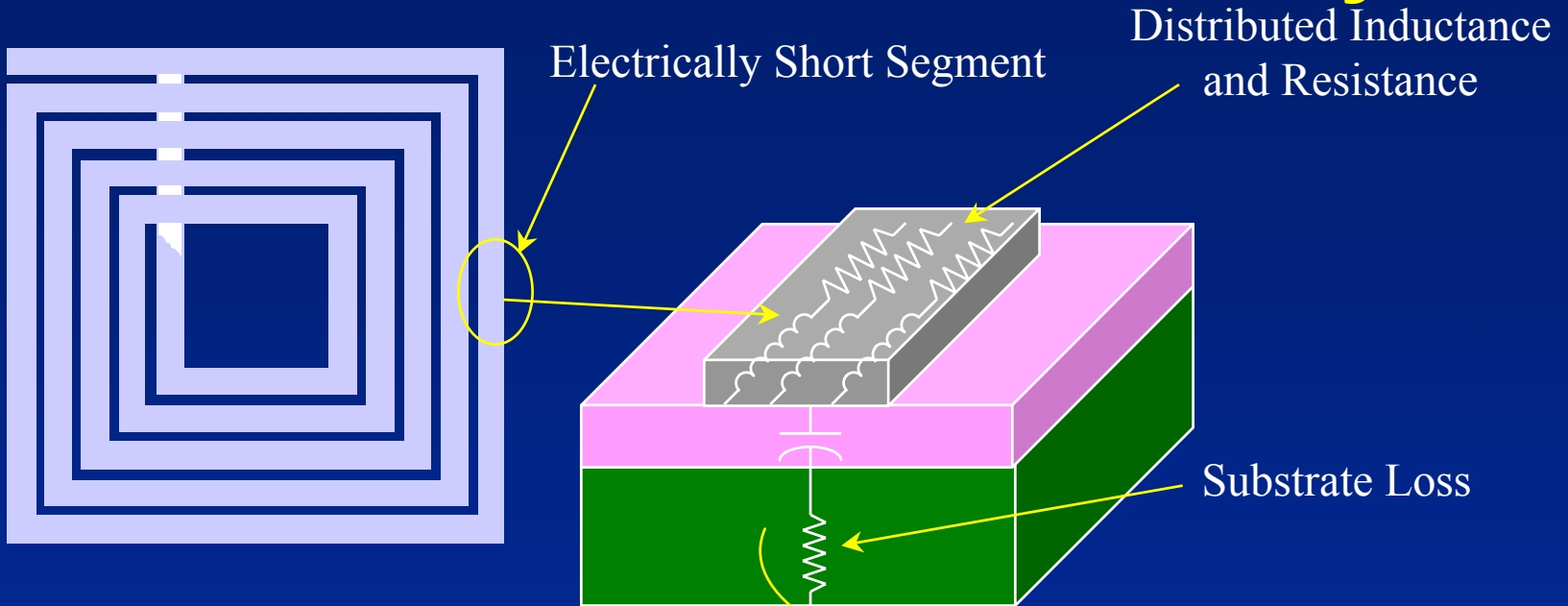


- 3D structures allow more flexibility
- Shunting several spirals lowers series loss
- Series interconnection of spirals can enhance magnetic field and provide nearly n^2 increase in inductance due to tight magnetic coupling
- New transformer topologies are also possible
- Multi-layer finger capacitor structures offer high density

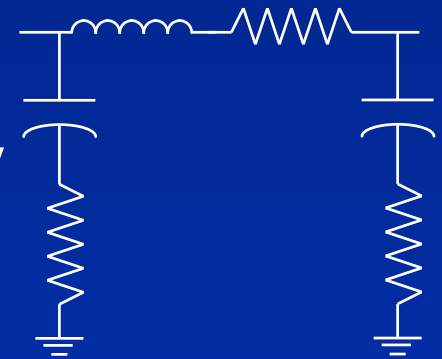
High Freq. Effects Over Si Substrate



Efficient/Accurate Method of Analysis



- Model short metal segment as lumped RLC Circuit
- Metal segments are linked capacitively and inductively
- Set up node equations for complete system and solve
- Method equivalent to solving Maxwell's equations



Reference: A. Ruehli, H. Heeb, *MTT*, July '92
Partial Element Equivalent Circuits (PEEC)

Substrate Currents

- From Maxwell's equations (Coulomb Gauge):

$$\begin{aligned} -\nabla^2 A &= j\omega\mu\epsilon E + \mu J = j\omega\mu\epsilon'(-j\omega A - \nabla\phi) \\ &= \underbrace{\omega^2\mu\epsilon A}_{\text{radiation}} - \underbrace{j\omega\mu\sigma A}_{\text{eddy currents}} - \underbrace{j\omega\epsilon\mu\nabla\phi}_{\text{disp.}} - \underbrace{\mu\sigma\nabla\phi}_{\text{conduction}} \end{aligned}$$

- Neglect radiation as long as $l_{\max} \ll \lambda$
- Displacement and conduction current are curl-free
- Losses due to conduction currents accounted for by solving:

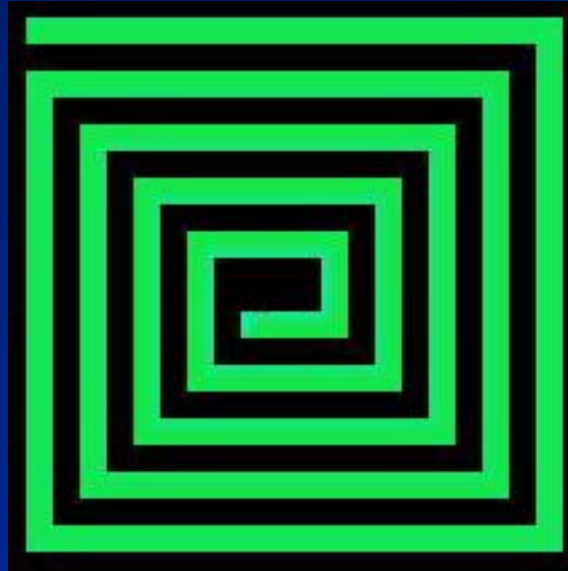
$$\nabla^2\phi = -\frac{\rho}{\epsilon'} \quad \epsilon' = \epsilon + \frac{j\sigma}{\omega}$$

- Losses due to eddy currents accounted for by solving:

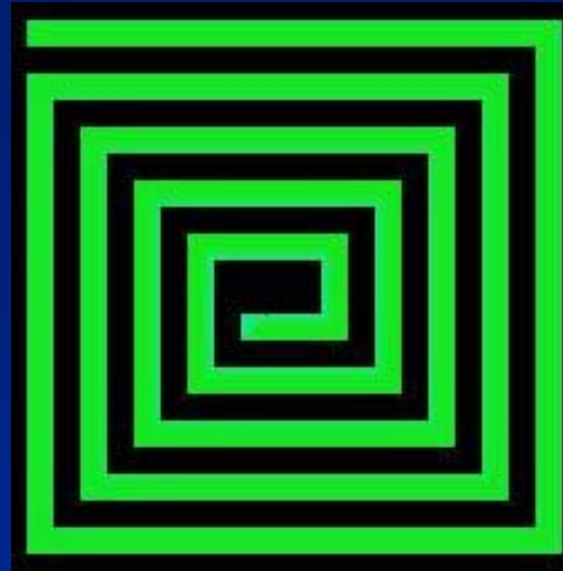
$$\nabla^2 A = j\omega\mu\sigma A$$

Current Constriction in Spiral Center

Current Density ↑

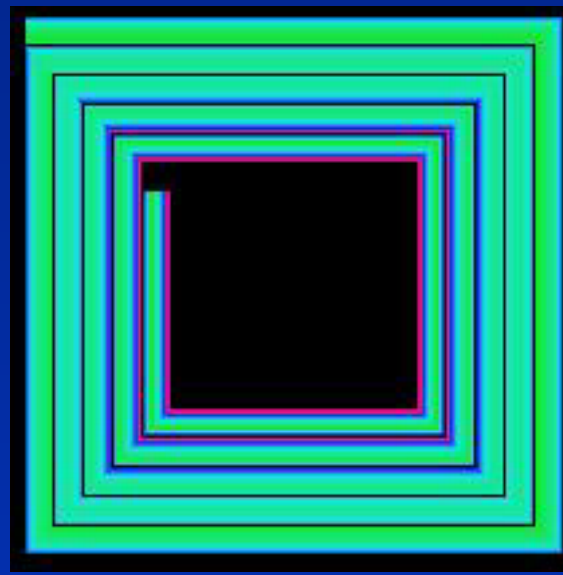
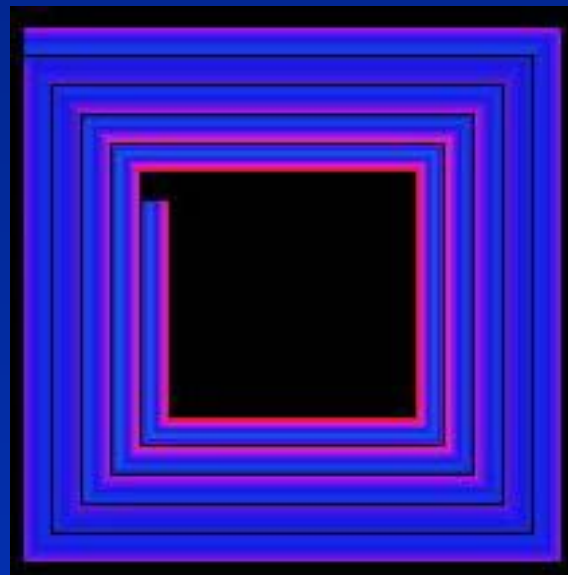
A vertical color scale bar on the left side of the image, with an upward-pointing arrow. The scale transitions from green at the bottom to red at the top, with intermediate colors of cyan, blue, and magenta.

1 GHz



5 GHz

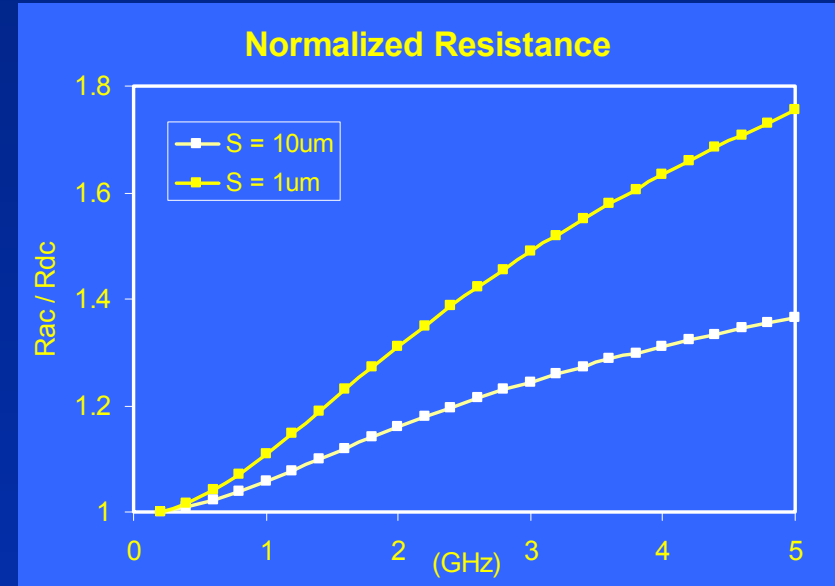
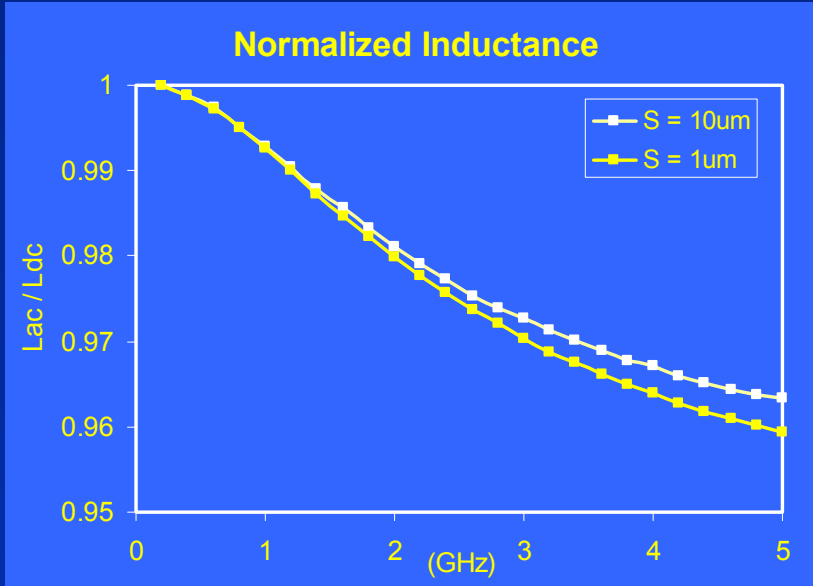
$L=200 \mu$
 $W=10 \mu$
 $S=10 \mu$
 $N=5$



$L=200 \mu$
 $W=10 \mu$
 $S=1 \mu$
 $N=5$

Partial Inductance Matrix Calculation

- Current constriction occurs at HF
 - Current concentrates along the outer *skin* of a conductor
 - *Proximity* of other conductors also influence the distribution
 - Inner turns in a spiral have most current constriction
- Example: Use $S=1 \mu$ spacing on and $S=10 \mu$.



$$L_{dc} = 5.2 \text{ nH and } 2.6 \text{ nH}$$

Bulk Eddy Current Losses

- Due to linearity in Maxwell's equations: $A(x, y, z) = A_{free-space} + A_{substrate}$
- Note that free-space contribution dominates inductance
- Substrate term dominates losses
- Use existing "3D" techniques to approximate inductance
- Use 2D formulation to approximate loss:

$$\tilde{Z}_{i,j}^{M,S} = \frac{-\mu j \omega}{2\pi} \int_0^{\infty} \frac{e^{-m|y-y_0|}}{m} \Gamma(m) K(m, w) \cos(m(x-x_0)) dm$$

- For single layer substrate (integral has analytic form):

$$\Gamma(m) = \frac{\gamma - m}{m + \gamma} e^{-2my_0}$$

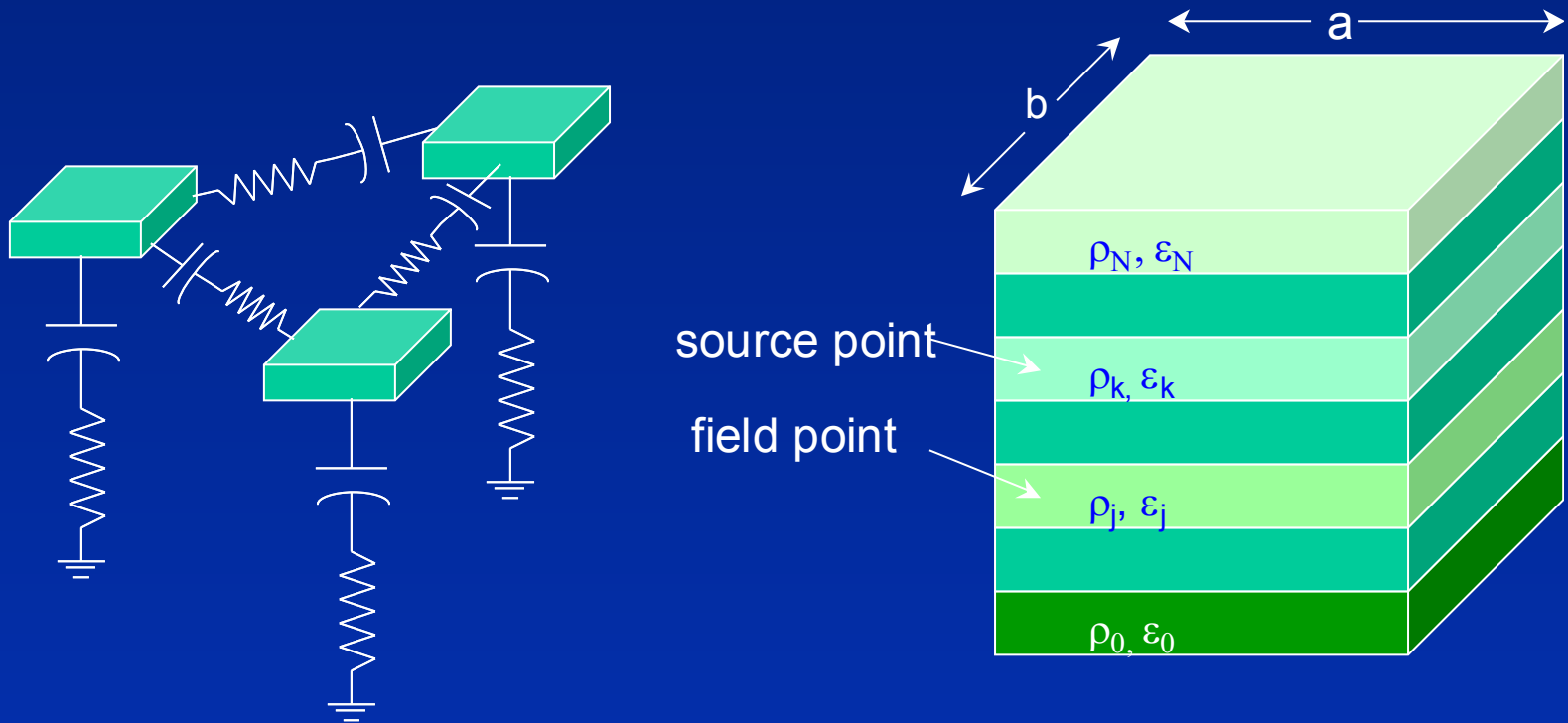
- For two layer substrate (use numerical integration):

$$\Gamma(m) = e^{-2my_0} \frac{\gamma_2(m - \gamma_3) - (\gamma_2^2 - m\gamma_3) \tanh(t\gamma_2)}{\gamma_2(m + \gamma_3) + (\gamma_2^2 + m\gamma_3) \tanh(t\gamma_2)} \quad \lim_{m \rightarrow 0} \frac{\text{Im}[\Gamma(m)]}{m} < \infty$$

Reference: A. M. Niknejad and R. G. Meyer, *MTT*, January '01

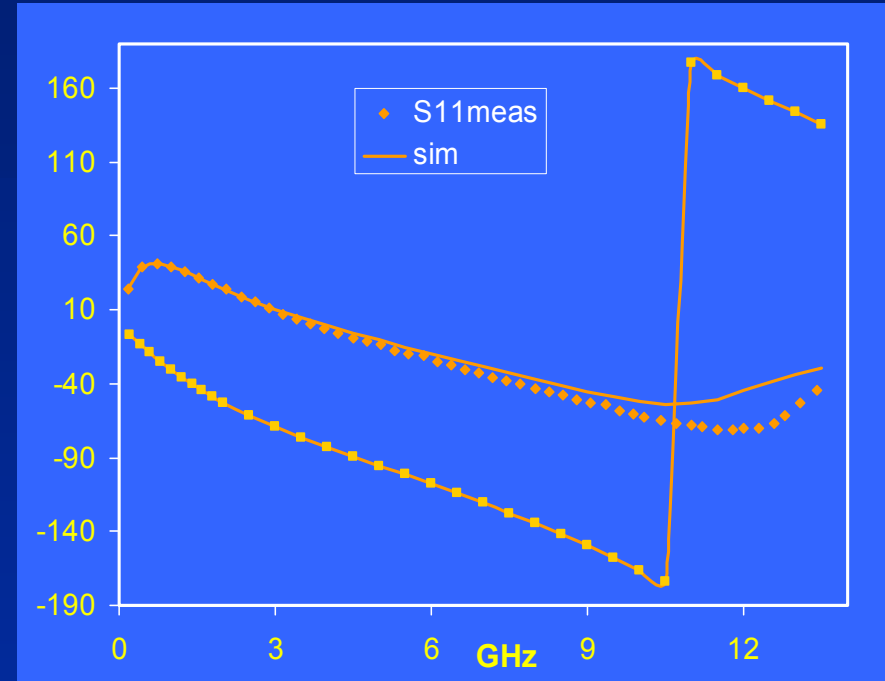
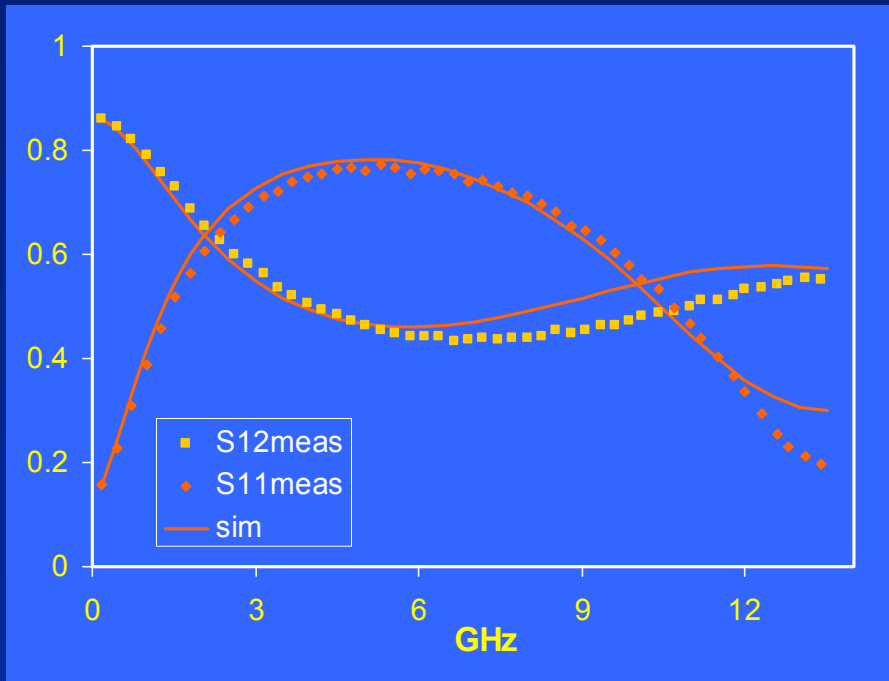
Capacitance Matrix Calculation

- Solve 3D Poisson's equation over multi-layer substrate
- Green function used to find impedance matrix
- Green func is calculated in efficient manner using DCT



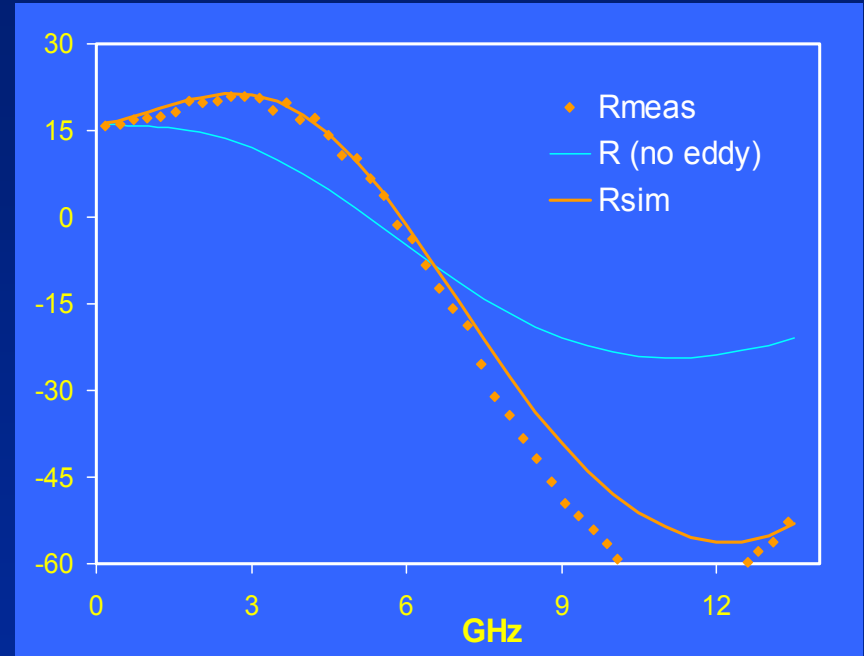
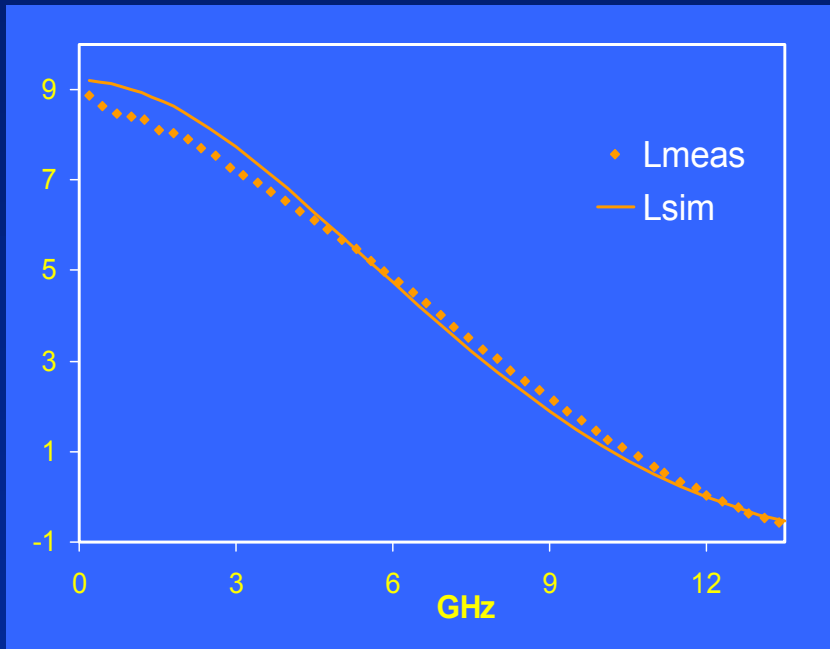
Reference: A. M. Niknejad, R. Gharpurey, R. G. Meyer, *TCAD*, April '98

Measurement and Simulation over a Conductive Substrate



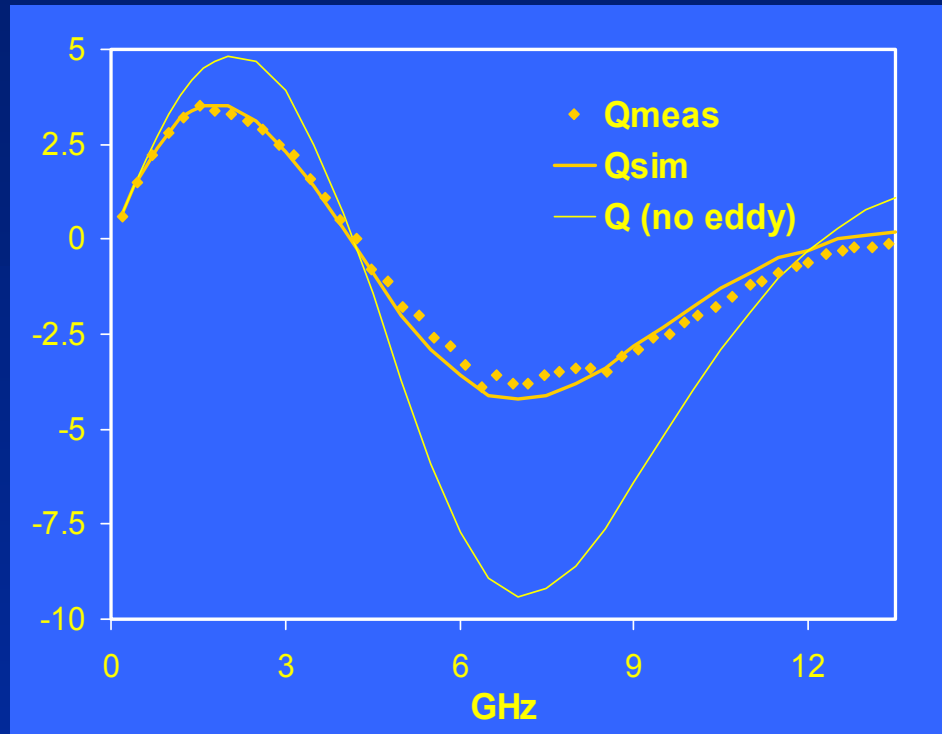
- Device self-resonance frequency: 4.25 GHz (sim at 4.15 GHz)
- Measurements performed using GSG air co-planar probes
- Processed with HP 8719C Network Analyzer (100 MHz - 14 GHz)

Extracted Device Inductance and Series Loss



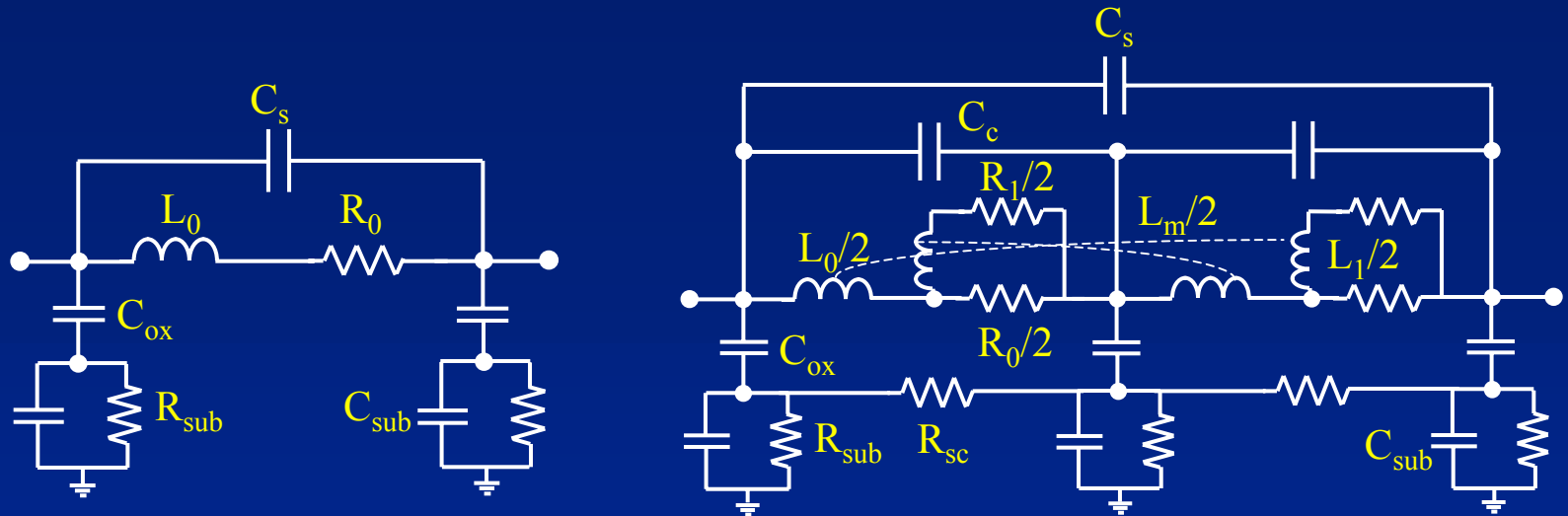
- Device “pi-parameters” equivalent to s-parameters
- Inductance and resistance calculated using real/imag part of s_{12}
- Inductance decrease due to capacitive currents at hf
- Resistance increase dominated by eddy current losses

Extracted Device Quality Factor Q



- Negative “Q” means device is acting capacitively
- Device Q predicted 40% higher without eddy currents

Broadband Compact Modeling



Reference: Yu Cao et. al., CICC 2002

- Conventional π model has physical roots
- Model works well over a narrow band
- Model cannot capture freq. dep. skin-effect and proximity effects: $L(f)$ $R(f)$
- Physically derived 2- π model can fit data over a wider frequency range

ASITIC Homepage

<http://www.eecs.berkeley.edu/~niknejad/asitic.html>

- **Current Release: *Grackle***
- **Supported Platforms:**
 - **Linux, Windows 2000/NT**
 - **HP-UX, SunOS**
- **Online Help, FAQ, Install Guide**
- **Quickstart, Sample Sessions**
- **Your feedback is very important!**



Limitations and Future of ASITIC

- Compute Conductor Thickness in Capacitance
- Include Reflected Substrate Inductance
- Automatically generate wideband models
- Divorce Geometric Layout and Electrical Model
 - Allow direct importing GDSII and CIF files
- Work on Full-Chip RF Extraction
- Work with Board and Package Environment