

# A 2.4 GHz Monolithic Mixer for Wireless LAN Applications

Keng Leong Fong, Robert G. Meyer

Department of Electrical Engineering and Computer Science  
University of California at Berkeley  
Berkeley, CA 94720-1772

## Abstract

A Class AB downconversion mixer for 2.4 GHz wireless LAN applications is presented. The circuit is implemented in a 13 GHz  $f_T$  BiCMOS process, and consumes 7.9 mA total current from a 3V supply. A single-balanced design using bond-wire degeneration in the common-emitter driver stage is optimal for power consumption and noise figure. The design has a power gain of 4.5 dB, a single-sideband noise figure of 10 dB, an input third-order intercept point of 1 dBm, and an input 1 dB compression point of -7.5 dBm.

## Introduction

The rapid growth of wireless communication services has now been extended to higher frequencies such as the 2.4 GHz band. Together with the demand for low cost and low power, this increase in frequency presents a challenge to RF circuit designers to find low-cost solutions for the realization of high-frequency receivers using plastic packages and high-volume silicon technologies.

Downconversion mixers, which convert radio frequency (RF) signals to an intermediate frequency (IF), are very important building blocks within a radio system. Their performance affects the performance of the entire system and the performance requirements of other building blocks. For instance, a mixer with low noise figure (NF) reduces the gain requirement of the low-noise amplifier (LNA). A mixer with appropriate power gain reduces the noise contribution from the intermediate-frequency (IF) stage. A mixer which requires a low local oscillator (LO) drive reduces the power consumption of the LO.

In this paper, a new class AB downconversion mixer for 2.4 GHz wireless LAN applications is presented. The design philosophy used to achieve simultaneous low noise figure and high linearity is described, and measurement results on an experimental circuit are presented.

## Circuit Design

The basic topology of the mixer is shown in Fig. 1. It comprises a common-emitter driver stage ( $Q_1$ ) and a differential switching pair ( $Q_2$  and  $Q_3$ ). The driver stage amplifies

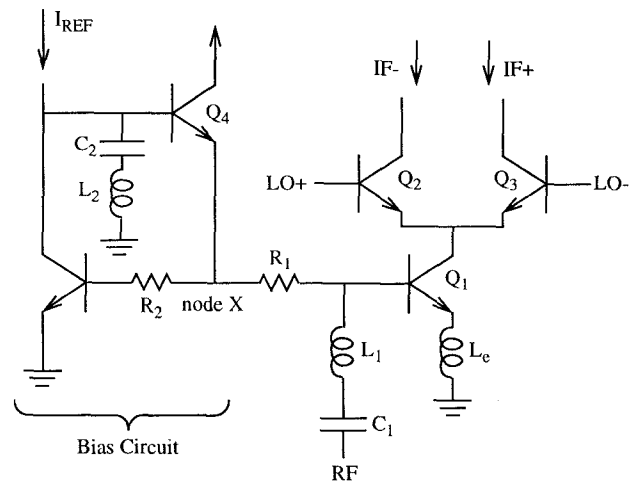


Fig. 1. Class AB Mixer

the radio frequency (RF) signal to compensate for the attenuation due to the switching process, and to reduce the noise contribution from the switching pair. The switching pair performs the mixing process, which converts the RF signal down to the IF.

The linearity of the common-emitter driver stage is increased by the use of degeneration provided by the bond-wire inductor  $L_e$ . In contrast to resistive degeneration, inductive degeneration does not contribute an additional source of noise. To reduce the noise contribution from  $Q_1$ , a large device with small base resistance ( $r_b$ ) is used. However, the increase in collector-base junction capacitance ( $C_{\mu}$ ) decreases linearity, and increases feedback from collector to base (this reduces gain and makes impedance matching difficult). The gain of the driver stage should be maximized (by minimizing the bond-wire inductance of  $L_e$ ) to reduce the noise contribution from the switching pair. However, the impedance matching requirement sets a lower limit on the value of the degeneration inductance. The impedance looking into the base of  $Q_1$  is

$$2\pi f_T L_e + r_b + sL_e + \frac{1}{sC_{\pi}} \quad (1)$$

## 9.4.1

where  $C_\pi$  is the total base-emitter capacitance. This equation neglects the effect of  $C_\mu$ . The  $(2\pi f_T L_e + r_b)$  term should be made large enough for impedance matching. The imaginary part of this equation is cancelled by the bond wire  $L_1$  in series with the external blocking capacitor  $C_1$ .

Capacitor  $C_2$  is a bypass capacitor used to prevent noise of the bias circuit from entering the base of  $Q_1$ . It also helps to stabilize the bias circuit. Although  $C_2$  does not filter the noise from  $Q_4$ , the noise contribution from  $Q_4$  is small since it is attenuated by the impedance divider network formed by the resistor  $R_1$  and the impedance looking into the base of  $Q_1$  in parallel with the source resistance of the RF input. Resistor  $R_1$  contributes little noise since the impedance at node X is high. It is undesirable to place a bypass capacitor at the emitter of  $Q_4$  (node X) because although this capacitor can filter noise from the bias circuit, the noise contribution from  $R_1$  becomes significant (increase noise figure of the mixer by 1.2 dB) due to low impedance at node X.

Without resistive feedback, the common-emitter driver stage also exhibits a class AB behavior [1]. This phenomenon is due to the nonlinear collector current ( $I_C$ ) versus base-emitter voltage ( $V_{BE}$ ) characteristics of the bipolar transistor. If the output current of the driver stage is represented as

$$I_{out} = I_0 + I_1 \cos \omega t + I_2 \cos 2\omega t + I_3 \cos 3\omega t + \dots \quad (2)$$

where  $I_n$  is the amplitude of the  $n$ 'th harmonic,  $I_0$  is the average current and  $I_1 \cos \omega t$  is the desired signal current. In a class A design, the average current ( $I_0$ ) is the same as the bias current used in the design, and the signal current amplitude ( $I_1$ ) has to be smaller than the bias current. As a result, input 1 dB compression point ( $P_{1dB}$ ) and gain requirements set a lower limit on the bias current. On the other hand, the signal current amplitude ( $I_1$ ) in a class AB design can increase beyond the bias current. Fig. 2 shows the simulated signal current amplitude ( $I_1$ ) and the average current ( $I_0$ ) of the class AB driver stage (biased at a collector current of 4 mA) as a function of RF input power. The increase in signal current and average current beyond the bias current is due to the nonlinearity of the device. Using the class AB behavior, a lower bias current can be used to meet the input  $P_{1dB}$  requirement. Simulation shows that the driver stage has an input  $P_{1dB}$  of 0 dBm. Since the signal current amplitude ( $I_1$ ) is larger than the average current ( $I_0$ ) at large input power, class AB design is also more efficient than class A design in the presence of large input signals.

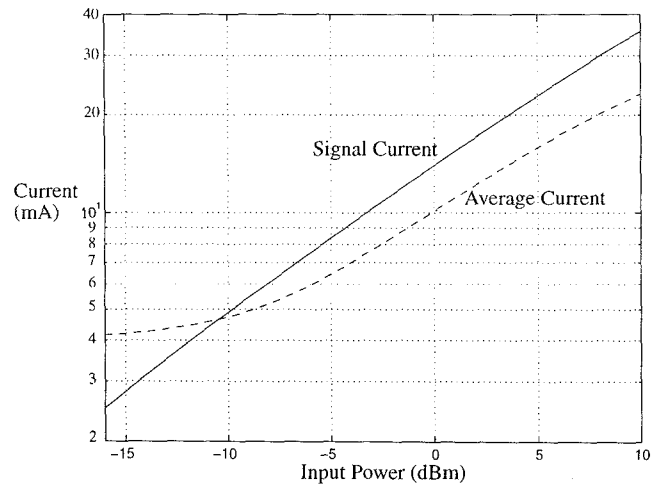


Fig. 2. Simulated Driver Output Currents versus Input Power

The presence of DC (resistive) feedback in the common-emitter driver stage can suppress the class AB behavior. To avoid gain compression due to the DC feedback, resistors  $R_1$  and the resistance at the emitter of  $Q_1$  should be minimized. However,  $R_1$  should be large enough to attenuate the noise contribution from the bias circuit. A resistance value of  $200\Omega$  is used for  $R_1$  as a compromise between noise figure and  $P_{1dB}$ .

The nonlinear behavior of this mixer is dominated by that of the switching pair ( $Q_2$  and  $Q_3$ ) because the pair cannot be switched very rapidly due to large values of  $C_\pi$ . On the other hand, the linearity of the common-emitter driver stage increases as device forward transit time ( $\tau_F$ ) and RF signal frequency increase since the device becomes more current driven.

The switching pair ( $Q_2$  and  $Q_3$ ) should be driven by a large LO signal to minimize its noise contribution. The switching pair contributes noise to the mixer output when both transistors ( $Q_2$  and  $Q_3$ ) are on [2], and a large LO signal is needed to reduce the duration of this condition. Fig. 3 shows the simulated noise figure (NF) of the mixer (LO buffer is not included) as a function of differential LO amplitude. However, a very large LO signal results in excessive current being pumped into the common emitter point of the switching pair through the base-emitter junction capacitance ( $C_{je}$ ), and thus generates additional nonlinearity [2]. Fig. 4 shows the simulated input third-order intercept point ( $IP_3$ ) of the mixer as a function of differential LO amplitude. For the same reason, the device sizes should be kept small to reduce the  $C_{je}$ . On the other hand, reasonably large devices should be used to reduce the  $r_b$  noise contribution and the voltage drop across  $r_b$ . Excessive voltage drop across  $r_b$  reduces the

## 9.4.2

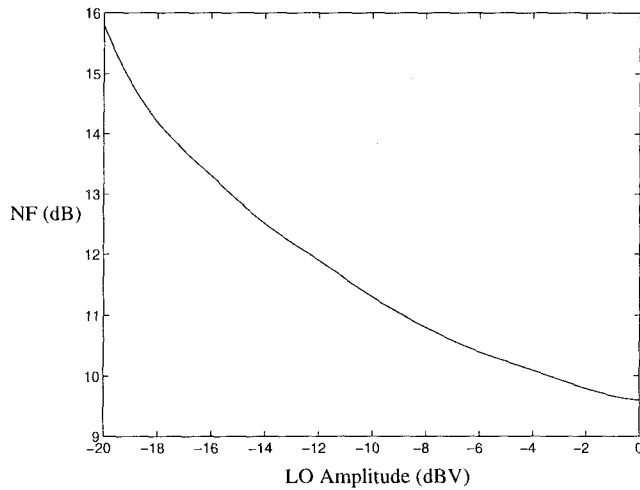


Fig. 3. Simulated Mixer Noise Figure versus LO Amplitude

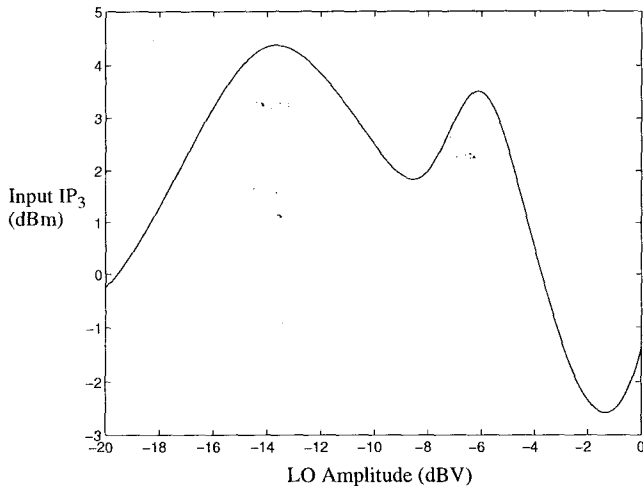


Fig. 4. Simulated Mixer Input  $IP_3$  versus LO Amplitude

effective amplitude of the LO signal switching the devices. Large LO amplitudes also increase power consumption and LO feedthrough, as well as decreasing head room at the collectors of  $Q_2$  and  $Q_3$ . Considering the trade-off among noise figure, linearity and power consumption, a differential LO amplitude of -8 dBV is used in this design.

Single-balanced mixers do not reject noise from the driver stage at the IF. When one transistor of the switching pair ( $Q_2$  and  $Q_3$ ) is on, the mixer functions as a cascode amplifier. Noise from the driver stage at the IF can feedthrough to the IF outputs. Since the driver stage has high gain at the IF (due to the inductive degeneration), the output noise of the mixer would increase significantly if a single-ended output were taken. This common-mode noise can be suppressed by either taking the IF outputs differentially or performing single-ended to differential conversion. Since

most IF filters are single-ended, the current combiner network [3] shown in Fig. 5 is used to perform the differential to

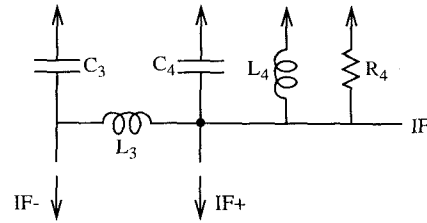


Fig. 5. Current Combiner Network

single-ended conversion.  $C_3$  and  $L_3$  resonate partially ( $(2\pi\sqrt{2L_3C_3})^{-1} = IF$ ) and reverse the phase of  $IF^-$  so that it can added in phase to  $IF^+$ .  $C_4 (=C_3)$  is used to cancel the residual reactance due to partial resonance between  $C_3$  and  $L_3$ .  $C_3$  and  $C_4$  are monolithic MOS capacitors. They also help to suppress RF and LO feedthrough to the IF port. Due to the large inductor value,  $L_3$  is implemented externally.  $L_4$  is an external AC choke used to bias the collectors of  $Q_2$  and  $Q_3$ , while  $R_4$  defines the output resistance at the IF port. This implementation is lower in cost than a transformer.

If the switching pair were driven directly by an external LO, 2 dBm of LO power would be required. To reduce the power consumption of the external LO, a LO buffer with a voltage gain of 12 dB is included in the design. Fig. 6 shows

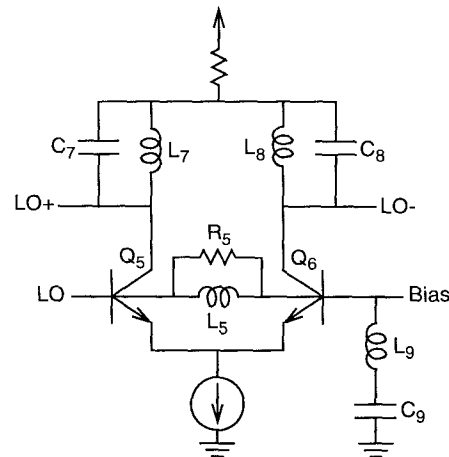


Fig. 6. LO Buffer

the basic topology of the LO buffer. One side of the differential pair ( $Q_5$  and  $Q_6$ ) accepts the LO input, while the other side is AC grounded by series tuning between capacitor  $C_9$  (external capacitor for good AC ground) and a bond wire  $L_9$ . Since the differential pair ( $Q_5$  and  $Q_6$ ) is not degenerated, the impedance looking into the base of  $Q_5$  is too low for imped-

### 9.4.3

ance matching. An integrated spiral inductor  $L_5$  is needed to tune out the  $C_\pi$  of  $Q_5$  and  $Q_6$ .

For a single-balanced design, the noise from the LO buffer at the IF can feedthrough to the IF output port. Hence, integrated spiral inductors  $L_7$  and  $L_8$  (low impedance at IF) are used at the output of the LO buffer to remove this noise. Since the capacitance at the bases of  $Q_2$  and  $Q_3$  is nonlinear, the LO signal at the output of the LO buffer becomes highly distorted without the linear capacitors  $C_7$  and  $C_8$ . This LO signal distortion tends to decrease the linearity of the mixer. Hence, the value of  $C_7$  and  $C_8$  should be much larger than  $C_\pi$  of  $Q_2$  and  $Q_3$  to reduce this LO signal distortion. The upper limit is set by current consumption and the quality factor ( $Q$ ) of  $L_7$  and  $L_8$ .

### Implementation

The mixer is implemented in a BiCMOS process with peak npn  $f_T$  of 13 GHz and CMOS  $L_{eff}$  of 0.8  $\mu\text{m}$ . The CMOS devices are mainly used in the biasing circuit. Fig. 7

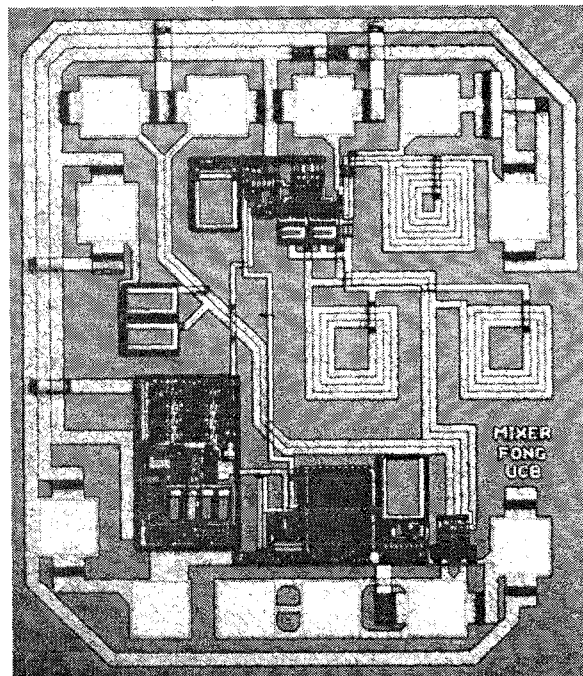


Fig. 7. Chip Micrograph

shows the die micrograph. The bonding pads are ESD protected and the die is housed in a SSOP20 plastic package. Transistor  $Q_1$  is placed close to the bonding pads to which the bond wires used for degeneration are connected. This is to minimize parasitic capacitance and resistance at the emitter of  $Q_1$ . The degeneration inductor  $L_e$  is implemented by three adjacent bond wires and pins in parallel. The LO pin and the AC ground pin ( $L_9$ ) are placed next to each other to

minimize the cross-sectional area of the resulting current loop. The two LO pins and the two IF pins are placed on the opposite side of the package from the RF pin to minimize coupling. The ESD buses are routed outside the bonding pads to minimize the routing distance between devices and bonding pads, and to avoid crossing with the signal buses. To further minimize the routing distance of high-frequency signals, the mixer and LO buffer are placed next to their corresponding bonding pads.

### Measurement Results

The measured performance of the mixer is summarized in Table 1. The measurements were performed at 25°C with

TABLE 1. Performance Summary

Parameters	Simulations	Measurements
Power Supply	2.7V to 5.5V	2.7V to 5.5V
Current Consumption	8 mA	7.9 mA
Conversion Gain (Power)	4 dB	4.5 dB
Input Third-Order Intercept Point	2.5 dBm	1 dBm
Input 1dB Compression Point	-5 dBm	-7.5 dBm
Single-Sideband Noise Figure	10.8 dB	10 dB
LO to RF Feedthrough	-30 dBc	-28 dBc

a 3V supply, using LO power of -8 dBm. Since the LC network at the output of the LO buffer is tuned to a lower frequency (due to parasitic capacitance), a slightly higher LO power is used. The RF, LO and IF frequencies used are 2.6 GHz, 2.4GHz and 200 MHz respectively. The input  $IP_3$  was measured with two RF tones of 1 MHz spacing.

### Acknowledgment

The authors would like to thank W. D. Mack, S. H. Lee, K. McAdams, A. Niknejad, F. Fang and Y. Peng for their help on this project. Fabrication of the prototype by Phillips Semiconductors is appreciated. This material is based on work supported in part by the U.S. Army Research Office under Grant Number DAAH04-93-F-0200.

### References

- [1] K. L. Fong, C. D. Hull, R. G. Meyer, "A Class AB Monolithic Mixer for 900 MHz Applications", unpublished.
- [2] C. D. Hull, "Analysis and Optimization of Monolithic RF Downconversion Receivers", Ph.D. dissertation, University of California at Berkeley, Berkeley, California, 1992.
- [3] S. H. Lee, "Resonance Balun with Arbitrary Impedance", US Patent No. 5412355.