

# A Wideband Low-Phase-Noise CMOS VCO

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## Abstract

A CMOS VCO has been designed and fabricated in a commercial 0.25 $\mu\text{m}$  CMOS process. Using a combination of switched binary-weighted capacitors and standard varactors, this VCO achieves a 28% tuning range with a control voltage ranging from 0-2 V, while maintaining a tuning sensitivity of less than 75 MHz/V over its entire frequency range. Compact choke inductors are used in place of resistors to provide a low noise bias point to the varactors. The choke inductors achieve more than 90 nH of effective inductance while consuming a die area of only 92 x 92  $\mu\text{m}^2$ . The measured single-sided phase noise is -127 dBc/Hz at a 600 kHz offset from a 1.24 GHz carrier when the VCO core is drawing 3.6 mA from a 2 V supply.

## Introduction

Voltage controlled oscillators (VCOs) are essential building blocks of modern communication systems. The VCO performance in terms of phase noise, tuning range, and power dissipation determines many of the basic performance characteristics of a transceiver. The current trend to utilize multi-band multi-standard receivers and also very wideband systems is driving the effort to create new VCO topologies with wide tuning range, low phase noise, and low power consumption.

Whereas relaxation oscillators easily achieve very wide tuning range (i.e. 100% or more), their poor phase noise performance disqualifies them in most of today's wireless and wireline applications. Because LC VCOs have been successful in narrowband wireless transceivers, there is a growing interest to extend their tuning range. Recently, several wideband CMOS LC VCOs have been demonstrated using a variety of techniques [1-4]. The high intrinsic  $C_{\text{max}}/C_{\text{min}}$  of inversion- or accumulation-type MOS varactors supports a very wide tuning range and their Q is sufficiently high that good phase noise performance can be maintained. However in practice, the overall phase noise performance is also highly dependent on the tuning sensitivity of the VCO, since noise from preceding stages of the frequency synthesizer is inevitably injected onto the VCO control input. Hence, aside from achieving a high raw tuning range, practical wideband VCO solutions must properly limit the overall VCO tuning sensitivity.

## Circuit Design

An LC VCO topology is chosen mainly for its potential to achieve good phase noise performance, relative to ring oscillators or other types of relaxation VCOs. The LC tank consists of integrated spiral inductors, P+/N-WELL varactors allowing continuous frequency tuning, and an array of binary-weighted switched capacitors providing coarse tuning steps. Compact bias chokes are used to bias the anode-side of the varactors. This design is implemented in a 0.25 $\mu\text{m}$  bulk CMOS technology with a thick top metal layer.

### A. Frequency tuning scheme

One of the main goals of this design is to concurrently achieve low phase noise and a wide frequency tuning range. A single varactor device with a steep C-V characteristic (i.e. a large  $C_{\text{max}}/C_{\text{min}}$ ) can be used to achieve a wide frequency range and typically has sufficiently high Q so that it does not degrade the phase noise performance of the VCO [1,4-6]. However, this can result in an excessively high tuning sensitivity,  $K_{\text{VCO}}$ . In practice, this is undesirable since the tuning line feeds substantial noise originating from preceding blocks of the frequency synthesizer. Noise present on the tuning line appears across the varactors and effectively modulates the device junction capacitance, resulting in phase noise sidebands about the carrier. To avoid this problem, the targeted frequency range is split into several sub-bands by means of a switched capacitor array [8]. Because the desired tuning range has been divided, a small varactor device with a shallow C-V characteristic is sufficient to cover each frequency sub-band.

The capacitor array configuration is illustrated in Fig. 1. Capacitors  $C_a$ - $C_b$  are implemented as high-quality metal-insulator-metal (MIM) capacitors. Minimal-length NMOS devices are used to switch each capacitor in and out of the tank. Because each MOS switch contributes additional loss to the tank due to its finite on-resistance,  $R_{\text{on}}$ , much effort has been expended in minimizing this penalty. On the other hand, the transistors cannot be made arbitrarily wide since in the off-state their parasitic overlap and drain-to-bulk capacitances limit the achievable tuning range. Simulations were used to establish a good compromise. This critical trade-off is one of many examples that reveal the conflicting nature of concurrently achieving low phase noise and a wide frequency tuning range.

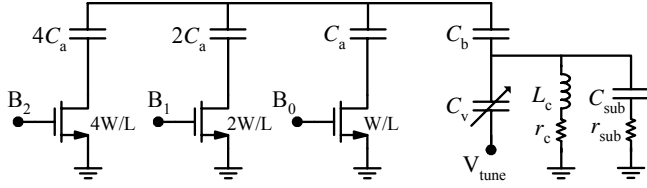


Fig. 1: Switched capacitor array and varactor configuration.

The varactors used in this design are implemented using reverse-biased P+/N-WELL junctions. MIM capacitor  $C_b$  is used to decouple the varactor from the high voltage amplitude that develops across the tank. This helps to prevent these junctions from reaching forward-bias conditions during large voltage peaks, which would degrade the tank Q and result in an unacceptable increase in phase noise. Another benefit of adding  $C_b$  is that the finite varactor loss is now reflected across the tank by a factor of  $(C_b + C_v)^2 / C_b^2$ . The anode-side of the varactor is commonly biased to ground using a large-value resistor to sustain a high impedance. Because this method of preserving the tank Q comes at the expense of additional noise (this trade-off can be optimized), choke inductors are used instead, as illustrated in Fig. 1. These structures were designed to provide a very high inductance while consuming relatively little die area. This goal was achieved using ASITIC [9] to determine the optimal structure dimensions, given restrictions imposed on the quality factor and self-resonant frequency. The resulting structure consists of 11 turns of  $3.6 \mu\text{m}$  wide traces spaced apart by  $0.4 \mu\text{m}$  and occupying the first four metal layers. The area consumed by each choke is  $92 \times 92 \mu\text{m}^2$ . The benefits of using an inductive bias network as opposed to resistors can be analyzed considering the  $\Pi$ -equivalent network of the choke inductor as shown in Fig. 1. In the frequency range of interest, the equivalent resistance reflected across the tank terminals,  $R_{\text{eq}}$ , is given by:

$$R_{\text{eq}}(\omega_0) = \left| (r_c + j\omega_0 L_c) \parallel (r_{\text{sub}} + 1/j\omega_0 C_{\text{sub}}) \right| \cdot n^2 \quad (1)$$

where  $n = (C_b + C_v') / C_b$  and  $C_v' \cong C_v$  since for the intended use of the choke inductor  $\omega_0 \gg 1/\sqrt{L_c \cdot C_v}$ .

### B. VCO core design

The LC VCO core is based on a fully-differential PMOS cross-coupled topology and is shown in Fig. 2. Differential topologies are generally preferred since they offer better power supply and substrate noise rejection over single-ended designs. Although a complementary cross-coupled topology is attractive because of its higher tank voltage amplitude for a given bias current and LC tank configuration, this benefit should be carefully weighted against its reduced headroom, increased parasitics, and additional noise sources.

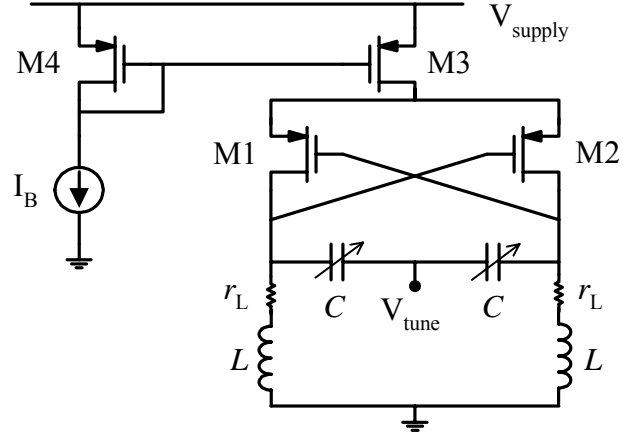


Fig. 2: Cross-coupled PMOS-only LC VCO

For this design, a non-complementary topology was determined to be preferable. PMOS devices were chosen to reduce flicker noise at the expense of reduced transconductance for a given aspect ratio. Despite the fact that the conductive channel is no longer buried as in older technologies, close scrutiny of the available flicker noise data revealed PMOS devices to have slightly lower flicker noise in the expected operating regimes. As an additional benefit, the device N-WELL provides some amount of isolation from the substrate.

The aspect ratio of cross-coupled devices M1 and M2 is chosen strictly based on oscillation startup requirements, for the minimum expected bias current. In other words,  $W/L_{1,2}$  is made just large enough such that the resulting initial loop gain (i.e. negative resistance) guarantees startup with a reasonable safety margin under worst-case conditions. For a wideband VCO, the pronounced frequency dependence of the equivalent tank impedance at resonance,  $R_T$ , must be considered. In the low-GHz regime where the tank loss is dominated by the series resistance of the spiral inductors, the small-signal transconductance,  $g_m$ , must satisfy the following inequality:

$$g_m \geq 1/R_T \cong r_L / (\omega_0 \cdot L)^2 \quad (2)$$

Thus, the worst-case scenario occurs at the low-end of the targeted frequency range (i.e. the frequency where the equivalent tank resistance is lowest), for the smallest expected bias current. Although not considered here, practical implementation should also address the negative temperature dependence of the device transconductance. Since the drain noise current of the cross-coupled devices is the dominant thermal noise contributor in this design, the lengths of M1 and M2 are made larger than minimum-size to reduce hot-electron effects, which cause the excess noise factor  $\gamma$  to increase significantly above the long-channel value of  $2/3$ . The gate length is chosen based on a careful inspection of the tradeoff between noise and capacitive parasitics.

### Experimental Results

This VCO has been fabricated in a commercially available  $0.25\mu\text{m}$  CMOS technology. The tank inductors were realized on a thick top metal layer and have a measured  $Q$  ranging from about 9 to 10.5 over the VCO frequency range. Simulations suggest a loaded tank  $Q$  of about 7. The VCO was measured on a test board built on standard FR4 material. The die was glued directly onto the PC board with conductive silver epoxy and wirebonds were used to connect all inputs and outputs. Fig. 4 shows the VCO chip photograph.

A wide tuning range from 1.06 to 1.40 GHz (28%) is achieved with a tuning voltage from 0 to 2 V. As shown in Fig. 5, there are 8 partially overlapping frequency sub-bands over which  $K_{\text{VCO}}$  remains below 75 MHz/V. A low and fairly constant  $K_{\text{VCO}}$  helps to maintain good phase noise performance and eases stability constraints once the VCO is used in an actual phase-locked loop.

The measured inductance and  $Q$  of the choke inductor are shown in Fig. 6. The choke inductor self-resonates around 1.95 GHz.

Phase noise measurements were performed using the HP5500 phase noise measurement system. Fig. 7 shows a typical result for the measured phase noise near the middle of the tuning range. As illustrated in Fig. 8, the phase noise varies by less than 1.6 dB across the entire frequency range for frequency offsets above 100kHz. When biased at a core current consumption of 3.6 mA with a 2 V supply, this VCO achieves a phase noise of  $-111$ ,  $-127$ ,  $-131$  dBc/Hz with respect to a 1.244 GHz carrier at 0.1, 0.6 and 1.0 MHz offsets, respectively.

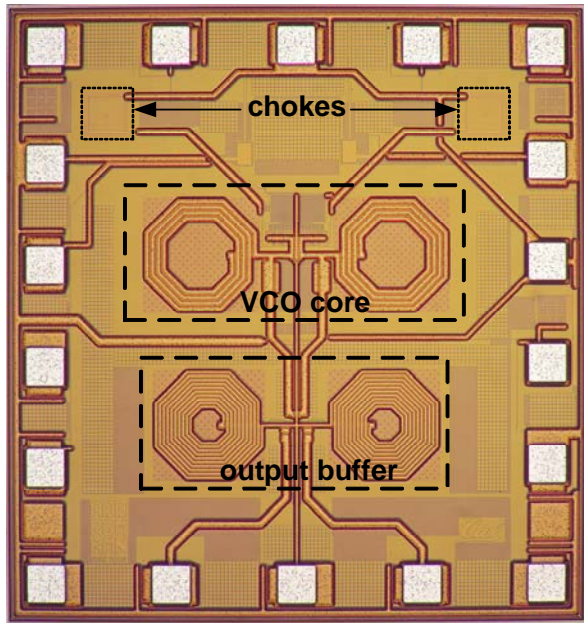


Fig. 4: Chip photograph.

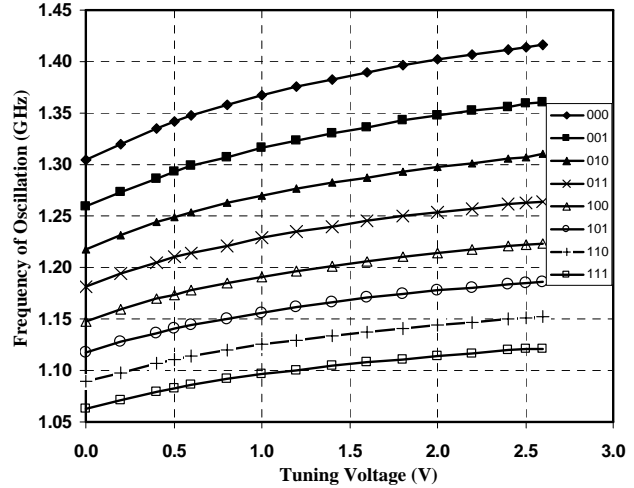


Fig. 5: Measured frequency tuning range.

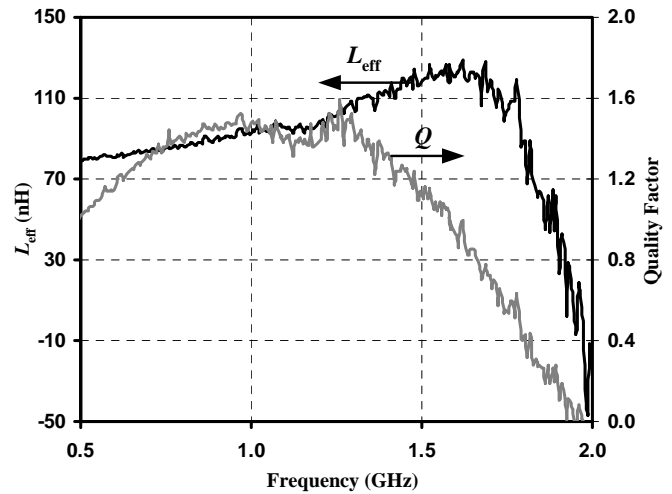


Fig. 6: Measured inductance and  $Q$  of choke inductor.

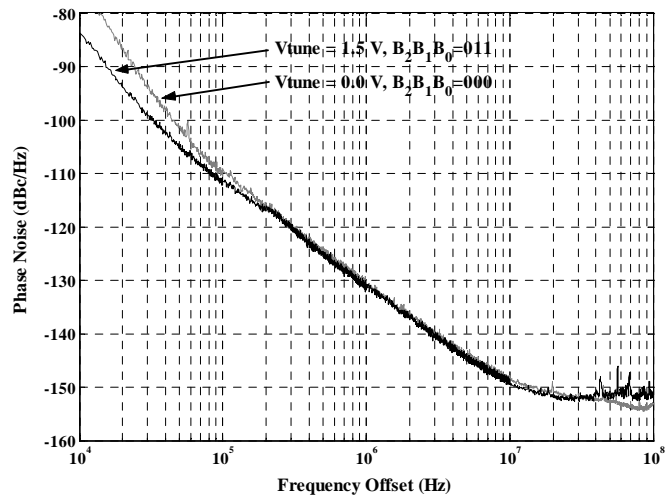


Fig. 7: Measured phase noise for a 1.244 GHz carrier frequency with  $I_B = 3.6$  mA and a 2 V supply. (a)  $V_{\text{tune}} = 1.5$  V and  $B_2B_1B_0 = 011$ . (b)  $V_{\text{tune}} = 0$  V and  $B_2B_1B_0 = 000$ .

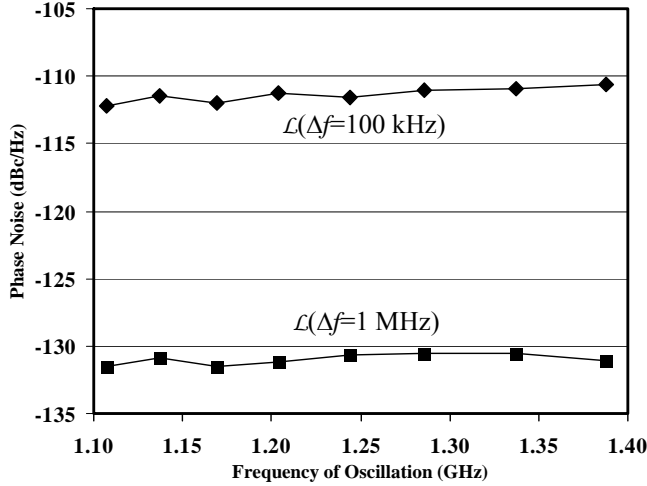


Fig. 8: Phase noise measured at 0.1 and 1.0 MHz offsets from the carrier with  $V_{\text{tune}}=1.5$  V,  $I_B=3.6$  mA and a 2 V supply.

As can be seen from Fig. 7, even for the case where the tuning voltage is set to 0 V and the VCO is operated at the upper end of the tuning range ( $B_2B_1B_0=000$ ) where the tank amplitude is largest (since the equivalent tank impedance is highest at that point), the phase noise degrades by less than 2 dB for offsets greater than 100 kHz. Applications that require lower phase noise can achieve this by providing the VCO core with a higher bias current, as long as the VCO stays in the current-limited regime [1]. However, care must be taken to avoid forward-biasing the varactors, as discussed earlier. Restricting  $V_{\text{tune}}$  from 0.5 to 2.0 V only incurs a marginal penalty on the tuning range, which decreases from 28% to 26%. Table 1 summarizes the VCO performance.

Technology	0.25 $\mu$ m CMOS
Supply Voltage	2 V
Current Consumption (VCO core)	3.6 mA
Center Frequency	1.25 GHz
Tuning Range	28 %
Tuning Sensitivity ( $K_{\text{VCO}}$ )	$< 75$ MHz/V
Phase Noise ( $f_o=1.244$ GHz, $\Delta f=100$ kHz)	-111 dBc/Hz
Phase Noise ( $f_o=1.244$ GHz, $\Delta f=600$ kHz)	-127 dBc/Hz
Phase Noise ( $f_o=1.244$ GHz, $\Delta f=1$ MHz)	-131 dBc/Hz

Table 1: VCO performance summary

The VCO performance summarized above can be compared to previously published VCO by means of a figure of merit (FOM), as defined in [1] and repeated here for convenience:

$$FOM = 10 \log \left( \frac{kT}{P} \cdot \left( \frac{f_{o,\text{max}} - f_{o,\text{min}}}{\Delta f} \right)^2 \right) - \mathcal{L}\{\Delta f\} \quad (3)$$

where  $f_o$  is the carrier frequency,  $\Delta f$  is the frequency offset,  $P$  is the power consumed by the VCO core, and  $\mathcal{L}\{\Delta f\}$  is the

phase noise measured at an offset  $\Delta f$  from the carrier. This results in a FOM of about -0.6 dB. Table 2 shows how this number compares to some other notable published VCOs implemented in bulk CMOS. With the exception of [3], the FOM for our VCO compares favorably to the others listed in Table 2. The design presented in [3] uses bondwires in place of integrated spiral inductors.

Reference	Center Freq. (GHz)	Power (mW)	Tuning range	FOM (dB)
[1]	2.6	10	26%	-3.1
[2]	1.8	32.4	28%	-3.8
[3]	2.1	12.2	35%	+5.8
[4]	1.30	12	28%	-10.3
[5]	5.8	5	14%	-10.6
[6]	5.15	7.2	21%	-1.1
[7]	2.33	6	14%	-13.2
<b>This work</b>	<b>1.25</b>	<b>7.2</b>	<b>28%</b>	<b>-0.2</b>

Table 2: VCO Performance Comparison

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