University of California, Berkeley EECS 242 Spring 2009 Prof. A. Niknejad



Design a broadband mixer based on the design topology above in the provided 90nm technology to meet the following specifications:

- Operating frequency from 3-10 GHz. Voltage conversion gain of 20 dB from 3-10 GHz. IF bandwidth of 500 MHz. Gain flatness of 1-dB in band.
- Noise figure <12 dB (DSB). Integrate the noise from 1MHz up to the bandwidth. IIP3 > -10 dBm.
- Power consumption < 5 mW for the G_m stage (1V supply). Rail to rail LO drive is available if needed. Be sure to design the current sources with real transistors. The design of the op-amp is optional and you may use an additional 5 mW of power.
- 1. Simulate and plot the conversion gain versus the LO amplitude.
- 2. Estimate the NF of the mixer designed above under large LO drive at the IF center frequency. Include (estimate) the contribution from flicker noise. Simulate the NF of the mixer as a function of the LO and verify the results.
- 3. Estimate the amount of LO port noise that can be tolerated while only increasing the overall NF by 0.2dB.
- 4. Specify the maximum tolerable op-amp noise (voltage and current) in order to meet these specifications.
- 5. Estimate the LO/RF/IF feedthrough signals and verify with simulation.
- 6. Simulate and calculate the IIP2/IIP3 of the mixer. Predict the performance by assuming the transconductor is the only source of non-linearity.