Problem Set 3
Due Wednesday March 18, 2009

1. Analyze the noise contribution of the degeneration inductor L if it has a finite quality factor Q_L.

2. Using the Pospiesalski noise model (aka our 142 MOSFET noise model), derive the input impedance and minimum achievable noise figure for an inductively degenerated LNA but include the effects of the transistor bulk terminal.

3. Using the transistor BSIM4 model provided, design an LNA using the following specifications. You may use any topology and any number of amplifier stages. Make a sketch of the amplifier layout. Be sure to include the gate resistance $rgateMod = 2$ and $tnoimod = 1$ (holistic).

   (a) Center frequency of 10 GHz, bandwidth of 400 MHz.

   (b) Transducer gain greater than 15dB. Assume the source impedance is 50ohms and that the LNA drives a load of 800ohms.

   (c) Minimum possible noise figure while consuming only 5mW from a 1V supply.

   (d) $S_{11} < -10$ dB across the band.

   (e) Inductors of $Q = 10$ are available. Minimum junction length of $0.1\,\mu$m. Transistors have a single gate contact.