# EECS 242:
# Active Technology for Communication Circuits

**Professor Ali M Niknejad**

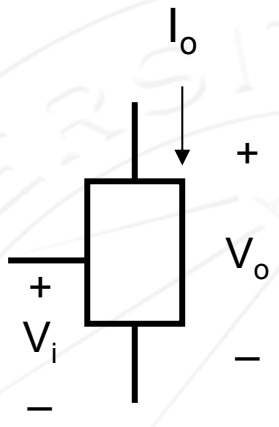
**Advanced Communication Integrated Circuits**

**University of California, Berkeley**

# Outline

- Comparison of technology choices for communication circuits
  - Si npn, Si NMOS, SiGe HBT, CMOS, JFETs, MESFETs…
- Key metrics
- Large signal relations
- Small signal models

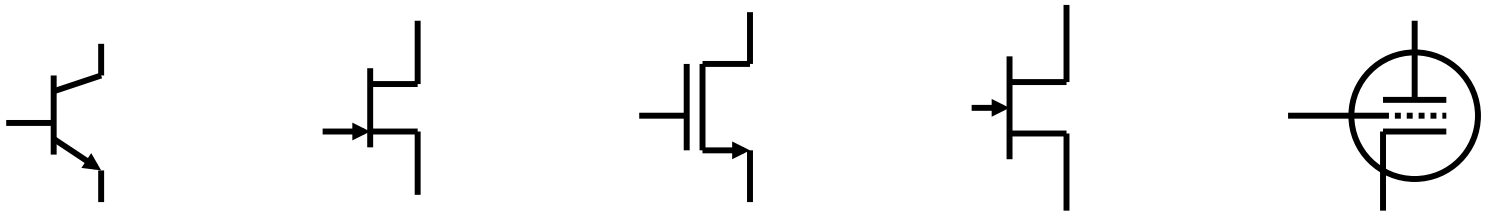
# Generic Three Terminal Device




Output current is dependent on input voltage:

$$I_o = f(V_i, V_o) \approx f(V_i)$$

Examples:



**npn BJT** **n-ch JFET** **NMOS** **GaAs MESFET** **vacuum tube**

Emerging Technologies: ~SOI, Multi-Gate, FETs (FinFETs)
CNT, Nanowire

# Large Signal Equations

Bipolar: ("forward active")

$$I_o \approx I_S e^{\frac{qV_{BE}}{kT}}$$

JFET/MESFET: ("pinch-off" regime)

$$I_D = I_{DSG}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

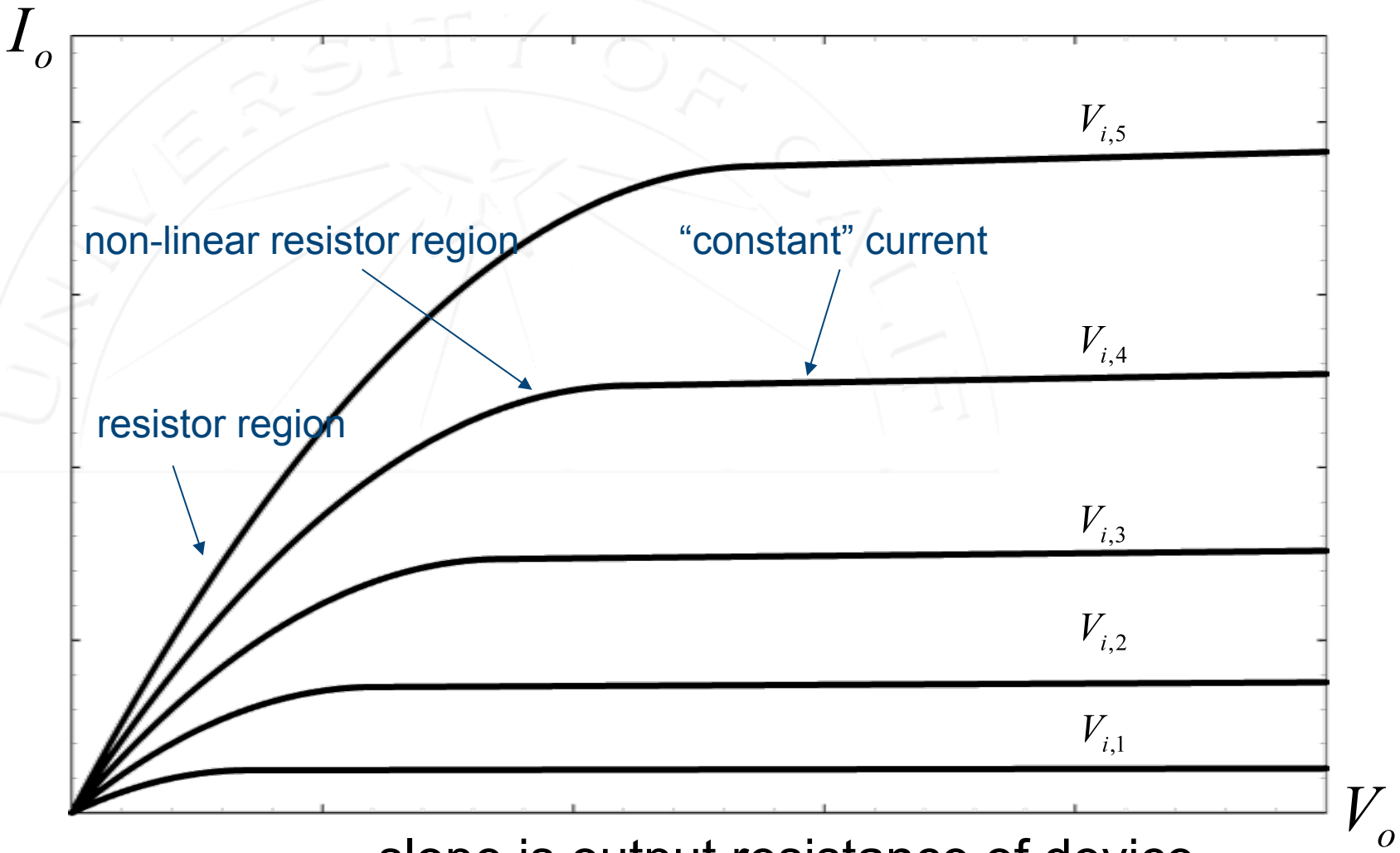
MOSFET: ("saturation")

$$I_D = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2$$

Vacuum Tube:

$$I_o = G\left(V_i + \frac{V_o}{\mu}\right)^{3/2}$$

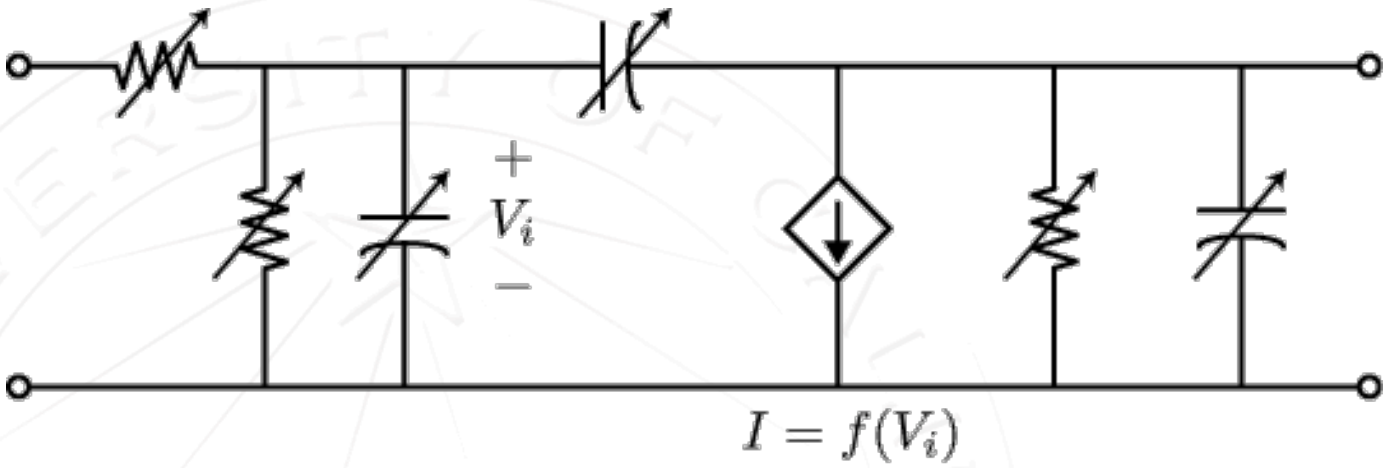
# Generic Device Behavior




slope is output resistance of device

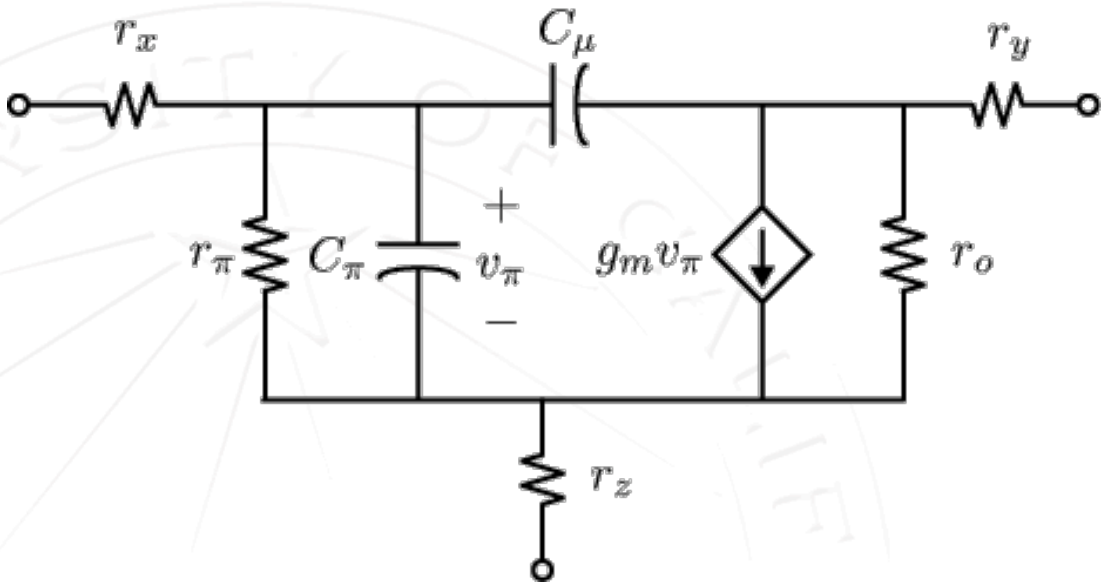
# Large Signal Models




- Resistors and capacitors are non-linear
  - $R_\pi$ and $R_o$ depend on bias point
  - $R_g$ (intrinsic) depends on channel inversion level
  - $R_b$ can change due to current spreading effects
  - $C_{gs}$ varies from accumulation to depletion to inversion
  - Junction capacitors vary with bias

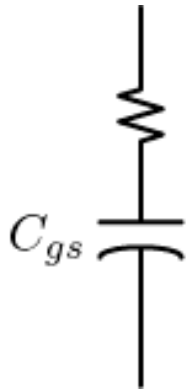
# Small Signal Models




- In small signal regime, R & C linear about a bias point:

For BJT:
$r_x = r_b$

For a FET input: ⇨




$$R_g = R_{nqs} + \frac{1}{d} R_{poly}$$

$$d = 3 \leftrightarrow 12$$

$$R_{nqs} \sim \frac{1}{5 g_m}$$

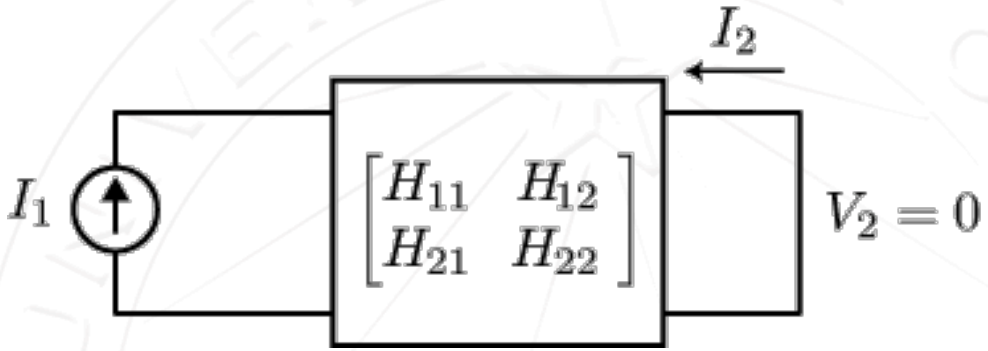
# Various Figures of Merit

- Intrinsic Voltage Gain ($a_0$)
- Power Gain
- Unilateral Gain
- Noise
  - Noise figure ($NF$) and $M$ (Noise Measure)
  - Flicker noise corner frequency
- Unity Gain Frequency $f_{T,}$ Maximum Osc. Freq $f_{max}$
- Gain (normalized to current): $g_m/I$
- Gain Bandwidth: $f_T \times g_m/I$

# Other Important Metrics

- Complementary devices
  - Device with same order of magnitude of $f_T/f_{max}$
  - Lateral pnp a "dog" compared to vertical npn
- Availability of Logic
  - Low power/high density
  - Useful with S/H (sample hold) and SC (switch capacitor) circuits
  - Important for calibration
- Breakdown voltage
  - Power amplifiers, dynamic range of analog circuitry
- Thermal conductivity
  - Power amplifiers
- Quality and precision of passives
  - Inductors, capacitors, resistors, and transmission lines

# Device Current Gain




H-parameters:

$$V_1 = H_{11}I_1 + H_{12}V_2$$

$$I_2 = H_{21}I_1 + H_{22}V_2$$

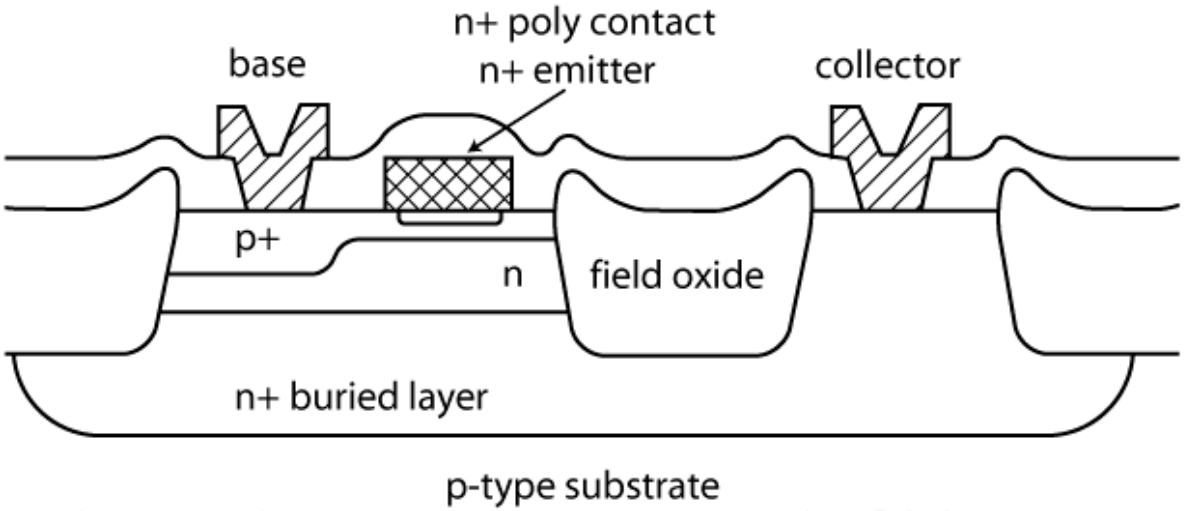
Current gain:

$$G_i = H_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0}$$

$$G_i = g_m \times \frac{1}{j\omega C_i} \times \frac{j\omega C_i}{j\omega C_i + G_\pi} = \frac{g_m}{j\omega C_i + G_\pi} \approx \frac{g_m}{j\omega C_i}$$

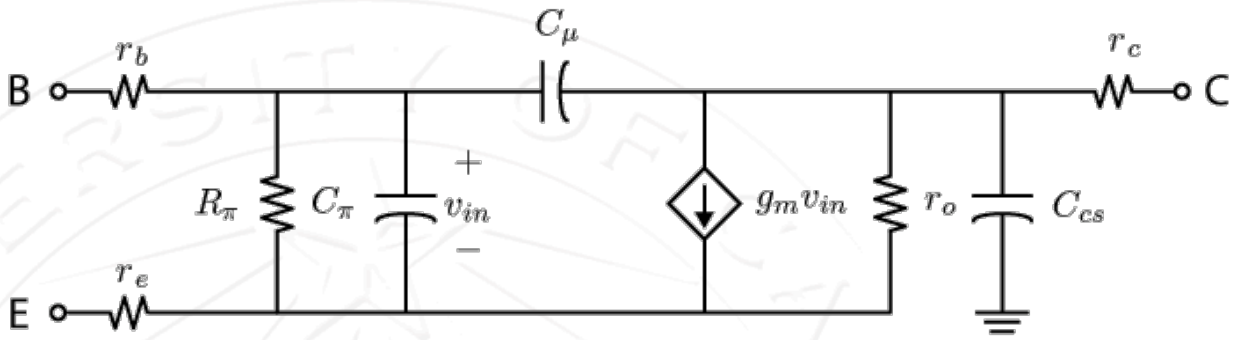
$$|G_i| = 1 = \frac{g_m}{\omega_T C_i} \qquad \boxed{\omega_T \equiv \frac{g_m}{C_i}} \longrightarrow G_i \approx \frac{\omega_T}{j\omega}$$

# BJT Cross Section




- Most transistor "action" occurs in the small npn sandwich under the emitter. The base width should be made as small as possible in order to minimize recombination. The emitter doping should be much larger than the base doping to maximize electron injection into the base.
- A SiGe HBT transistor behaves very similarly to a normal BJT, but has lower base resistance rb since the doping in the base can be increased without compromising performance of the structure.

# Bipolar Small-Signal Model




- The resistor $R_\pi$, dominates the input impedance at low frequency. At high frequency, though, $C_\pi$ dominates.
- $C_\pi$ is due to the collector-base reverse biased diode capacitance. $C_{cs}$ is the collector to substrate parasitic capacitance. In some processes, this is reduced with an oxide layer.
- $C_\pi$ has two components, due to the junction capacitance (forward-biased) and a diffusion capacitance

$$C_\pi = C_{bje} + C_{diff}$$

# Bipolar Exponential

- Due to Boltzmann statistics, the collector current is described very accurately with an exponential relationship

$$I_C \approx I_S e^{qV_{BE}kT}$$

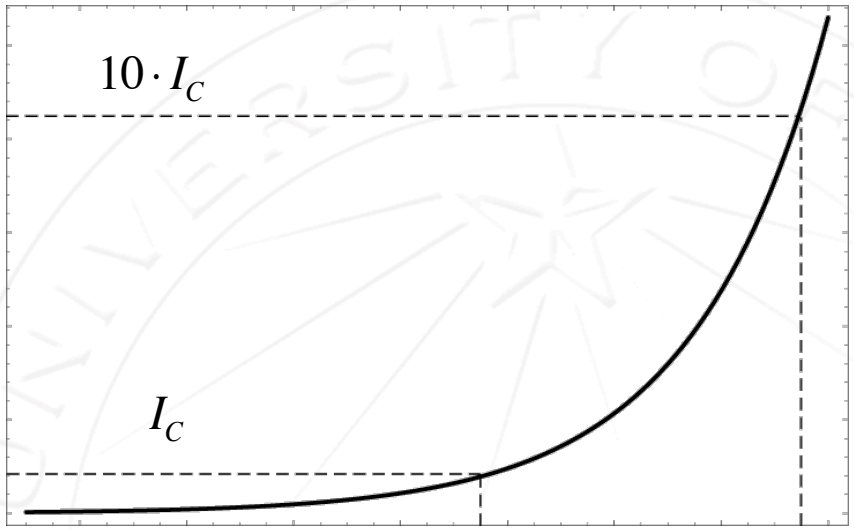
- The device transconductance is therefore proportional to current

$$g_m = \frac{\partial I_C}{\partial V_{BE}} = I_S \frac{q}{kT} e^{\frac{qV_{BE}}{kT}} = \frac{qI_C}{kT}$$

- where kT/q = 26mV at room temperature. Compare this to the equation for the FET. Since we usually have kT/q < ($V_{gs}$ -$V_T$ ), the bipolar has a much larger transconductance for the same current. This is the biggest advantage of a bipolar over a FET.

# Control Terminal Sensitivity




BJT:

$$10 = \exp\left(\frac{q\Delta V_{BE}}{kT}\right)$$

$$\Delta V_{BE} = \frac{kT}{q} \times \ln 10 \approx 60\text{mV}$$

MOSFET: $\Delta V_{GS} = \frac{1-\sqrt{10}}{\sqrt{10}}\left(V_{GS,1} + V_T\right) \sim 1\text{V}$

$$10 = \left(\frac{V_{GS,1} - V_T}{V_{GS,2} - V_T}\right)^2$$

$$\sqrt{10} = \frac{V_{GS,1} - V_T}{V_{GS,1} + \Delta V_{GS} - V_T}$$

# Bipolar Unity Gain Frequency

- The unity gain frequency of the BJT device is given by

$$\omega_T = \frac{g_m}{C_\pi + C_\mu} = \frac{g_m}{C_{diff} + 2C_{bej0} + C_\mu}$$

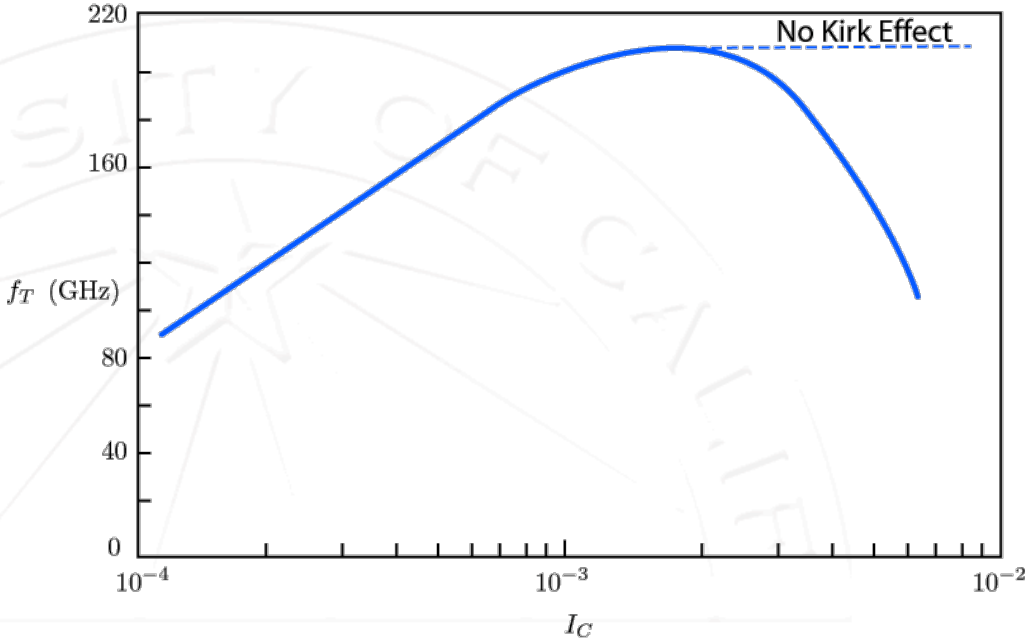
- where we assumed the forward bias junction has $C_{je} \sim 2\ C_{je0}$
- Since the base-collector junction capacitance $C_\pi$ is a function of reverse bias, we should bias the collector voltage as high as possible for best performance.
- The diffusion capacitance is a function of collector current

$$\omega_T = \frac{g_m}{C_\pi + C_\mu} = \frac{g_m}{g_m\tau_F + 2C_{bej0} + C_\mu}$$

$$\omega_T = \frac{g_m}{C_\pi + C_\mu} = \frac{1}{\tau_F + \frac{2C_{bej0}+C_\mu}{g_m}}$$

# Bipolar Optimum Bias Point



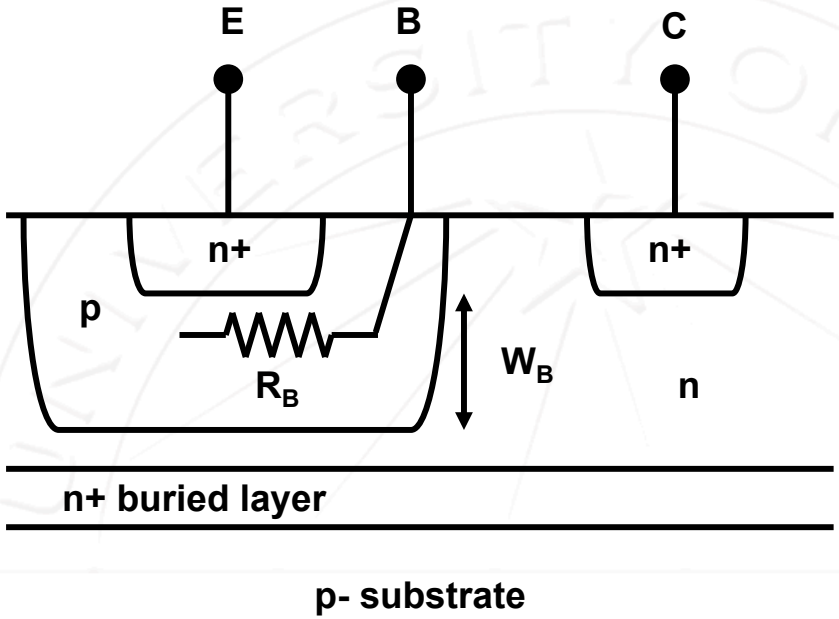

- We can clearly see that if we continue to increase $I_C$, then $g_m$ / $I_C$ increases and the limiting value of $f_T$ is given by the forward transit time

$$\omega_T \rightarrow \frac{1}{\tau_F}$$

- In practice, though, we find that there is an optimum collector current. Beyond this current the transit time increases. This optimum point occurs due to the Kirk Effect. It's related to the "base widening" due to high level injection. (Not Star Trek!)

# BJT Base Transit Time




$$C_i = C_j + C_{diff} \approx C_{diff} = \tau_f \cdot g_m$$

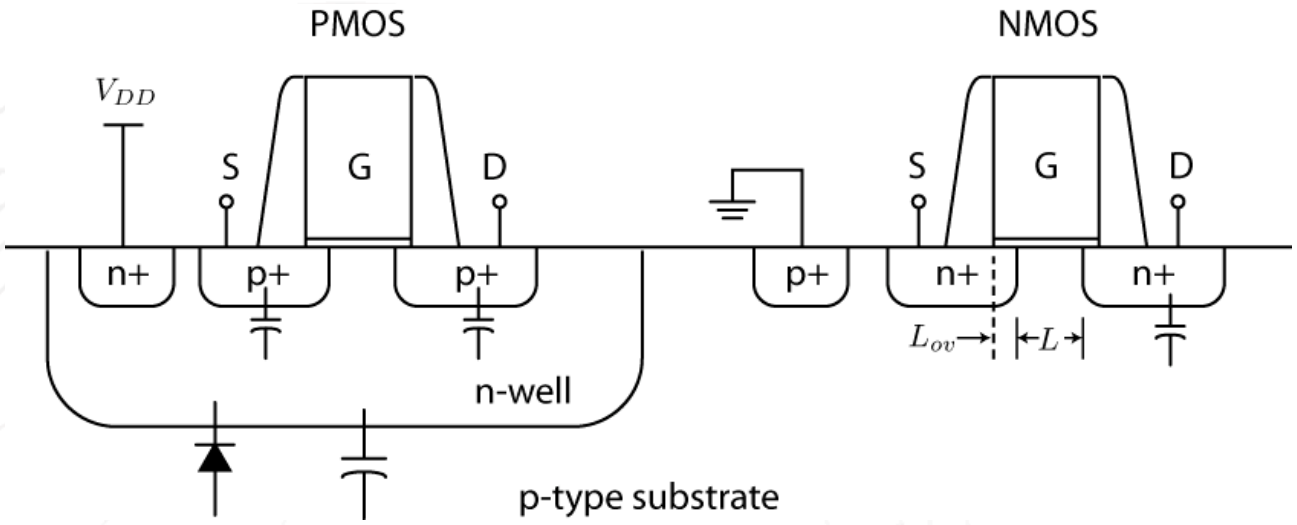
- Base transit time
- Current gain unity freq.

$$f_T = \frac{g_m}{2\pi C_i} \approx \frac{1}{2\pi \tau_f}$$

$$f_T \approx \frac{2\mu_n}{2\pi W_B^2}\frac{kT}{q}$$

$$f_T \propto \frac{1}{W_B^2}$$

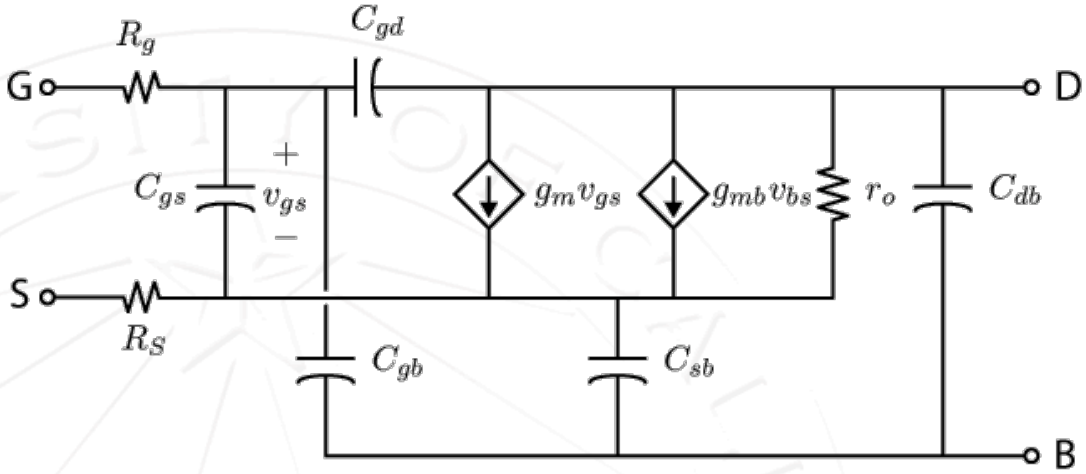
# CMOS Cross Section




- Modern CMOS process has very short channel lengths (L < 100 nm). To ensure gate control of channel, as opposed to drain control (DIBL), we employ thin junctions and thin oxide (tox < 5 nm).
- Due to lithographic limitations, there is an overlap between the gate and the source/drain junctions. This leads to overlap capacitance. In a modern FET this is a substantial fraction of the gate capacitance (up to half).

# FET Small Signal Model




- The junctions of a FET form reverse-biased pn junctions with the substrate (well), or the body node. This is another form of parasitic capacitance in the structure, $C_{db}$ and $C_{sb}$.
- At DC, input is an open circuit. The input impedance has a small real part due to the gate resistance $R_g$ (polysilicon gate and NQS) and $R_{s,d}$ account for junction and contact resistance.
- In the forward active (saturation) region, the input capacitance is given by $C_{gs}$

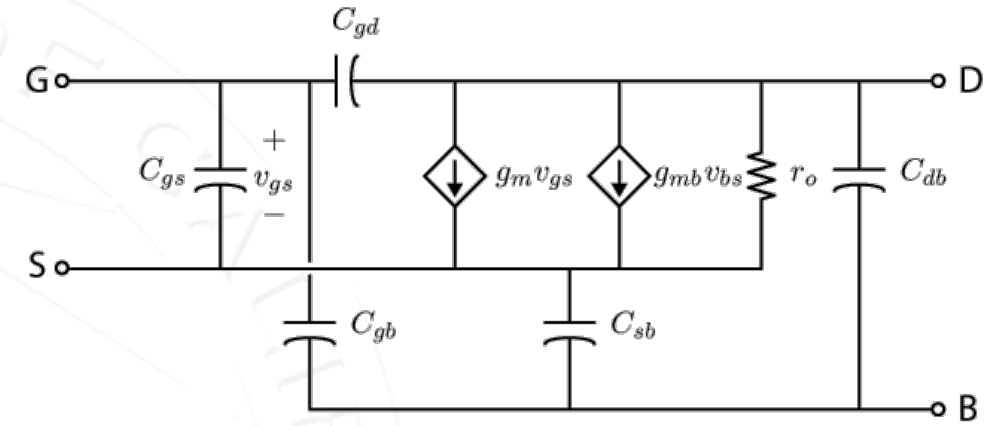
$$C_{gs} = \frac{2}{3} W \cdot L \cdot C_{ox}$$

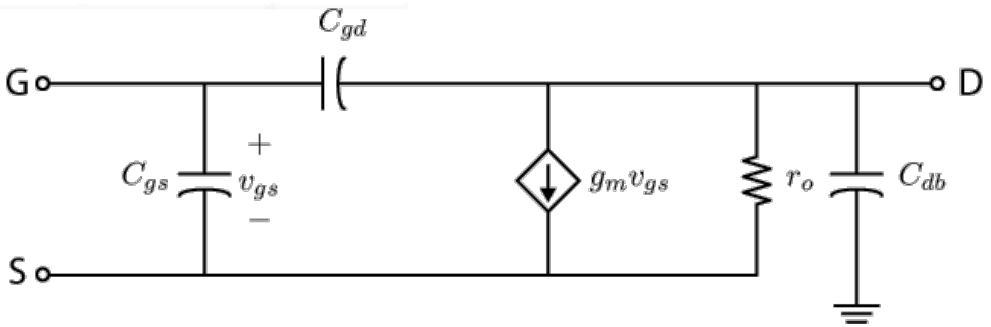
- $R_o$ is due to channel length modulation and other short channel effects (such as DIBL).

# FET Simplified Models

- For low frequencies, the resistors are ignored. But these resistors play an important role at high frequencies.
- If the source is tied to the bulk, then the model simplifies a lot more.
- Don't forget that layout parasitics increase the capacitance in the model, sometimes substantially (esp in deep submicron technologies).



# FET Unity Gain Frequency

- Long channel FET:
- Note that there is a peak $f_T$ since eventually the mobility of the transistor drops due to high vertical fields
- Short channel limit

$$f_T \approx \frac{1}{2\pi}\frac{g_m}{C_{gs}+C_{gb}+C_{gd}}$$

$$C_{gs} >> C_{gb}+C_{gd}$$

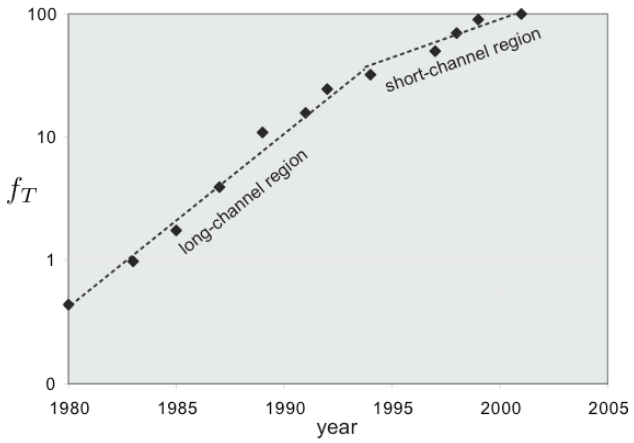
$$f_T \approx \frac{1}{2\pi}\frac{g_m}{C_{gs}} = \frac{3}{2}\frac{\mu_n}{2\pi L^2}(V_{GS}-V_T)$$

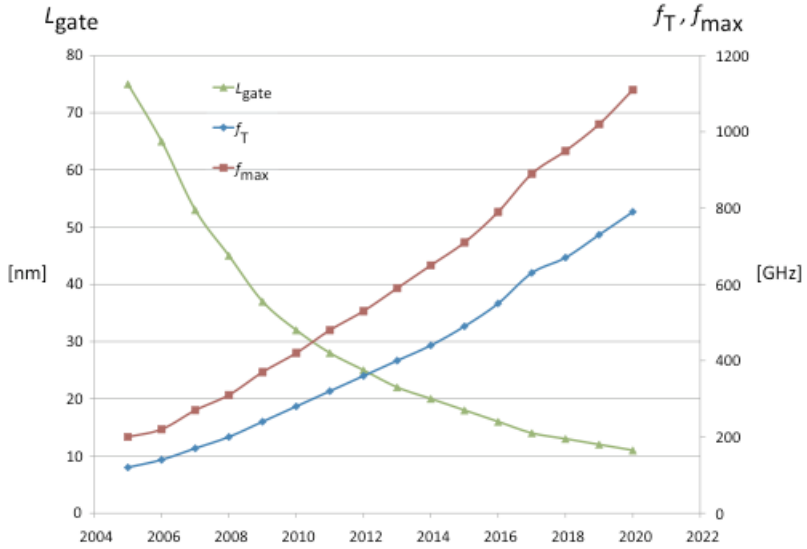
Bias dependent

$$I_{DS} \approx v_{sat}Q_{inv}W = WC_{ox}(V_{GS}-V_T)v_{sat} \rightarrow g_m = WC_{ox}v_{sat}$$

$$f_T = \frac{g_m}{C_{gs}} = \frac{3}{2}\frac{WC_{ox}v_{sat}}{WLC_{ox}} \propto \frac{1}{L}$$

# Scaling Speed Improvements




- CMOS transistors have steadily improved in performance just as predicted by theory. In the short channel regime the improvements are linear with scaling.
- At the same time, the decreasing supply voltage has led to a reduced dynamic range. Also the maximum gain has not improved as much…

# Intrinsic Voltage Gain

- Important metric for analog circuits

$$A_{v,mos} = g_m r_o = \frac{2I_{DS}}{V_{dsat}} \frac{V_A}{I_{DS}} = 2\frac{V_A}{V_{dsat}}$$

$$A_{v,bjt} = g_m r_o = \frac{qI_C}{kT} \frac{V_A}{I_C} = \frac{V_A}{\frac{kT}{q}}$$

- Communication circuits often work with low impedances in order to achieve high bandwidth, linearity, and matching.
- Inductive loads are also common to tune out the load capacitance and form a resonant circuit. The gain is thus given by

$$A_v = g_m R_p = g_m \omega_o Q L$$

- To achieve high $f_T$, the $V_{dsat}$ is relatively large so the current is increased to obtain sufficient gain.

# Normalized Gain

- For a bipolar device, the exponential current relationship results in a high constant normalized gain

$$\frac{g_m}{I_Q} = \frac{q}{kT} \approx \frac{1}{26\text{mV}}$$

- For a square law MOSFET, in saturation we have

$$\frac{g_m}{I_D} = \frac{2}{V_{GS} - V_T}$$

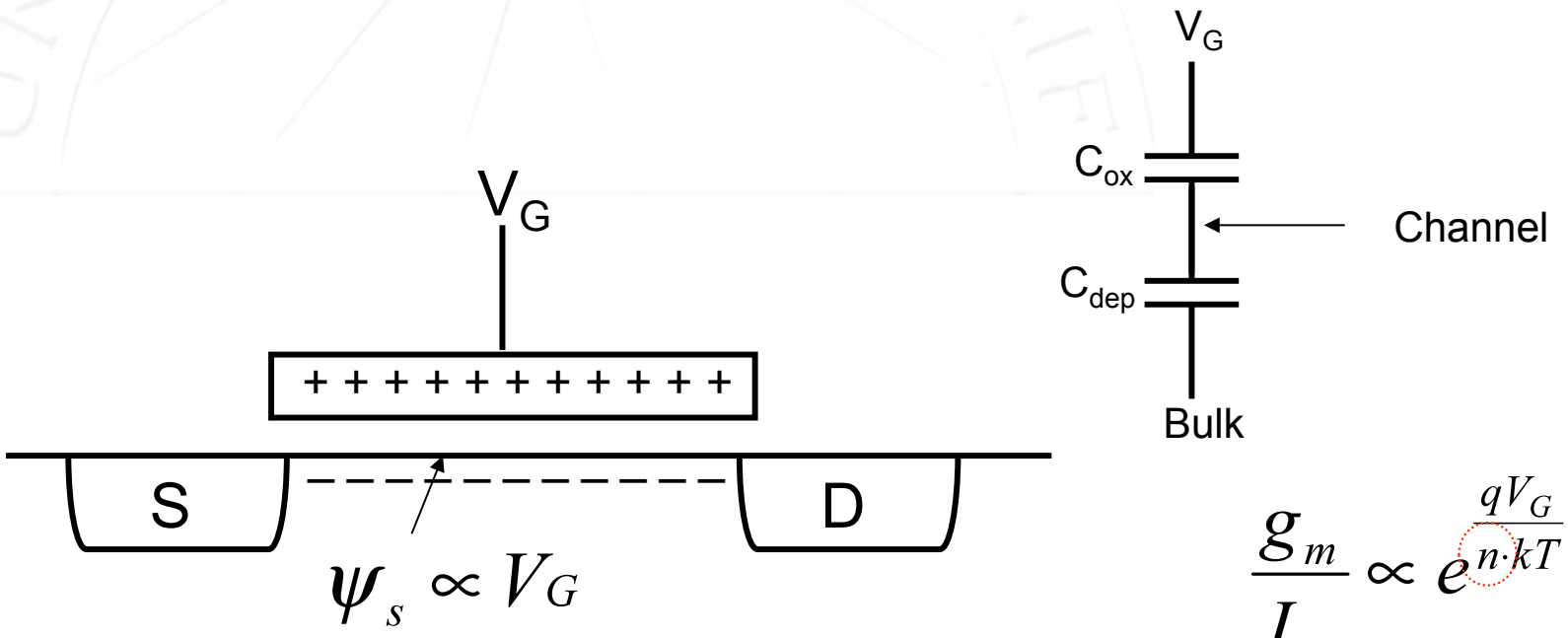
- In weak inversion, the MOSFET is also exponential

$$\frac{g_m}{I_Q} = \frac{q}{nkT} \approx \frac{1}{26\text{mV}} \frac{1}{n}$$

- The factor $n$ is set by the ratio of oxide to depletion capacitance

# MOSFET in subthreshold

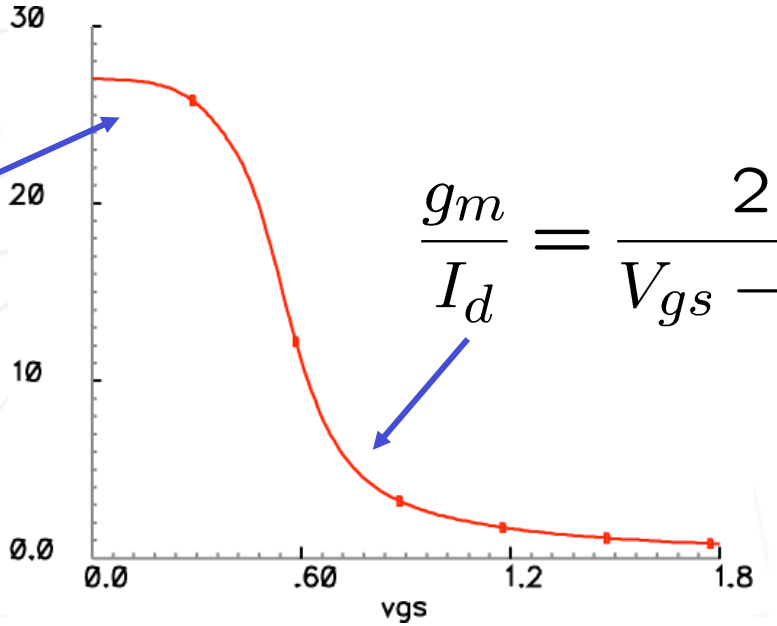
- In sub-threshold, the surface potential varies linearity with $V_G$
- The surface charge, and hence current, is thus exponentially related to $V_G$



# MOS Transconductor Efficiency

$$\frac{g_m}{I_d} = \frac{1}{n\frac{kT}{q}}$$




$$\frac{g_m}{I_d} = \frac{2}{V_{gs} - V_T} = \frac{2}{V_{dsat}}$$

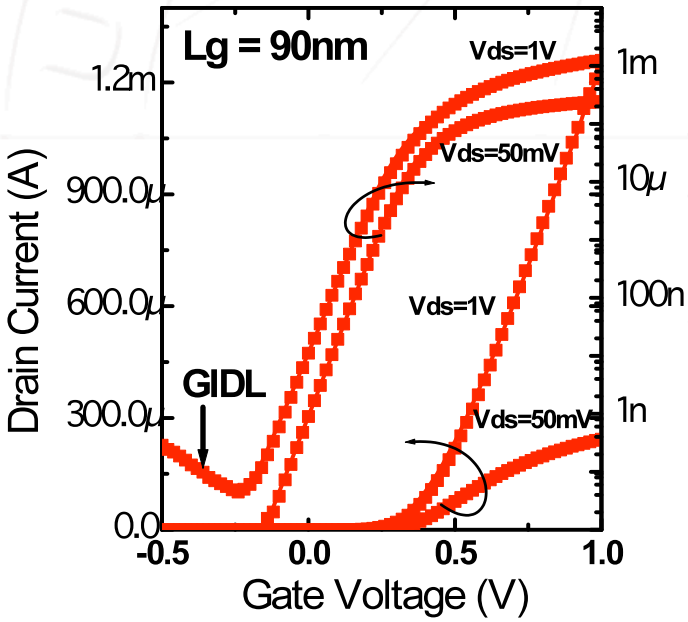
- Since the power dissipation is determined by and large by the DC current, we'd like to get the most "bang" for the "buck".
- From this perspective, the weak and moderate inversion region is the optimal place to operate.
- The price we pay is the speed of the device which decreases with decreasing $V_{GS.}$ Current drive is also very small.

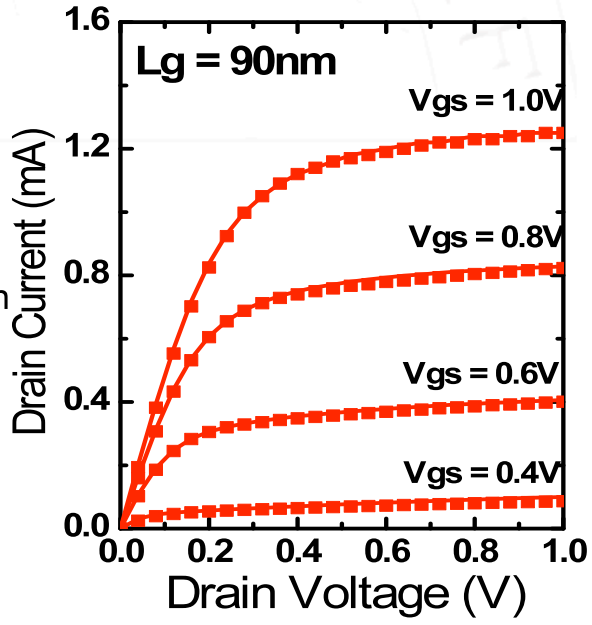
# I-V Curves of Interest

- Typical I-V curves used to evaluate a technology/model:

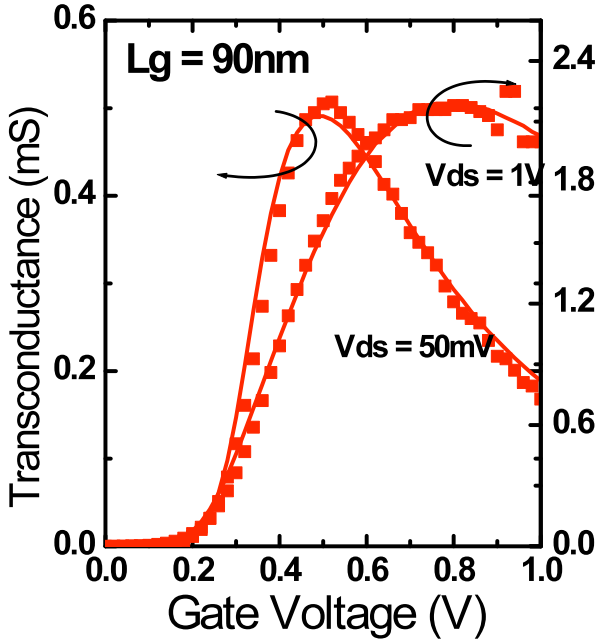
**Drain Current v.s Vgs (Lg = 90nm)**




**Drain Current v.s. Vds (Lg = 90 nm)**



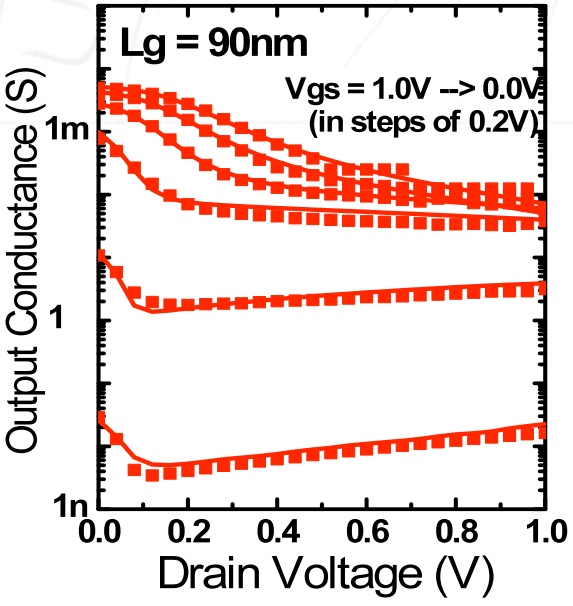

**Transconductance (Lg = 90nm)**



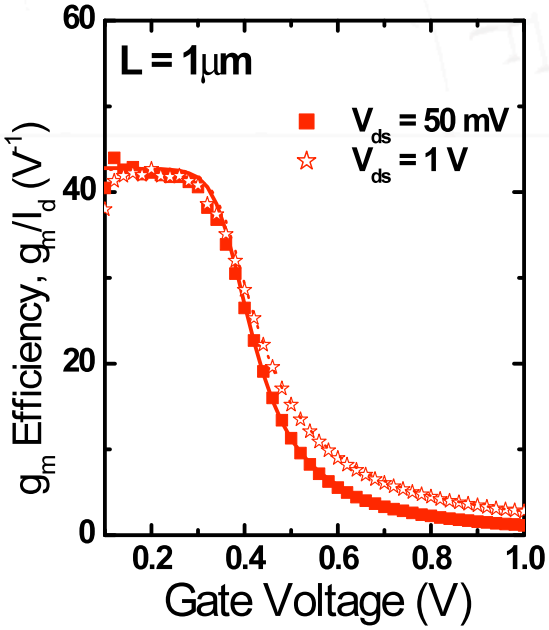
# I-V Derivatives of Interest

- Most analog/RF circuits depend on the derivatives of the I-V relations (gm and ro)

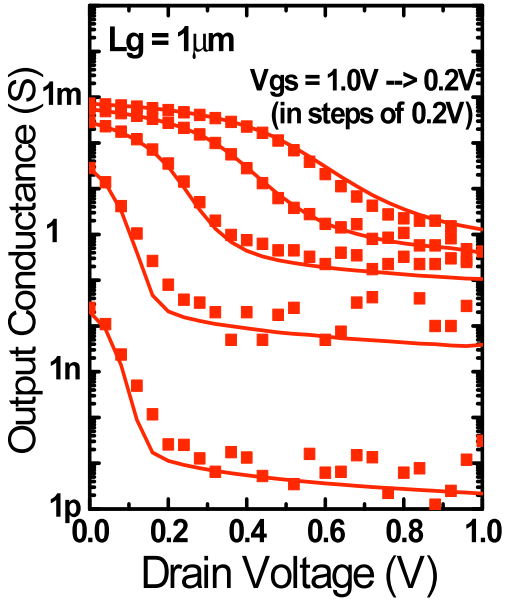
**Output Conductance (Lg = 90 nm)**




**Gm / Id (Lg = 1 µm)**




**Output Conductance (Lg = 1 µm)**



# High BJT Transconductance

$$g_m = \frac{\partial I_C}{\partial V_i} = \frac{q}{kT} \cdot I_S e^{\frac{qV_{BE}}{kT}} = \frac{qI_C}{kT}$$

⇨ for fixed current, BJT gives more gain

- Precision
  - Important in multiplication, log, and exponential functions
  - More difficult in FETs due to process/temp. dependence
  - $I_S$ process dependent in BJT … use circuit tricks

# Advantages of BJT

$$\frac{g_m}{I_C} = \frac{q}{kT} = \frac{1}{25\,\text{mV}}$$

$$\frac{g_m}{I_{DS}} = \frac{2}{V_{GS} - V_T} \approx \frac{1}{250mV}$$

$$\frac{g_m}{I_C} \propto e^{-E/kT} \propto e^{qV_{BE}/kT}$$

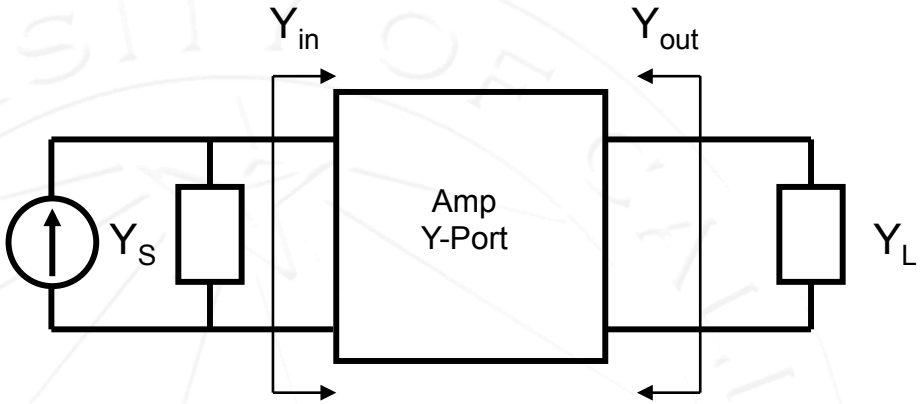
For high-speed applications,

Need to bias in strong inversion…

Results in ~10x lower efficiency

- For a BJT, this relationship is fundamental and related to the Boltzman statistics (approximation of Fermi-Dirac statistics)
- For a MOSFET, this relationship is actually only valid for a square-law device and varies with $V_T$ (body bias) and temperature

# Maximum Two-Port Power Gain




Condition: measure at maximum gain $G_{max}$

$$Y_S = Y_{in}^*$$

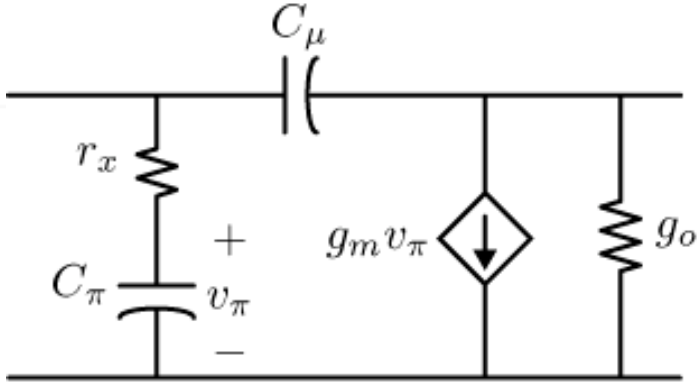
$$Y_L = Y_{out}^*$$

# Maximum Power Gain Fmax

$f_{max}$ = max. freq. of activity = freq. when {power gain = 1}

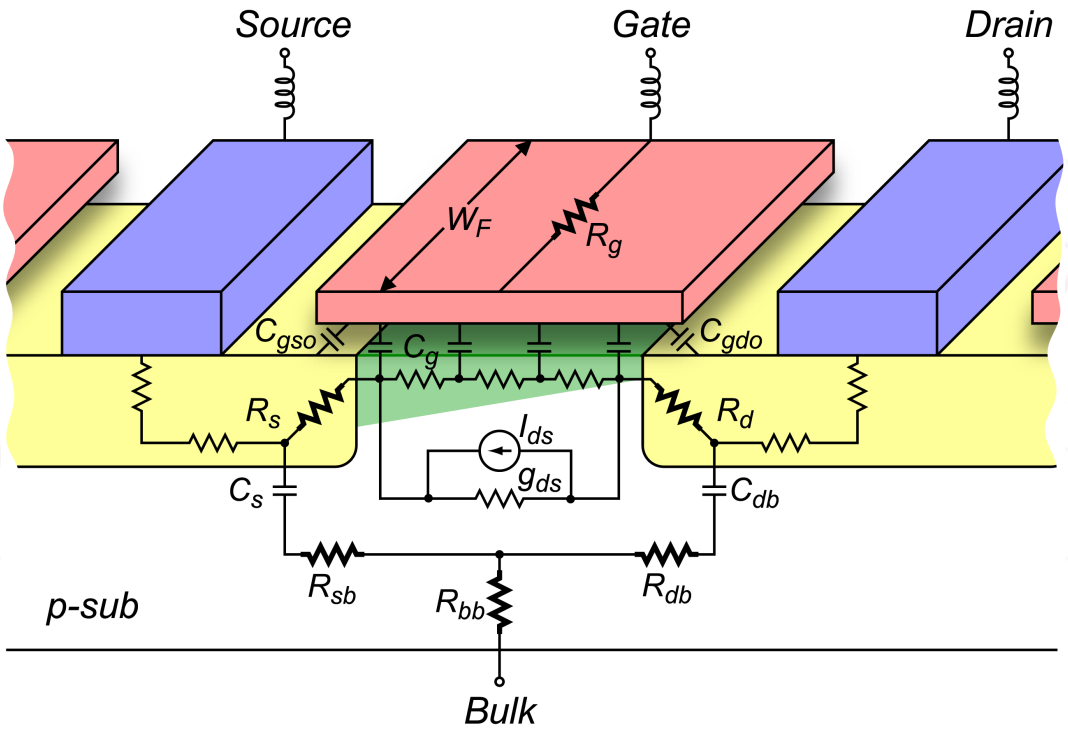
$$G_p \approx \frac{\left(\frac{f_T}{f}\right)^2}{4r_x\left(g_o + g_m\frac{C_\mu}{C_\pi}\right) + 4r_x g_o}$$

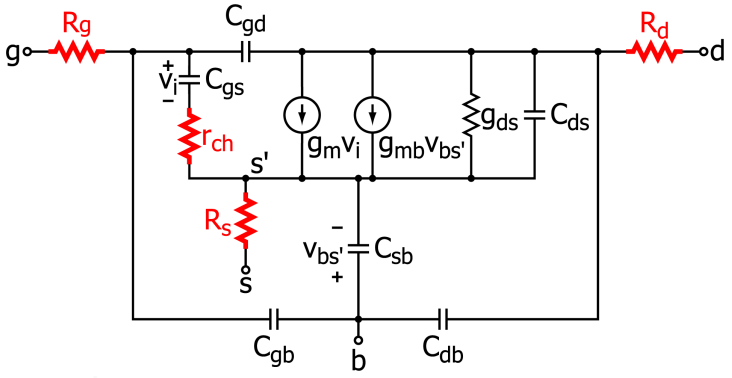



$$G_{max} \approx \frac{f_T}{8\pi r_x C_\mu f_{max}^2} = 1$$

$$f_{max} = \sqrt{\frac{f_T}{8\pi r_x C_\mu}}$$

# FET Fmax




$$f_t \approx \frac{g_m}{2\pi C_{gg}}$$

$$f_{max} \approx \frac{f_t}{2\sqrt{R_g(g_m C_{gd}/C_{gg}) + (R_g + r_{ch} + R_s)\, g_{ds}}}$$

## Minimize all resistances

- $R_g$ – use many small parallel gate fingers, <1 μm each
- $R_{sb}$, $R_{db}$, $R_{bb}$ – substrate contacts <1–2 μm from device
- $R_s$, $R_d$ – don't use source/drain extensions to reduce L

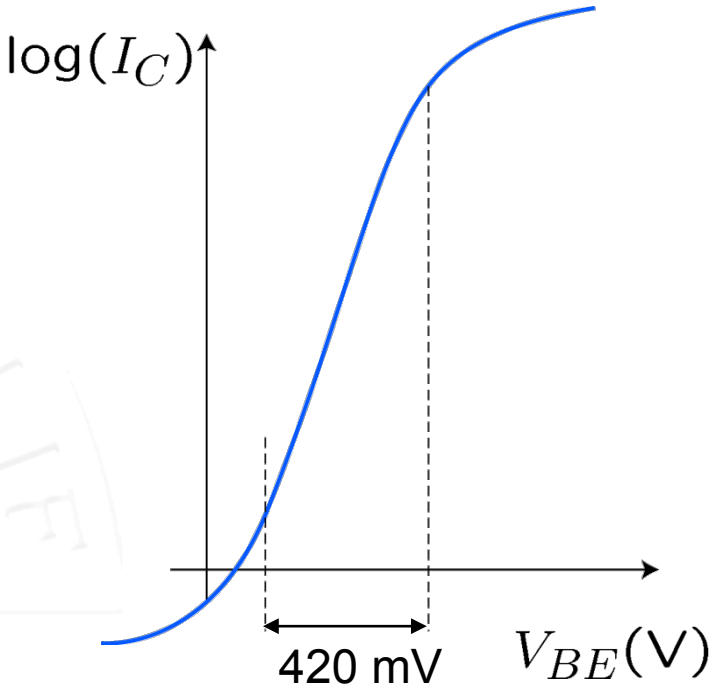
# Advantage of BJT over FET (2)

- Better precision
  - About 4 decades (420mV) of linearity
- Example:

$$V_{BE1} + V_{BE2} = V_{BE3}$$

$$V_{BE} = V_T \ln \frac{I_C}{I_S}$$

$$\frac{I_{C1} I_{C2}}{I_{S1} I_{S2}} = \frac{I_{C3}}{I_{S3}}$$




- Can build exp, log, roots, vector mag …
- Lower 1/f noise corner
- Lower offset voltage $V_{OS} \sim 1\text{mV}$

# Disadvantage of BJT

- $r_b$ → hurts gain (power), NF
  - SiGe allows fast transistors with low $r_b$
- Exponential transfer function (advantage and disadvantage)
  - Exponential → non-linear → restoration
- Expensive
  - Lower volume than CMOS
- Absence of a switch

Old CMOS gets cheaper!
0.065um ~ $1M (mask)

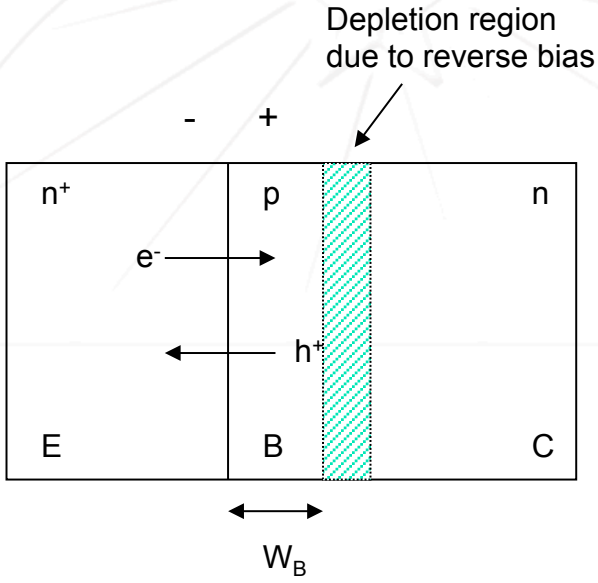
0.13um ~ $40k

# Advantage of FET over BJT

- Cheaper and more widely available (many fabs in US, Asia, and Europe)
- Square law → less distortion
- P-FET widely available
- Triode region → variable resistor
- Widely available digital logic
- Low leakage in gates
  - Sample and hold (S/H) and switch cap filters (SCF)
- Dense digital circuitry / DSP for calibration
  - Offset voltages and mismatches can be compensated digitally
- Dense metal layers allows MIM ("MOM") capacitors for free

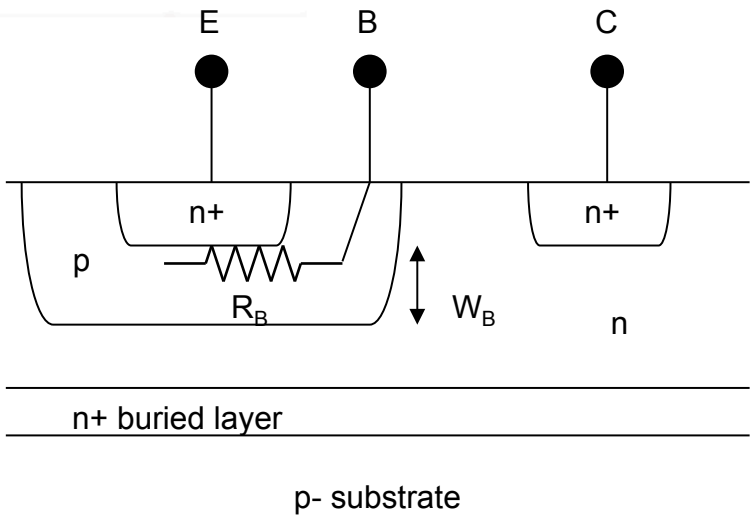
# SiGe Technology

Higher Performance: $f_T \geq 350\text{GHz}$




$$\beta = \frac{I_C}{I_B}$$

Problem:
As $W_B$ decreases → $r_b$ increases
Solution:
SiGe base allows for higher $f_T$ without reducing $W_B$

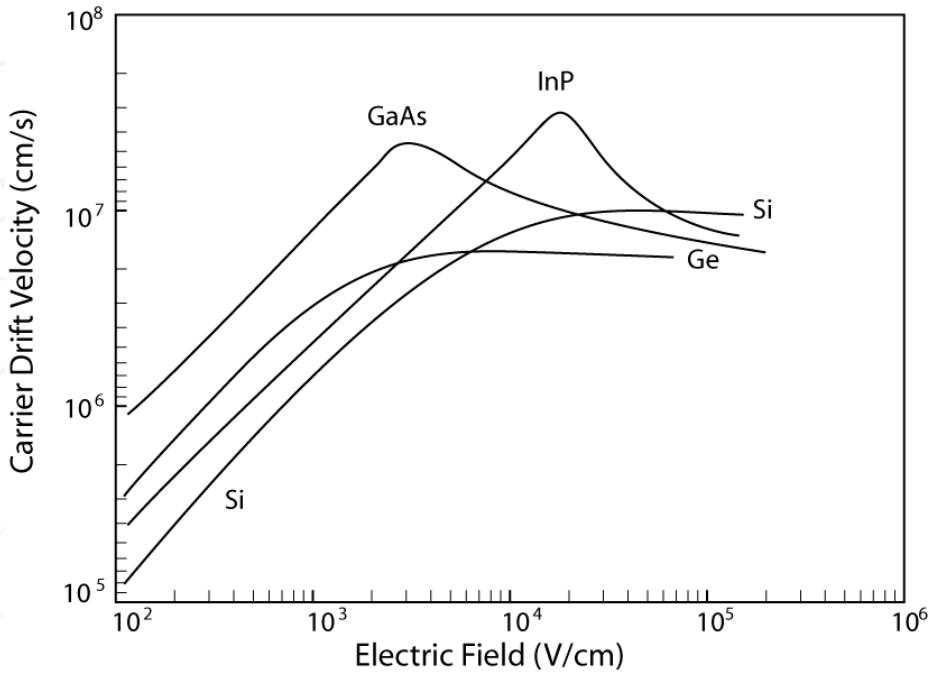


# SiGe HBT Action

- A SiGe BJT is often called a HBT (heterojunction bipolar transistor)
- Ge epitaxially grown in base
  - Causes strain in crystal
  - Causes extra potential barrier for holes (majority carrier) in the base from flowing into emitter
- Beneficial effects

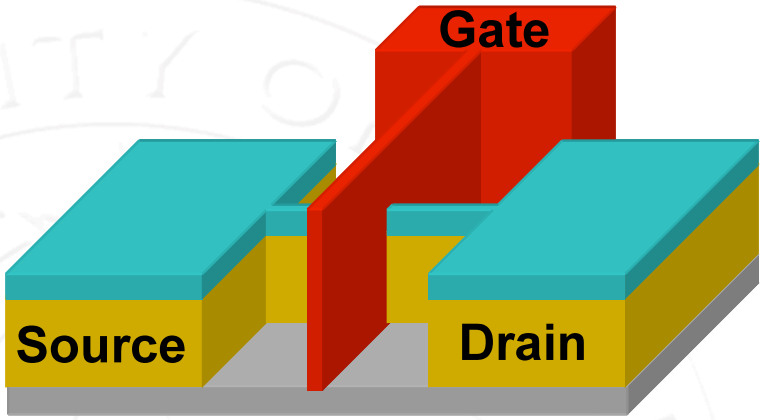
| | | |
|---|---|---|
| $W_B$ decreases | $N_B$ increases | $r_b$ low |
| $N_E$ decreases | $C_j$ decreases | |

# GaAs/InP Technology




- One of the primary advantages of the III-V based transistors is the higher peak mobility compared to Si.
- The insulating substrate also allows higher Q passives.
- The extra cost of these technologies limits it to niche applications such as very high frequencies, high performance, and power amplifiers.

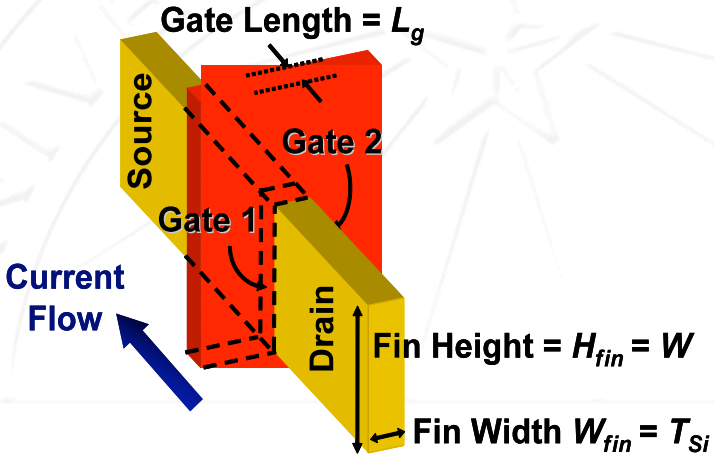
# FinFETs and Multigate Transistors

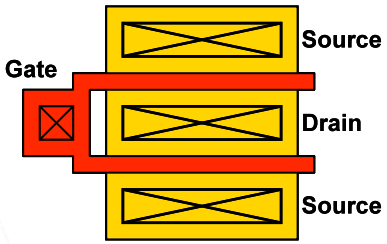



- To combat the problems with scaling of MOSFETs below 45nm, Berkeley researchers introduced the “FinFET”, a double gate device.
- Due to thin body and double gates, there is better “gate control” as opposed to drain control, leading to enhanced output resistance and lower leakage in subthreshold.

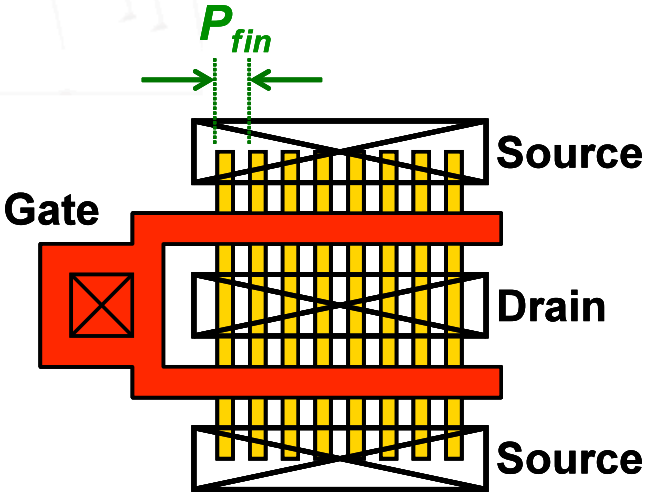
# FinFET Structure and Layout

- Gate straddles thin silicon fin, forming two conducting channels on sidewall




Bulk-Si MOSFET




Multi-fin layout

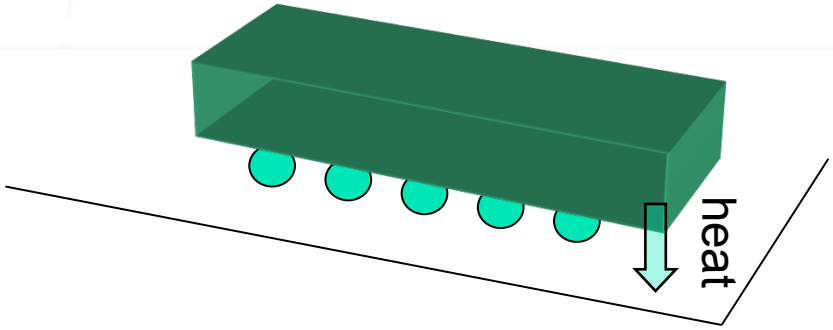
*Source (all images): T-J King, et al, "FinFET Technology Optimization…" presentation slides, Oct. 2003*

# An Aside on Thermal Conductivity

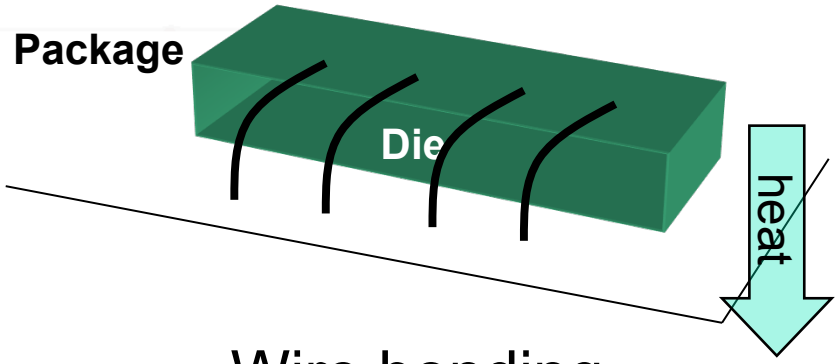
- GaAs
  - Semi-insulating substrate
  - Not very good conductor of heat
  - High quality passive elements (next topic)
- Si
  - Semi-conducting substrate
  - Good conductor of heat
  - Lossy substrate leads to lower quality passives

# An Aside on Thermal conductivity (2)

- Also depends on packaging
  - Example: in flip-chip bonding, thermal conductivity function of # of bumps rather than substrate
  - Back-side of die can lose heat through radiation or convection through air but thermal contact is much more effective




Flip chip bonding




Wire bonding

# References and Further Reading


- **UCB EECS 142/242 Class Notes** (Niknejad/Meyer)
- **UCB EECS 240 Class Notes**, (Niknejad/Boser)
- **Analysis and design of analog integrated circuits**, Paul R. Gray, Robert G. Meyer. 3rd ed. New York : Wiley, c1993.
- **Microwave CMOS-device physics and design,** Manku, T., *IEEE Journal of Solid-State Circuits*, vol.34, (no.3), March 1999. p.277-85. 32