Class E/F Amplifiers

Ali M Niknejad

Excerpts from the Ph.D. dissertation of Dr. Scott Kee

The Class E/F Family of Harmonic-Tuned Switching Power Amplifiers

Normalized Output Power

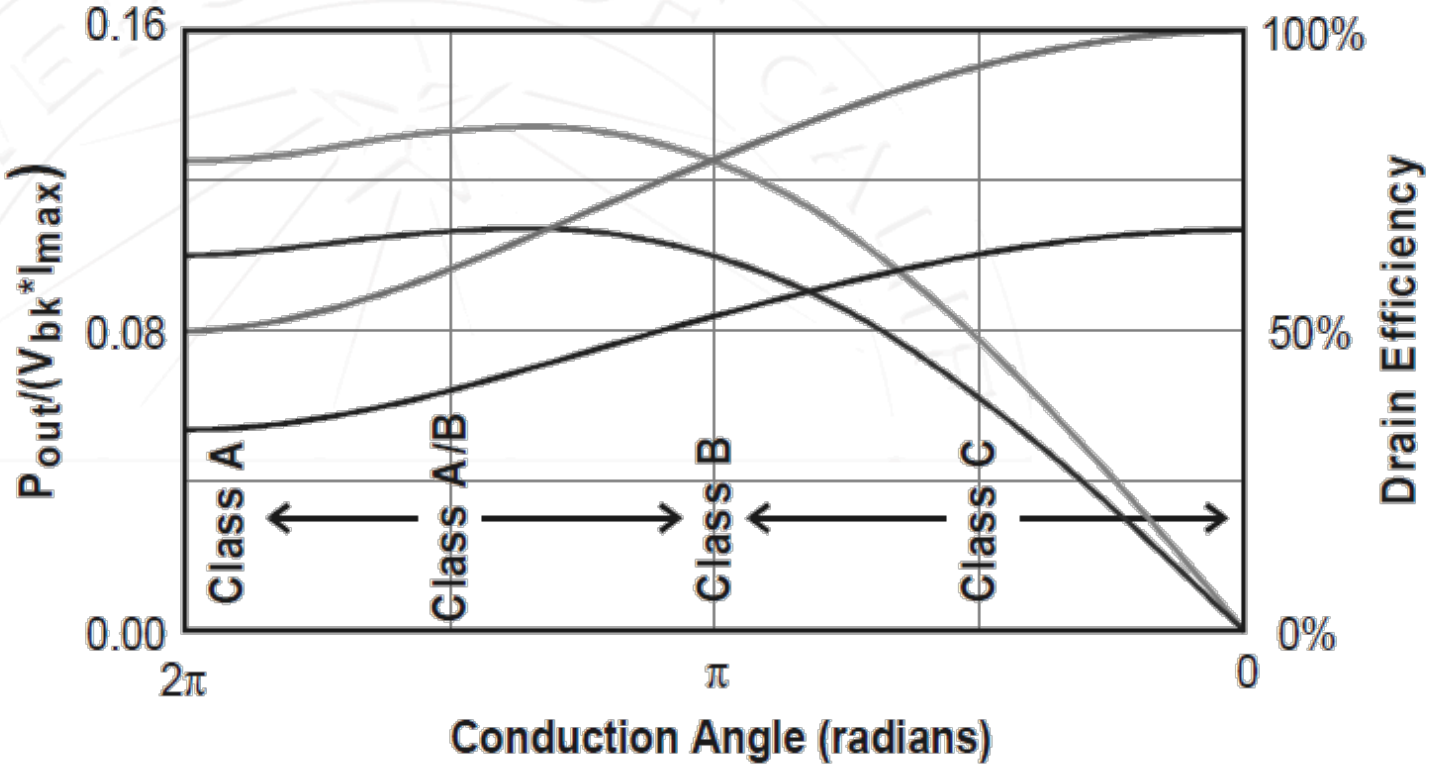
- It's easy to show that for Class A/B/C amplifiers, the efficiency and output power are given by:

$$\eta_D = \frac{1}{2} \cdot \left[\frac{1 - V_k / V_{bk}}{1 + V_k / V_{bk}} \right] \cdot \left[\frac{\alpha - \sin\alpha}{2\sin(\alpha/2) - \alpha\cos(\alpha/2)} \right]$$

$$P_{out} = \frac{1}{8\pi} \cdot \left[\frac{\alpha - \sin\alpha}{1 - \cos\alpha/2} \right] \cdot \left[1 - \frac{V_k}{V_{bk}} \right] \cdot V_{bk} \cdot I_{max}$$

- It's useful to normalize the output power versus the product of V_{bk} and I_{max} (I_{dc})

Class A/B/C

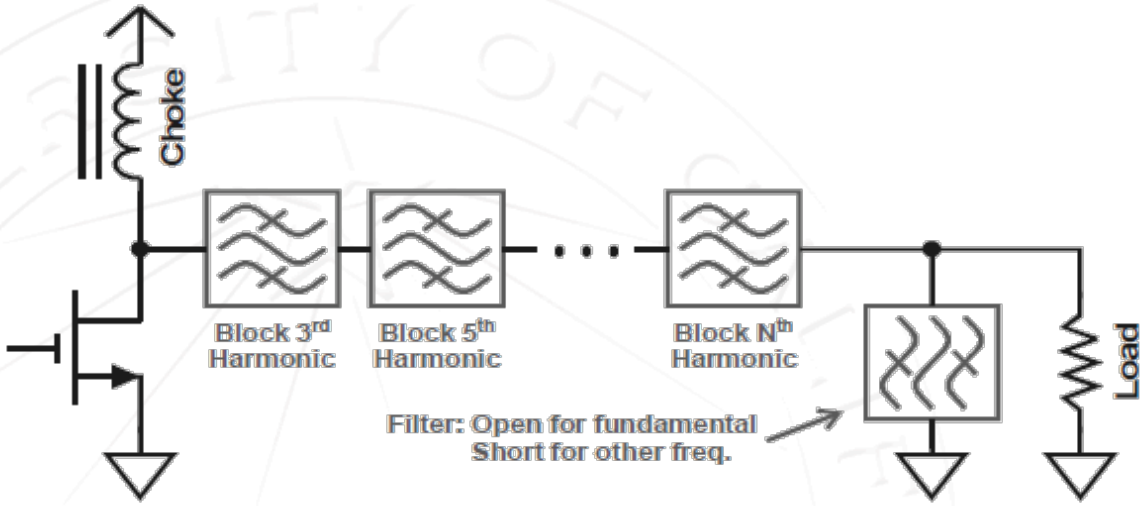


- As efficiency improves, the normalized output power drops from ~10% down to 0%

Class A/B/C Properties

- Keep voltage waveform sinusoidal → amplitude is limited to $V_{dd}/2$
- Only way to improve efficiency is to control current
- Require very large "on" current to deliver power

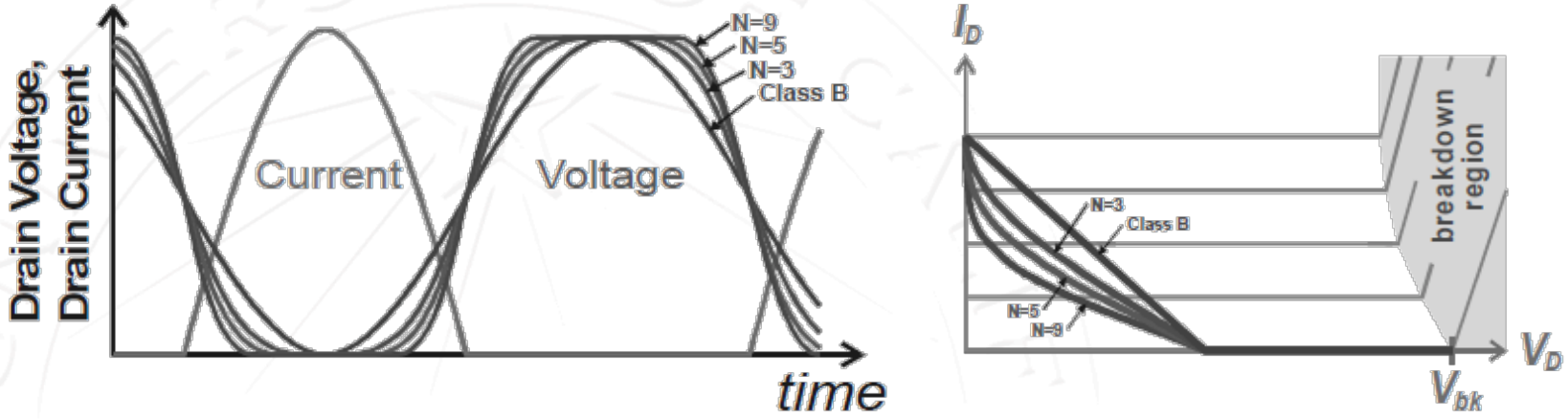
Class F



Class-F circuit conceptual implementation.

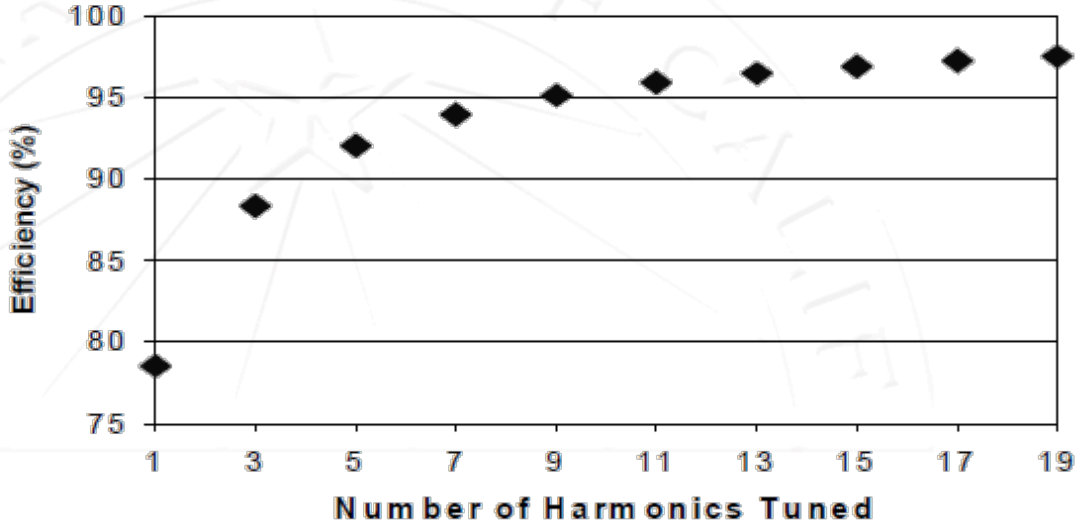
- Start with Class B current waveform → only odd harmonics
- Tune impedance at odd harmonics to be an open circuit to dissipate no harmonic power but allow odd harmonics in voltage waveform
- Tune even harmonics to short circuit to avoid dissipating power

Class F Waveforms



- Maximally flat Class F waveforms.
- An ideal Class F amplifier has a square voltage waveform and 100% efficiency.

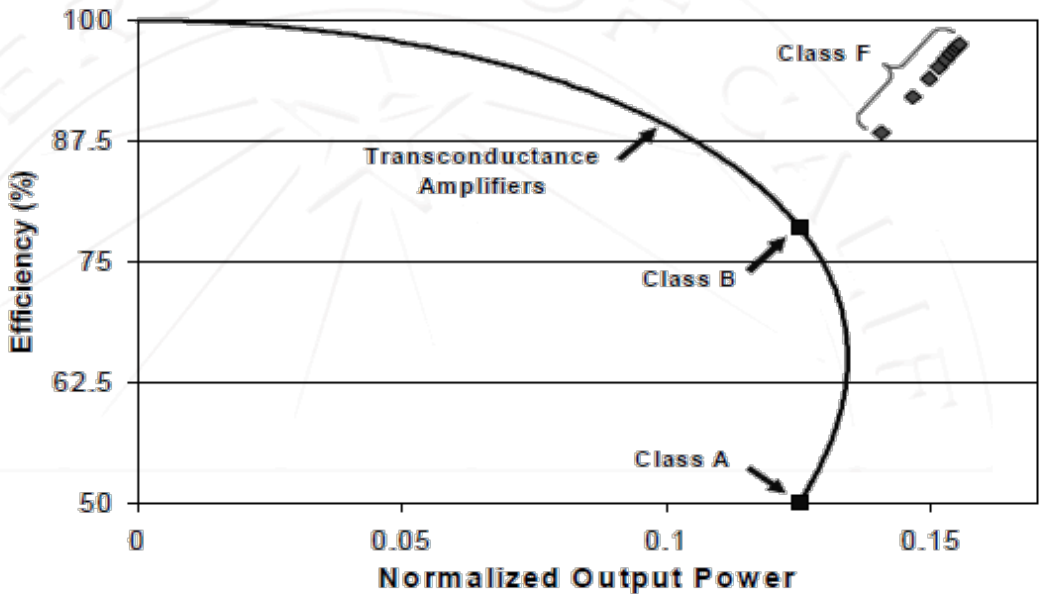
Class F Efficiency



Efficiency of maximally-flat voltage waveform class-F amplifiers with half-sinusoidal current for various numbers of voltage harmonics tuned.

- In theory, if you can control an infinite number of harmonics, efficiency approaches 100%

Class F Output Power



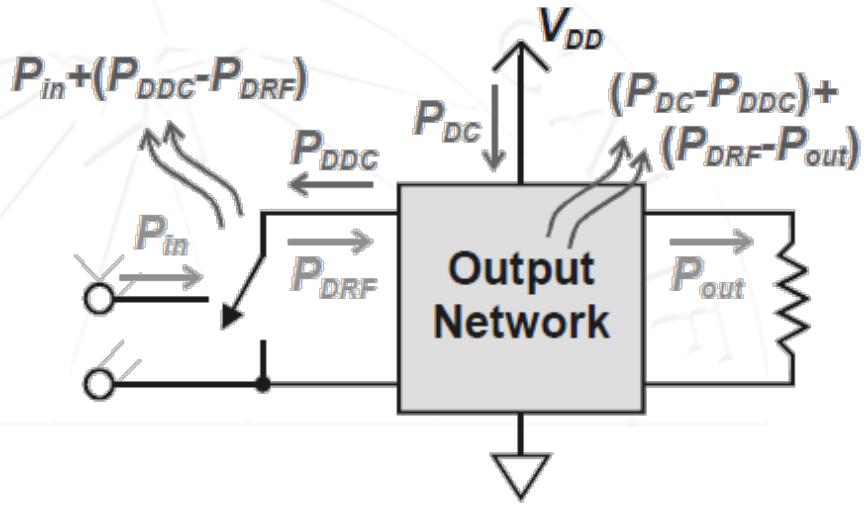
Efficiency vs. normalized output power for transconductance and class-F amplifiers. The output power is normalized to constant peak voltage and peak current.

- Square wave has a peak fundamental $4/\pi$ larger than the peak
  → 1 dB output power enhancement

Class F Disadvantages

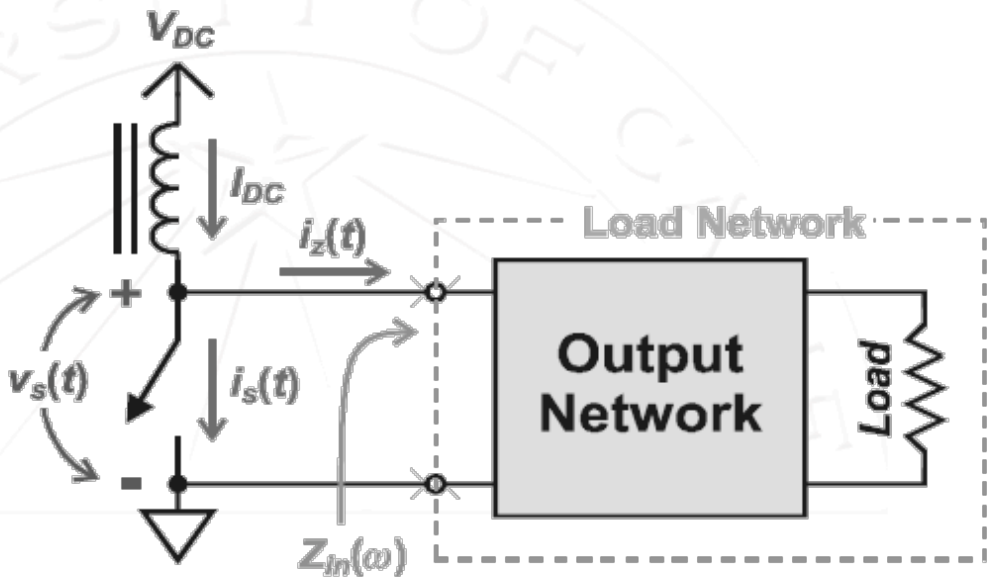
- Output capacitance of device not naturally absorbed into network → need inductor to tune it out
- Difficult to control more than 5^{th} harmonic … resonators are lossy and additional losses present diminishing returns on efficiency.

Switching Amplifiers



- Operate transistor in "triode" region where it acts like a switch.
- For an ideal switch the power dissipated in the switch is zero, right?
- Are all switching PA's the same?

Linear Time-Varying Systems

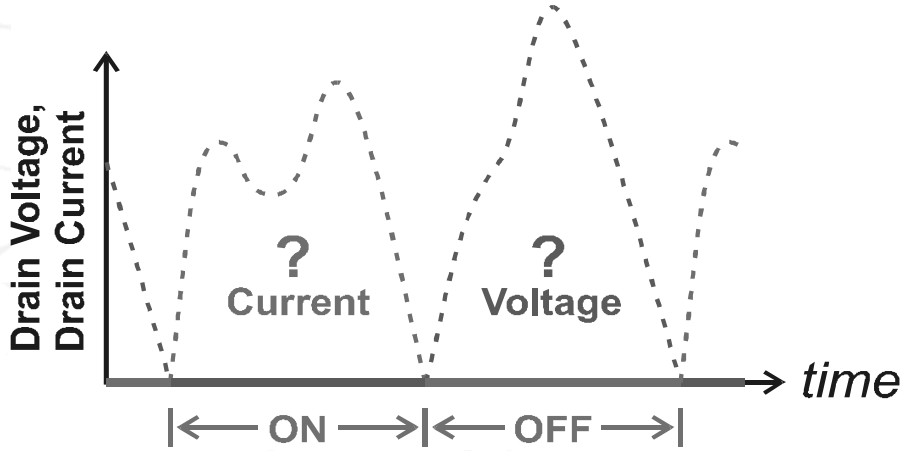


- Even though transistor is non-linear, the operation of the periodic switching action can be modeled as a linear time-varying (periodic) system. The design of the output network completely determines the behavior of the circuit.

I-V Solution for Swithing Amps

$$(\theta \in \boldsymbol{D}) \Rightarrow (v_s = 0)$$

$$(\theta \in \bar{\boldsymbol{D}}) \Rightarrow (i_s = 0)$$



- For trans-conductance amplifiers, the current is known, so the voltage is determined by the load network.
- In a switching amplifier, when the switch is on, the voltage is forced to zero, and the current through the switch can take on any value. Likewise, when the switch is off, the switch current is zero, but the voltage can take on any value

Impedance at Harmonics

$$v_s(\theta) = V_{DC} + \sum_{k=1}^{\infty} v_k \cos(k\theta + \alpha_k)$$

$$i_s(\theta) = I_{DC} + \sum_{k=1}^{\infty} i_k \cos(k\theta + \beta_k)$$

$$\underbrace{(v_k / i_k) e^{j(\alpha_k - \beta_k)} = Z_{in}(k)}_{\forall k \in \{1, 2, 3, 4, \ldots\}}$$

- The waveform shape, therefore, is completely determined by the load network impedance (it's a linear system viewed from this perspective)

Inverse Class of Operation

- By duality, any PA can be transformed into it's dual (where the role of current/voltage are switched) by imposing the complementary admittance condition
- For instance a Class D voltage switching amplifier can be transformed into a current switching amp

$$i_s(\theta) = I_{DC} + \sum_{k=1}^{\infty} i_k \cos(k\theta + \alpha_k)$$

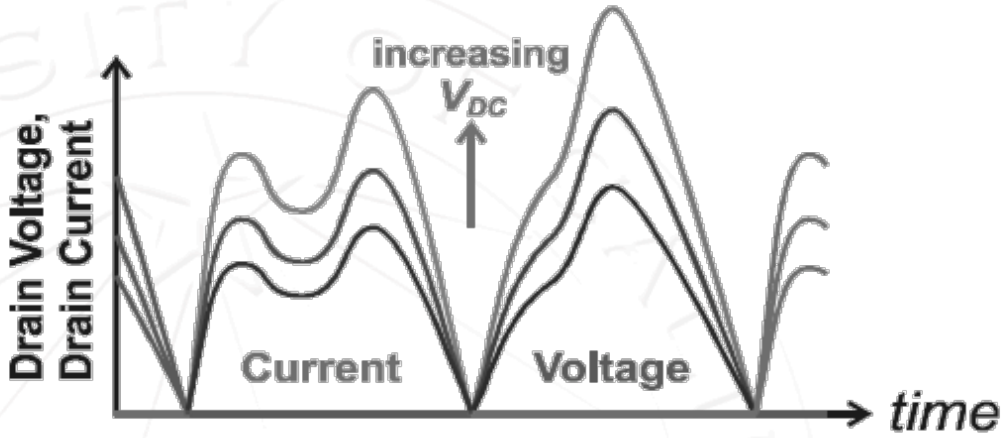
$$v_s(\theta) = V_{DC} + \sum_{k=1}^{\infty} v_k \cos(k\theta + \beta_k)$$

$$(\theta \in \boldsymbol{D}) \Rightarrow (i_s = 0)$$

$$(\theta \in \bar{\boldsymbol{D}}) \Rightarrow (v_s = 0)$$

$$\underbrace{(i_k / v_k) e^{j(\alpha_k - \beta_k)} = Y_{in}(k)}_{\forall k \in \{1, 2, 3, 4, \ldots\}}$$

Bias Scaling



$$V_{DC} \rightarrow \lambda V_{DC} \Rightarrow \begin{cases} i_s(\theta) \rightarrow \lambda i_s(\theta) \\ v_s(\theta) \rightarrow \lambda v_s(\theta) \end{cases}$$

$$\hat{i}(\theta) = \lambda i_s(\theta)$$

$$\hat{v}_s(\theta) = \lambda v_s(\theta)$$

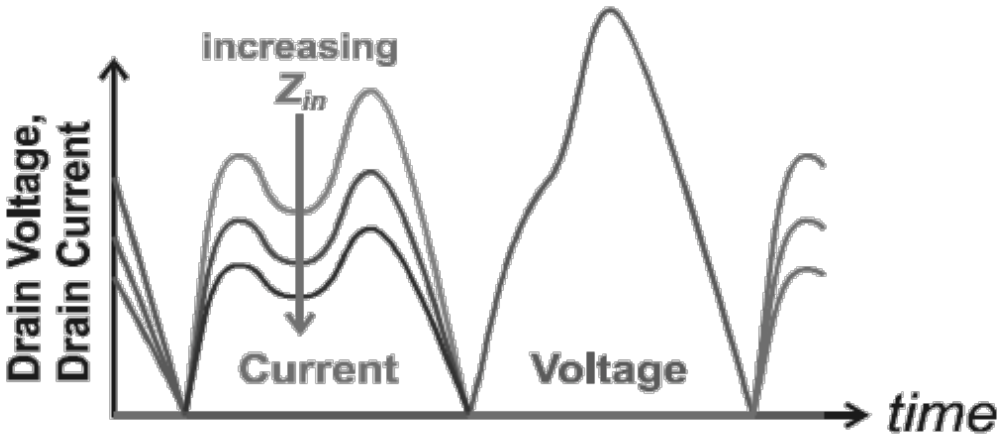
- Scaling supply changes voltage/current waveforms by the same scale factor.

Impedance Scaling

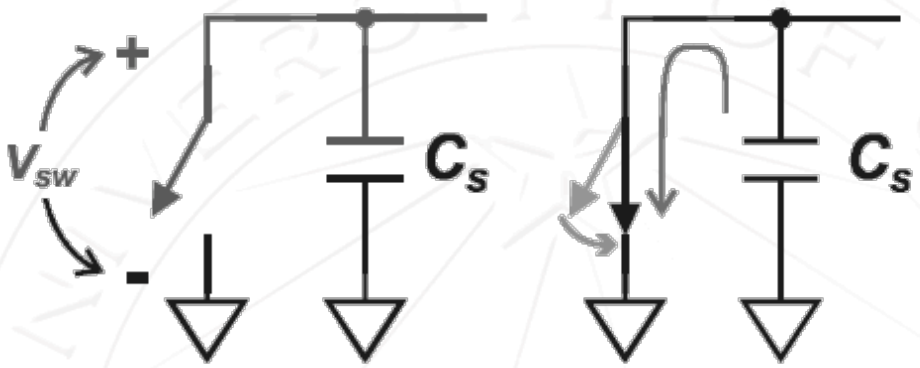
$$\hat{i}(\theta) = i_s(\theta)/\lambda$$

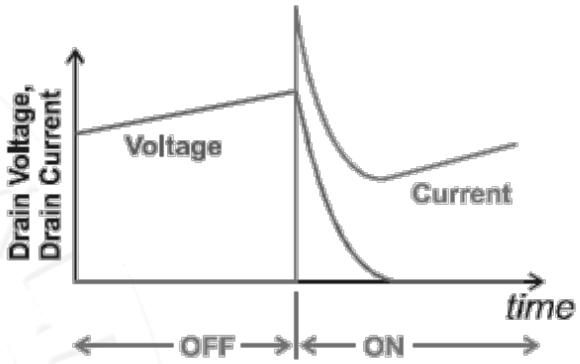
$$\hat{v}_s(\theta) = v_s(\theta)$$

$$\underbrace{Z_{in}(k) \rightarrow \lambda \cdot Z_{in}(k)}_{\forall k \in \{1, 2, 3, \ldots\}} \Rightarrow \begin{cases} i_s(\theta) \rightarrow i_s(\theta)/\lambda \\ v_s(\theta) \rightarrow v_s(\theta) \end{cases}$$



Switch Losses

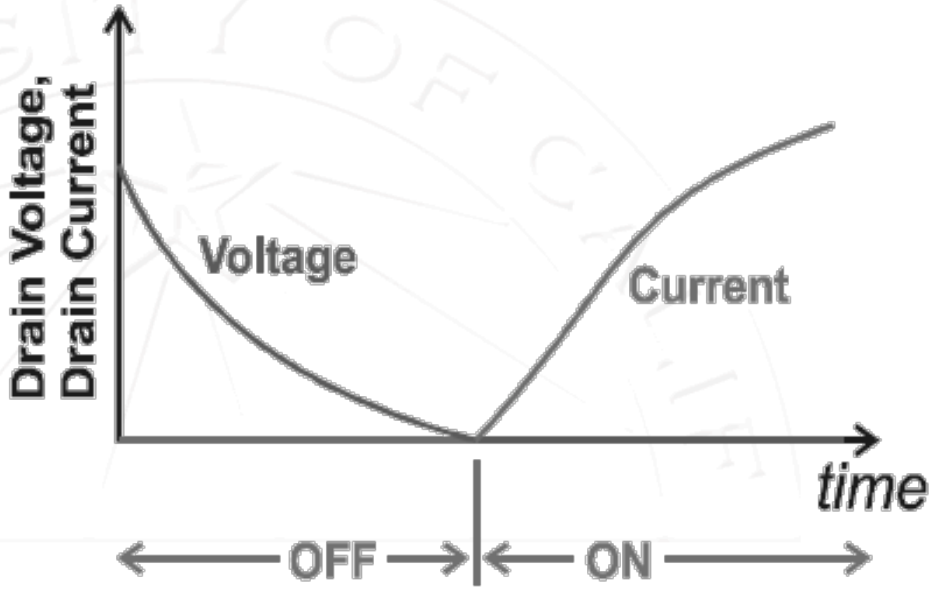




$$P_{sw} = \frac{1}{2} C_s V_{sw}^2 f_0$$

- When a switch is closed across a capacitor, an impulse of current flows through the switch to discharge the capacitor. The energy stored in the capacitor is dissipated into heat through the switch. (ideal switch?)
- If you make a smaller switch, the on-resistance goes down so you have to live with finite capacitance.

ZVS



- A ZVS network will return the voltage to zero at the moment of switch turn-on. To make the circuit more robust, the derivative of the voltage can also be forced to zero (or *n*-derivatives …) to obtain a maximally flat zero.

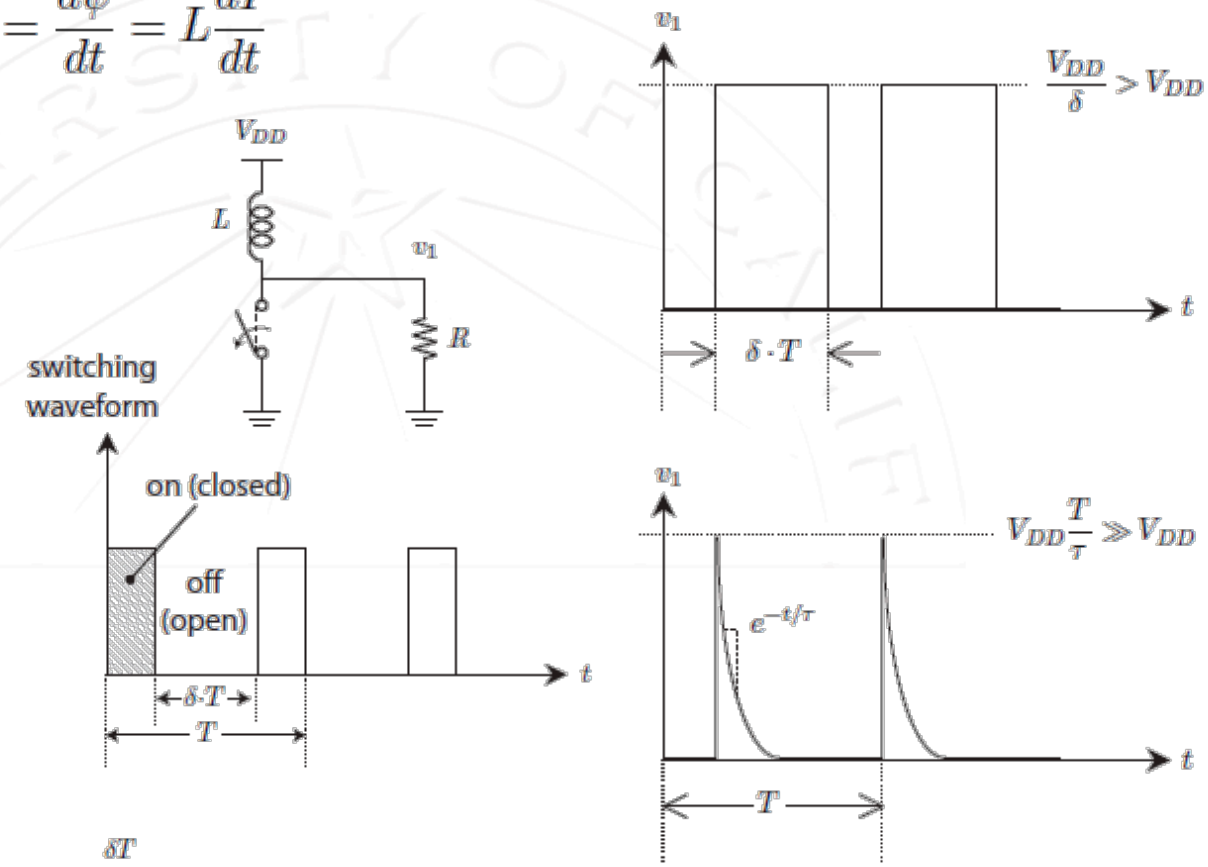
Switch Losses: ZCS Condition

- The dual of ZVS is ZCS.
- What happens if you open circuit an inductor with current (flux)? The energy stored in the magnetic flux is dissipated
- In practice the voltage "kick" produced by the inductor will break down the switch and conduct current.
- It's also possible to design a load network that returns the current to zero just before the switch opens.

$$P_{lost} = f \cdot E_m = \frac{1}{2} L I_M^2 f$$

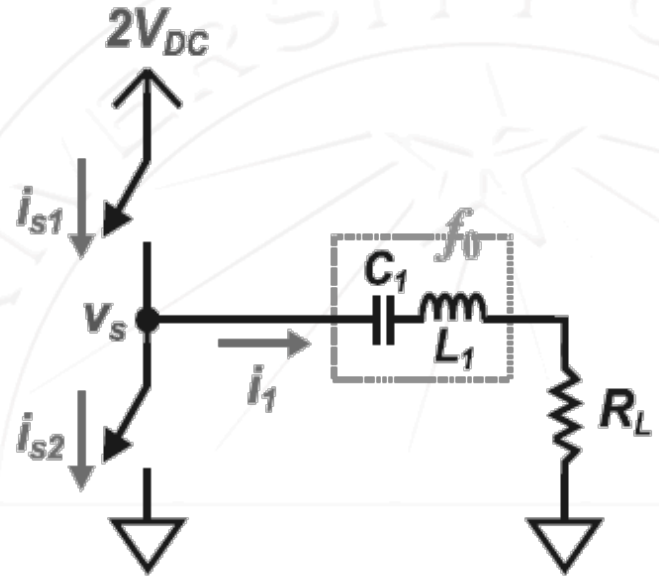
Switching Inductors

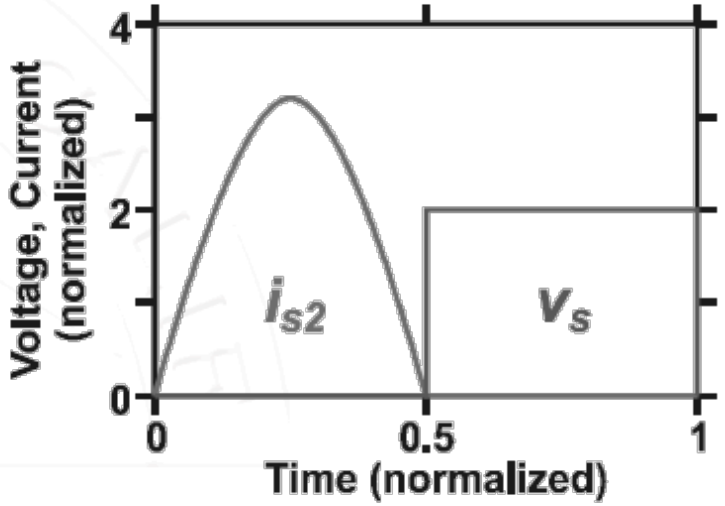
$$V_L(t) = \frac{d\psi}{dt} = L\frac{dI}{dt}$$



- If the inductor is large enough, it's switching behavior can be idealized.

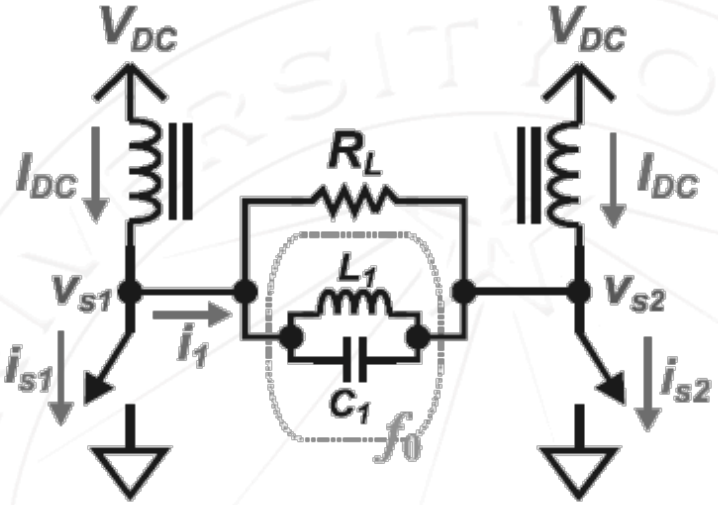
Class D

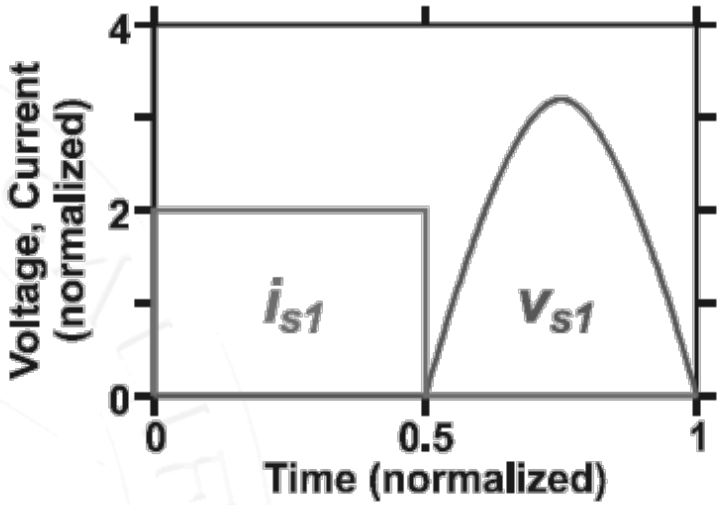




- Two switches used to realize square waveform.
- Series tank only allows fundamental current to flow into load.
- Switch capacitance limits efficiency in high frequency applications.

Class D^{-1}



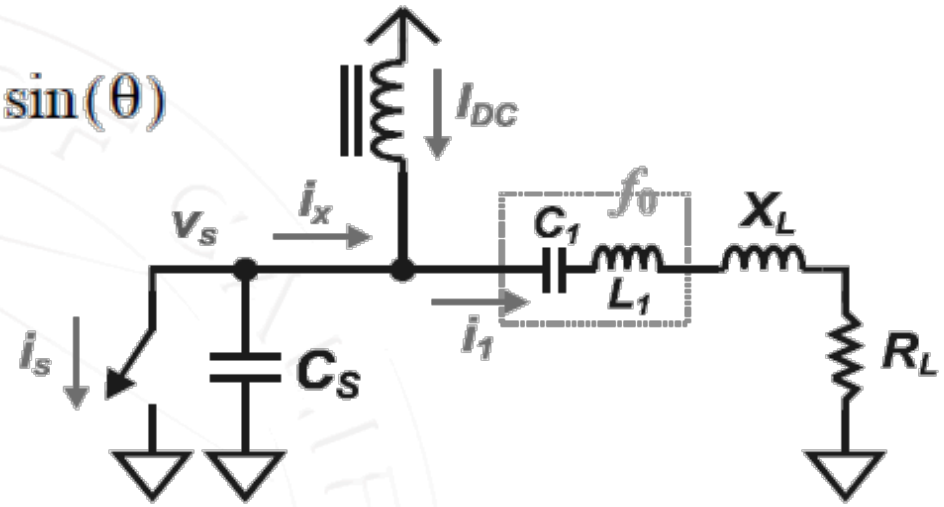


- The "Dual" Class D amplifier (interchange voltage/current → square wave current, sinusoidal voltage, parallel LCR filter)
- Chokes act like current sources. ZVS by "design" but only if there is no device capacitance to begin with.

$$v_{s1} = \begin{cases} 0 & 0 < \theta < \pi \\ -\frac{4}{\pi} I_{DC} R_L \sin(\theta) & \pi < \theta < 2\pi \end{cases}$$

Class E

$$i_x = -I_{DC} + \alpha\cos(\theta) + \beta\sin(\theta)$$



- Switch driven with 50% duty cycle. Device capacitance C_s absorbed into network.
- The current i_1 is sinusoidal and the current through the choke is DC. The sum of these currents flows through the switch + capacitor.

Class E Currents

$$i_s = \begin{cases} I_{DC} - \alpha\cos(\theta) - \beta\cos(\theta) & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases}$$

$$i_{cs} = \begin{cases} 0 & 0 < \theta < \pi \\ I_{DC} - \alpha\cos(\theta) - \beta\cos(\theta) & \pi < \theta < 2\pi \end{cases}$$

- When switch is closed, all the current flows through it. When open, this same current must flow through the capacitor. The voltage across the capacitor is given by the integral of the current since

$$\frac{dv_s}{dt} = \frac{1}{C_s} \cdot \begin{cases} 0 & 0 < \theta < \pi \\ I_{DC} - \alpha\cos(\theta) - \beta\cos(\theta) & \pi < \theta < 2\pi \end{cases}$$

Class E Voltages

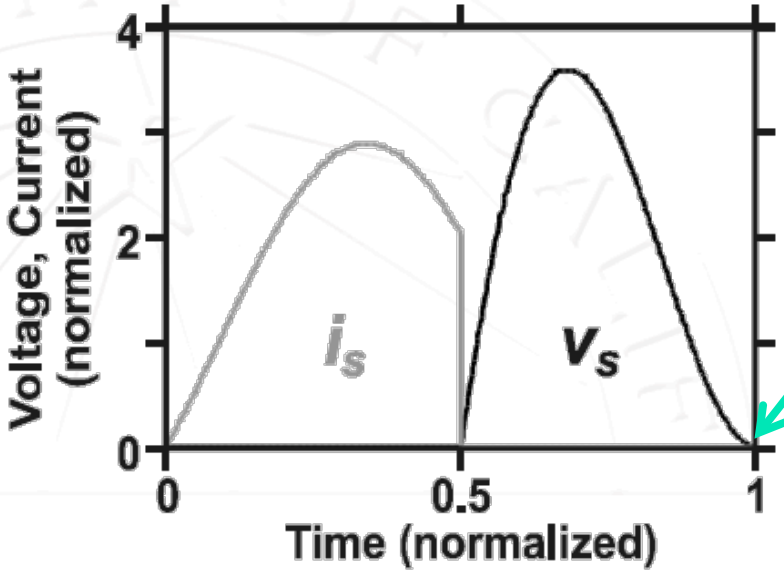
$$v_s = \frac{1}{2\pi f_0 C_s} \cdot \begin{cases} I_{DC} \cdot (\theta - \pi) - \alpha \sin(\theta) + \beta[\cos(\theta) + 1] & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases}$$

$$\alpha = I_{DC}$$

$$\beta = -\frac{\pi}{2} \cdot I_{DC}$$

- We can impose voltage continuity, so $\theta=\pi$. But we have two degrees of freedom, so we can also set the derivative of the voltage to zero (ZdVS). When both conditions are satisfied, we have a class E amplifier.

Class E Current/Voltage



ZVS & ZdVS

$$v_s = \frac{I_{DC}}{2\pi f_0 C_s} \cdot \begin{cases} 0 & 0 < \theta < \pi \\ \theta - \sin(\theta) - (\pi/2)\cos(\theta) - 3\pi/2 & \pi < \theta < 2\pi \end{cases}$$

$$i_s = \begin{cases} I_{DC} - \cos(\theta) + (\pi/2)\cos(\theta) & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases}$$

Class E Load & Swing

- The load is given from Fourier analysis of the current/ voltage.
- To realize a Class E amplifier requires an inductive load.
- One big disadvantage of the Class E amplifier is that the voltage swing across the device is very large (nearly $4\times V_{DD}$).

Switching Amplifier Efficiency

$$P_{SW} = \frac{1}{2} \cdot C_S V_{SW}^2 f_0 \qquad P_{SW} = \frac{1}{4\pi} \cdot \frac{V_{SW}^2}{Z_{CS}} \qquad Z_{CS} \equiv \frac{1}{2\pi f_0 C_S}$$

$$P_{diss} \approx I_{RMS}^2 R_{on} + \frac{1}{4\pi} \cdot \frac{V_{SW}^2}{X_{CS}} \qquad P_{DC} = V_{DC} I_{DC}$$

$$V_{DC} \equiv \frac{1}{2\pi} \cdot \int_0^{2\pi} v_s d\theta$$

$$\eta_D \equiv \frac{P_{out}}{P_{DC}} = 1 - \frac{P_{diss}}{P_{DC}}$$

$$I_{DC} \equiv \frac{1}{2\pi} \cdot \int_0^{2\pi} i_s d\theta$$

$$\eta_D \approx 1 - \left(\frac{I_{RMS}^2 R_{on}}{V_{DC} I_{DC}} + \frac{V_{SW}^2}{4\pi X_{CS} V_{DC} I_{DC}} \right)$$

$$G = \frac{P_{DC} - P_{diss}}{P_{in}} = \frac{V_{DC} I_{DC} - I_{RMS}^2 R_{on}}{P_{in}}$$

- For ZVS, P_{sw} is zero

Switching Amplifier PAE

$$PAE \approx \left(1 - \frac{P_{in}}{V_{DC}I_{DC} - I_{RMS}^2 R_{on}}\right) \cdot \left[1 - \left(\frac{I_{RMS}^2 R_{on}}{V_{DC}I_{DC}} + \frac{V_{SW}^2}{4\pi X_{CS} V_{DC} I_{DC}}\right)\right]$$

$$PAE \approx \left(1 - \frac{P_{in}}{V_{DC}I_{DC}}\right) \cdot \left[1 - \left(\frac{I_{RMS}^2 R_{on}}{V_{DC}I_{DC}} + \frac{V_{SW}^2}{4\pi X_{CS} V_{DC} I_{DC}}\right)\right]$$

$$PAE \approx \left(1 - \frac{P_{in}}{V_{DC}I_{DC}}\right) \cdot \left(1 - \frac{I_{RMS}^2 R_{on}}{V_{DC}I_{DC}}\right)$$

- This result includes the gain of the amplifier. To arrive at the final result, we assume 100% drain efficiency and ZVS. Note that P_{in} is a function of the transistor size.

Switch FOM

$$P_{out} = \frac{1}{2} v_1 i_1 \cos(\alpha_1 - \beta_1)$$

- It's useful to relate the effiency to peak current/voltage swings (stress) on the device. For a high efficiency PA we have

$$P_{out} \approx V_{DC} I_{DC}$$

$$P_{out} = (V_{pk} I_{pk}) \cdot \left(\frac{v_1 i_1 \cos(\alpha_1 - \beta_1)}{2 V_{pk} I_{pk}} \right) \qquad P_{out} \approx (V_{pk} I_{pk}) \cdot \left(\frac{V_{DC} I_{DC}}{V_{pk} I_{pk}} \right)$$

$$E_P \equiv \frac{P_{out}}{V_{pk} I_{pk}} = \left(\frac{v_1}{V_{pk}} \right) \cdot \left(\frac{i_1}{I_{pk}} \right) \cdot \left[\frac{1}{2} \cos(\alpha_1 - \beta_1) \right]$$

$$E_P \equiv \frac{P_{out}}{V_{pk} I_{pk}} \approx \left(\frac{V_{DC}}{V_{pk}} \right) \cdot \left(\frac{I_{DC}}{I_{pk}} \right)$$

FOM (cont)

$$F_V \equiv V_{pk}/V_{DC}$$

$$F_{PI} \equiv I_{pk}/I_{DC}$$

$$E_P \equiv \frac{P_{out}}{V_{pk} I_{pk}} \approx \frac{1}{F_V F_{PI}}$$

$$F_C \equiv \frac{P_{out}}{V_{DC}^2/Z_C}$$

- Peak voltage versus DC
- Peak current versus DC
- RMS current versus DC
- Output power versus peak stress on transsitor
- Output power versus stored reactive power.
  - The smaller this ratio, the more the design can tolerate output capacitance, and hence a larger transistor with lower conductive losses.

Device Size Limited Maximum Drain Efficiency

$$\eta_D \approx 1 - \frac{I_{RMS}^2 R_{on}}{V_{DC} I_{DC}}$$

$$\eta_D \approx 1 - \left[\left(\frac{I_{RMS}}{I_{DC}} \right)^2 \left(\frac{V_{pk}}{V_{DC}} \right)^2 \left(\frac{R_{on}}{V_{pk}^2} \right) (V_{DC} I_{DC}) \right]$$

$$\eta_D \approx 1 - \left[\left(\frac{I_{RMS}}{I_{DC}} \right)^2 \left(\frac{V_{pk}}{V_{DC}} \right)^2 \left(\frac{\bar{R}_{on}}{\bar{V}_{bk}^2} \right) (P_{out}) \right]$$

$$\eta_D \approx 1 - \left[(F_I^2 F_V^2) \frac{P_{out}}{(\bar{V}_{bk}^2 / \bar{R}_{on})} \right]$$

- All terms except the third are invariant and only depend on the tuning strategy.
- Minimize the third term by using the highest peak voltage possible (minimize current through device).

Capacitance Limited Drain Efficiency

$$\eta_D \approx 1 - \frac{I_{RMS}^2 R_{on}}{V_{DC} I_{DC}}$$

$$\eta_D \approx 1 - \left[\left(\frac{I_{RMS}}{I_{DC}} \right)^2 \left(\frac{V_{DC} I_{DC}}{2\pi f_0 C_s V_{DC}^2} \right) (R_{on} C_{out})(2\pi f_0) \left(\frac{C_S}{C_{out}} \right) \right]$$

- Increase device size until the switch output capacitance equals the total output capacitance
- All terms except the last are invariant (bias, impedance scaling) and only depend on the switching network. Note the third term depends on technology but is independent of transistor size. Voltage waveform properties do not come into play.
- To minimize the final term, maximize C_{out}. Final efficiency only depends on technology RC time constant:

$$\eta_D \approx 1 - \left[\left(\frac{I_{RMS}}{I_{DC}} \right)^2 \left(\frac{V_{DC} I_{DC}}{2\pi f_0 C_s V_{DC}^2} \right) (\bar{R}_{on} \bar{C}_{out})(2\pi f_0) \right]$$

Reactive Energy Term

- The second term needs further explanation: $\left(\frac{V_{DC}I_{DC}}{2\pi f_0 C_s V_{DC}^2}\right)$
- For a highly efficient amplifier, the numerator is equal to the output power, and the denominator has the switch capacitance admittance: $\left(\frac{P_{out}}{V_{DC}^2/Z_C}\right)$
- This is a ratio of the output power to the switch's stored reactive power. We wish to use a tuning strategy that maximizes the reactive energy of the switch and minimizes the RMS current through the switch. The voltage cannot be traded for current like the previous case.

$$\eta_D \approx 1 - \left[(F_I^2 F_C)\frac{2\pi(\bar{R}_{on}\bar{C}_{out})}{1/f_0}\right] \qquad F_C \equiv \frac{P_{out}}{V_{DC}^2/Z_C}$$

Gain Limited PAE

$$PAE \approx \left(1 - \frac{\bar{P}_{in}}{P_{out}} \cdot \lambda\right) \cdot \left(1 - \frac{I_{RMS}^2 \bar{R}_{on}}{V_{DC} I_{DC}} \cdot \frac{1}{\lambda}\right) \qquad \lambda = \sqrt{\frac{I_{RMS}^2 \bar{R}_{on} P_{out}}{V_{DC} I_{DC} \bar{P}_{in}}}$$

- For $C_s = C_{out}$, where λ is a scaling parameter. Clearly an optimal size exists since $R_{on} \sim \lambda$ whereas $P_{in} \sim 1/\lambda$.
- The optimal PAE is given by:

$$PAE \approx \left(1 - \sqrt{\frac{I_{RMS}^2 \bar{R}_{on} \bar{P}_{in}}{P_{out} V_{DC} I_{DC}}}\right)^2$$

$$PAE \approx \left[1 - \left(\frac{I_{RMS}}{I_{DC}}\right)\left(\frac{V_{pk}}{V_{DC}}\right)\left(\sqrt{\frac{\bar{P}_{in}}{V_{pk}^2 / \bar{R}_{on}}}\right)\right]^2$$

Under assumption of high drain efficiency

Gain Limited PAE (cont)

- Considering the breakdown limitations:

$$PAE \approx \left[1-(F_I F_V)\left(\sqrt{\frac{\bar{P}_{in}}{V_{bk}^2/\bar{R}_{on}}}\right)\right]^2$$

$$PAE \approx 1-(2F_I F_V)\left(\sqrt{\frac{\bar{P}_{in}}{V_{bk}^2/\bar{R}_{on}}}\right)$$

- Use a tuning network with low peak to DC current/voltage.
- Note that the final term is a scaling invariant property of transistor.

Capacitance Limited PAE

- If the optimal device is too large, it's output cap will be larger than C_s, and hence cannot be absorbed into the network. Must limit device size to C_s.

$$P_{in} = \frac{C_{out}}{\bar{C}_{out}} \cdot \bar{P}_{in} = \frac{C_s}{\bar{C}_{out}} \cdot \bar{P}_{in} \qquad F_C \equiv \frac{P_{out}}{V_{DC}^2 / Z_C}$$

$$PAE \approx \left(1 - \frac{C_s \bar{P}_{in}}{\bar{C}_{out} P_{out}}\right) \cdot \left[1 - (F_I^2 F_C)\left(\frac{2\pi \bar{R}_{on} \bar{C}_{out}}{1/f_0}\right)\right]$$

$$PAE \approx \left[1 - \left(\frac{\bar{P}_{in}}{\bar{C}_{out} V_{pk}^2}\right)\left(\frac{2\pi C_s V_{DC}^2}{P_{out}}\right)\left(\frac{V_{pk}}{V_{DC}}\right)^2\left(\frac{1}{2\pi f_0}\right)\right] \cdot \left[1 - (F_I^2 F_C)\left(\frac{2\pi \bar{R}_{on} \bar{C}_{out}}{1/f_0}\right)\right]$$

Cap Limited PAE

$$PAE \approx \left[1-\left(\frac{\bar{P}_{in}}{\bar{C}_{out}V_{pk}^2}\right)\left(\frac{F_V^2}{F_C}\right)\left(\frac{1}{2\pi f_0}\right)\right]\cdot\left[1-(F_I^2F_C)\left(\frac{2\pi\bar{R}_{on}\bar{C}_{out}}{1/f_0}\right)\right]$$

$$PAE \approx \left[1-\left(\frac{\bar{P}_{in}}{\bar{C}_{out}V_{bk}^2}\right)\left(\frac{F_V^2}{F_C}\right)\left(\frac{1}{2\pi f_0}\right)\right]\cdot\left[1-(F_I^2F_C)\left(\frac{2\pi\bar{R}_{on}\bar{C}_{out}}{1/f_0}\right)\right]$$

- Make the peak voltage as large as possible and increase the gain.

$$G = \left(\frac{\bar{C}_{out}V_{bk}^2}{\bar{P}_{in}}\right)\left(\frac{F_C}{F_V^2}\right)(2\pi f_0)$$

Summary

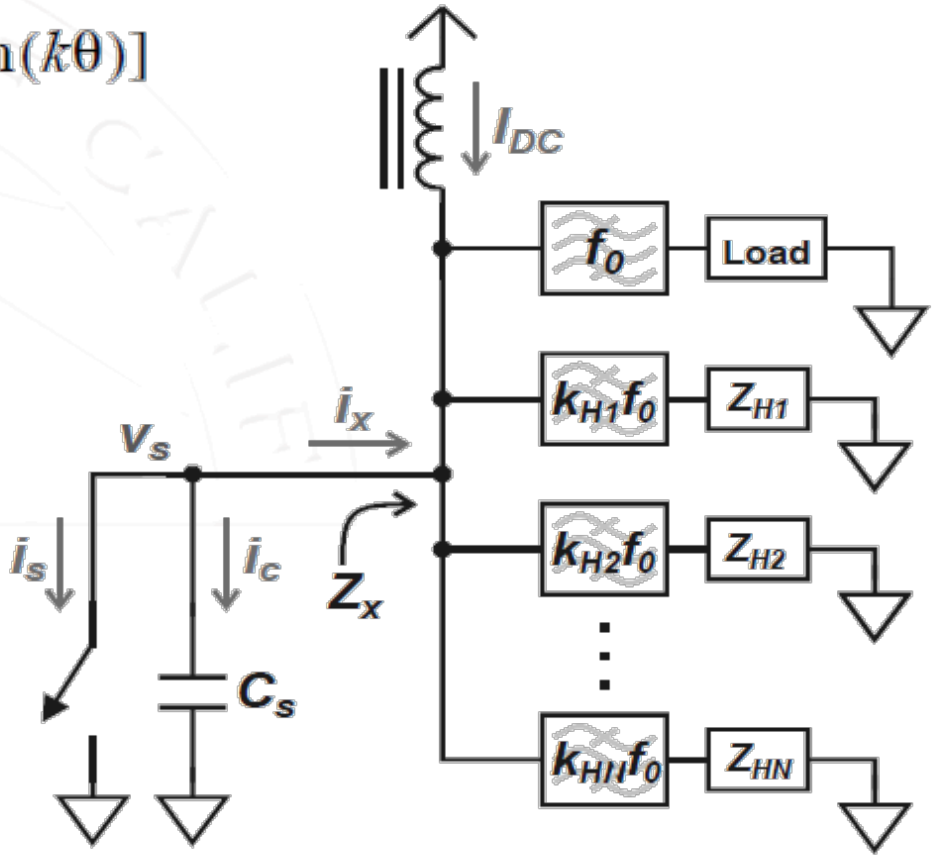
Design Constraint	Drain Loss WF Factor (W_D)	Gain WF Factor (W_G)	Drain Loss Device Factor (D_D)	Gain Device Factor (D_G)
device size limited η_D	$F_I^2 F_V^2$	N/A	$\frac{P_{out}}{(\bar{V}_{bk}^2/\bar{R}_{on})}$	N/A
capacitance limited	$F_I^2 F_C$	$F_V^{\,2}/F_C$	$\frac{2\pi \bar{R}_{on}\bar{C}_{out}}{1/f_0}$	$\frac{\bar{P}_{in}}{2\pi f_0 \bar{C}_{out} V_{bk}^2}$
gain limited PAE	$2F_I F_V$	$2F_I F_V$	$\sqrt{\frac{\bar{P}_{in}}{V_{bk}^2/\bar{R}_{on}}}$	$\sqrt{\frac{\bar{P}_{in}}{V_{bk}^2/\bar{R}_{on}}}$

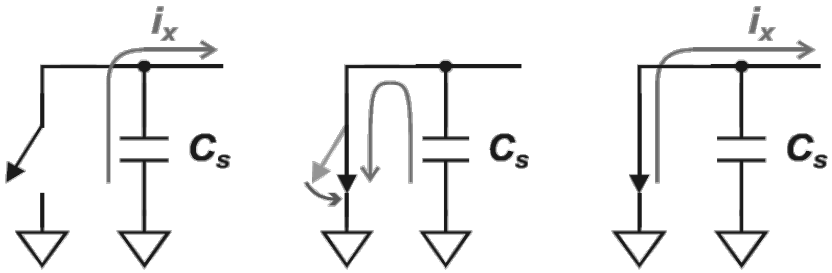
F_V	F_I	F_C	F_{PI}
V_{pk}/V_{DC}	I_{RMS}/I_{DC}	$\frac{P_{out}}{V_{DC}^2/Z_C}$	I_{pk}/I_{DC}

General Class E/F Design

$$i_x = a_0 + \sum_{k \in T} [a_k \cos(k\theta) + b_k \sin(k\theta)]$$

- A switch with parallel capacitance, an ideal choke, and a possibly countable infinite number of harmonic impedances.





Switch/Cap Current

- The switch carries an impulsive current component due to cap discharge.

$$i_s = -s(\theta)\cdot i_x(\theta) + Q\cdot\delta(\theta)$$

$$I_s(k) = \frac{1}{2\pi}Q - S_k \otimes I_x(k)$$

$$= \frac{1}{2\pi}Q - \sum_{|l|\in\{0,T\}} S_{k-l} I_x(l)$$

$$s(\theta) = \begin{cases} 1 & 0<\theta<2\pi D \\ 0 & 2\pi D<\theta<2\pi \end{cases}$$

$$i_{cs} = -\bar{s}(\theta)\cdot i_x(\theta) - Q\cdot\delta(\theta)$$

$$I_{cs}(k) = -\frac{1}{2\pi}Q - \bar{S}_k \otimes I_x(k)$$

$$= -\frac{1}{2\pi}Q - \sum_{|l|\in\{0,T\}} \bar{S}_{k-l} I_x(l)$$

$$S(\theta) = \begin{cases} D & k=0 \\ \dfrac{\sin(2\pi Dk)}{2\pi k} - j\dfrac{\sin^2(\pi Dk)}{\pi k} & k\neq 0 \end{cases}$$

Cap Voltage

- The voltage across the capacitor is calculated from the current.
- The harmonic impedance constraint implies the following relations.

$$v_s(\theta) = \begin{cases} 0 & 0 < \theta < 2\pi D \\ Z_{cs} \int_{2\pi D}^{\theta} i_{cs}(\theta) d\theta & 2\pi D < \theta < 2\pi \end{cases}$$

$$V_s(k) = -j\frac{Z_{cs}}{k} I_{cs}(k)$$

$$Z_{cs} = 1/(2\pi f_0 C_s)$$

$$I_{cs}(0) = 0$$

$$\underbrace{Z_k I_x(k) = V_s(k)}_{\forall k \in T}$$

$$\underbrace{jk\frac{Z_k}{Z_{cs}} I_x(k) - I_{cs}(k) = 0}_{\forall k \in T}$$

Constraint Equations

- There are |T| complex valued equations and one real valued equation and |T|+2 unknowns.
- These equations can be solved for Q and i_x
- The ZVS solution has an additional constraint Q=0.

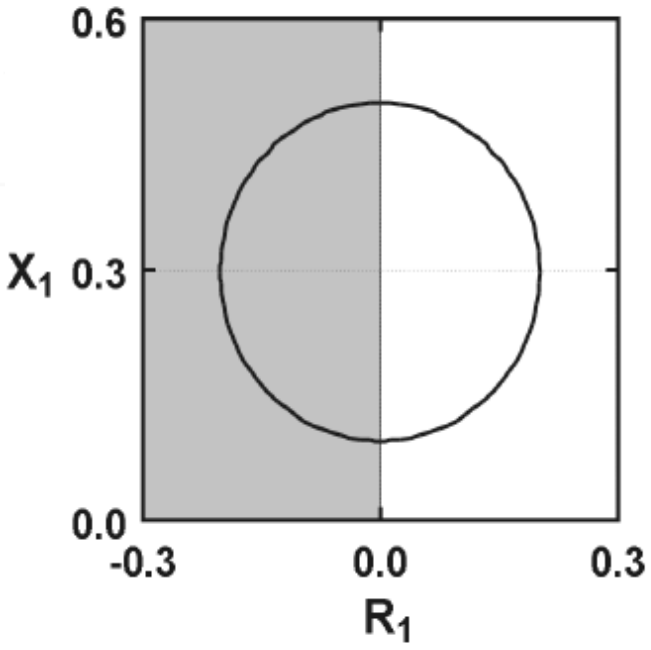
$$\underbrace{jk\frac{Z_k}{Z_{cs}}I_x(k) - I_{cs}(k) = 0}_{\forall k \in \{0, T\}}$$

$$\underbrace{jk\frac{Z_k}{Z_{cs}}I_x(k) + [\bar{S}_l \otimes I_x(l)]\Big|_{l=k} + \frac{1}{2\pi}Q = 0}_{\forall k \in \{0, T\}}$$

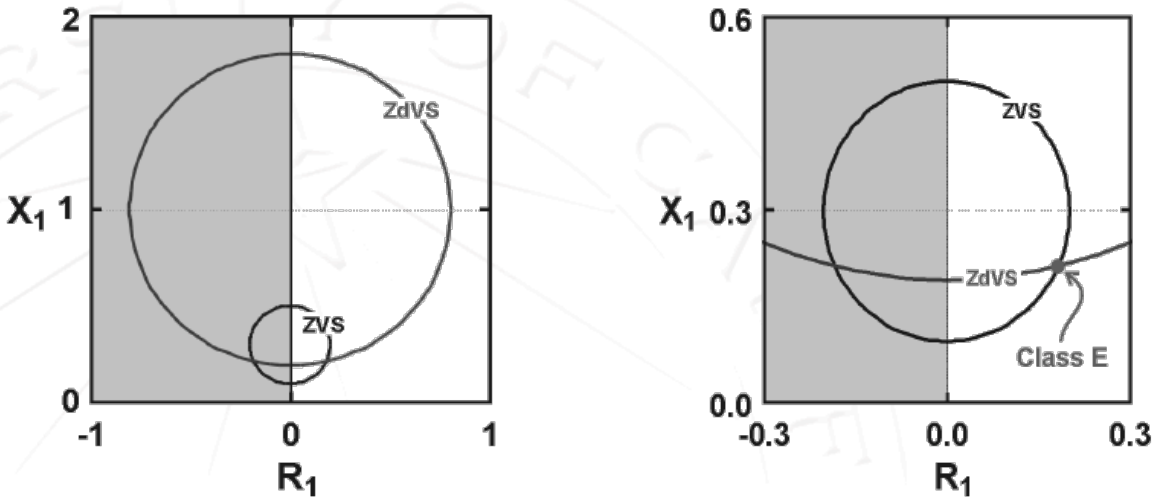
ZVS

- It can be shown that ZVS implies that:
- (R_1,X_1) is the fundamental load impedance.
- The center and radius of the circle is determined by the overtone network.

$$(X_1 - C_X)^2 + (R_1 - C_R)^2 - C_Z^2 = 0$$



ZdVS



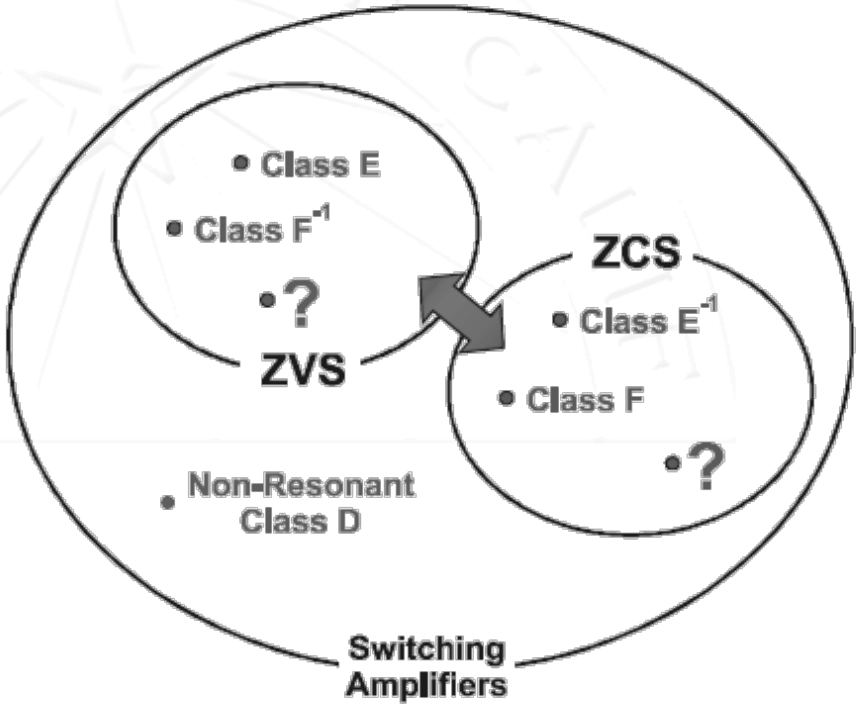
- The ZdVS conditions generate additional constraints.

$$\left.\frac{dV_s}{d\theta}\right|_{\theta=0} = Z_{cs} \sum_{k \in \{0.\,T\}} a_k$$

$$\frac{dV_s}{d\theta} = Z_{cs} i_{cs}$$

$$\sum_{k \in \{0.\,T\}} a_k = 0$$

Class E/F Amplifier Family

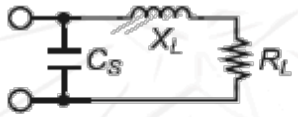
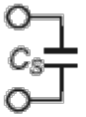
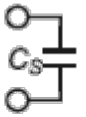
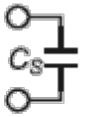
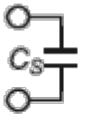
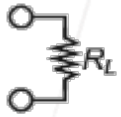


- Are there other interesting tuning networks besides the well known Class E and F?

Switching Amplifier Wish List

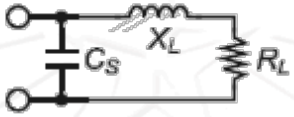
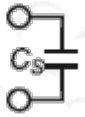
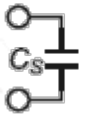
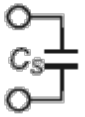
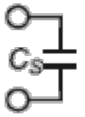
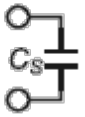
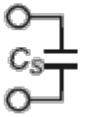
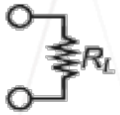
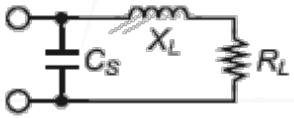
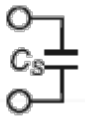
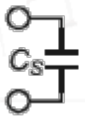
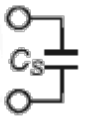
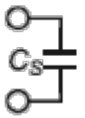
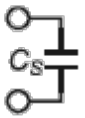
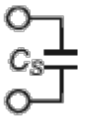
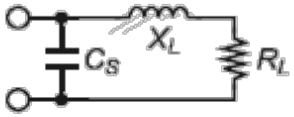
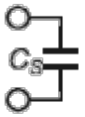
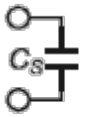
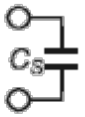
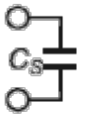
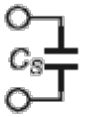
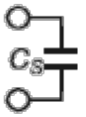
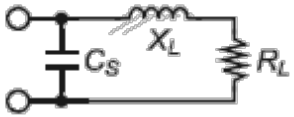
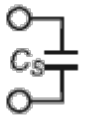
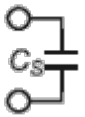
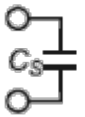
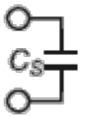
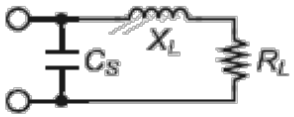
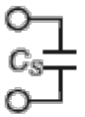
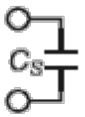
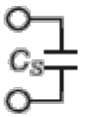
- ZVS Switching
- Inclusion of device output capacitance
- Simple circuit implementation
- Lower peak voltage (F_v)
- Lower RMS current (F_i)
- Capacitance Tolerance (F_c)

Class E versus F

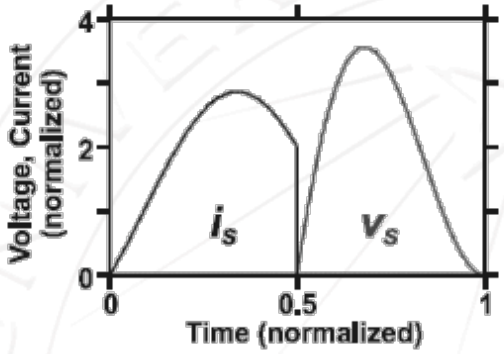
Tuning	f_0	$2f_0$	$3f_0$	$4f_0$	$5f_0$	$6f_0$	$7f_0$	$8f_0$
Class E								
Class F^{-1}		open	short	open	short	open	short	open

- Consider a hybrid of Class E and F with desirable properties of both. Construct such a hybrid by choosing harmonics to either satisfy Class E or F conditions. Note that the fundamental load is set by Class E ZVS conditions.

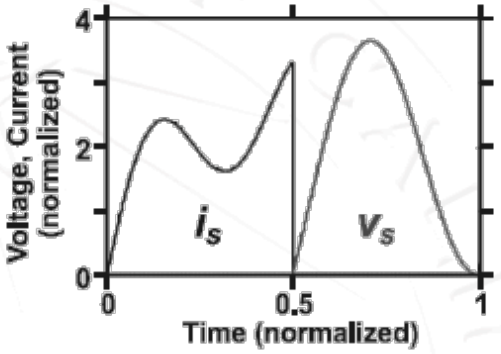
Class E/F Family

Tuning	f_0	$2f_0$	$3f_0$	$4f_0$	$5f_0$	$6f_0$	$7f_0$	$8f_0$
Class E								
Class F^{-1}		open	short	open	short	open	short	open
Class E/F_2		open						
Class E/F_3			short					
Class $E/F_{2,4,7}$		open		open			short	
Class $E/F_{2,3,4,5}$		open	short	open	short			

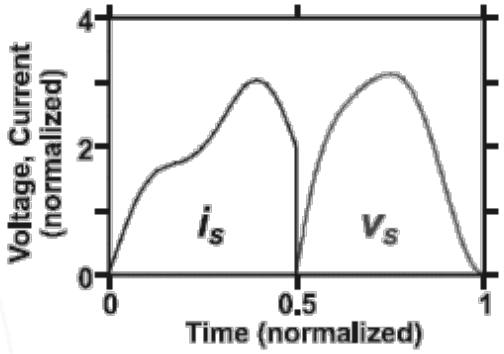
Example Class E/F Waveforms



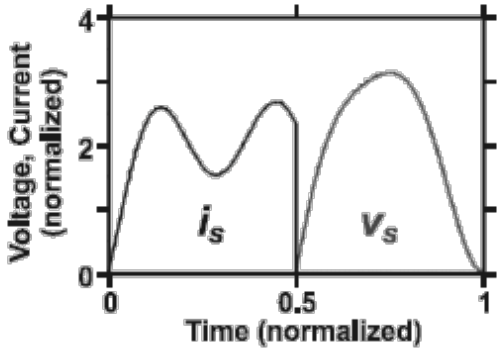
Class E



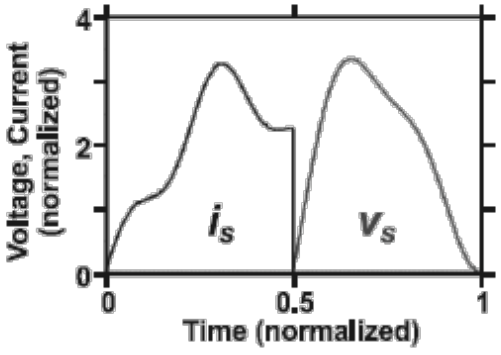
Class E/F_2



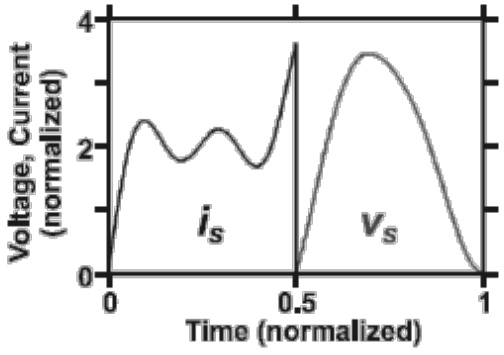
Class E/F_3



Class $E/F_{2,3}$

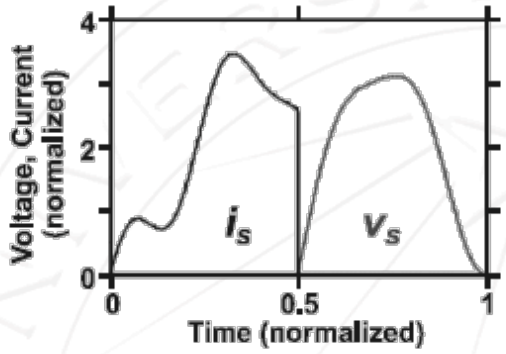


Class E/F_4

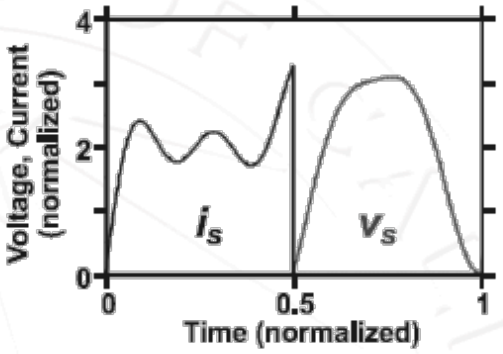


Class $E/F_{2,4}$

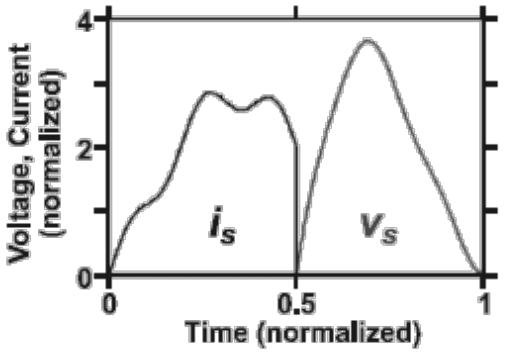
More Waveforms



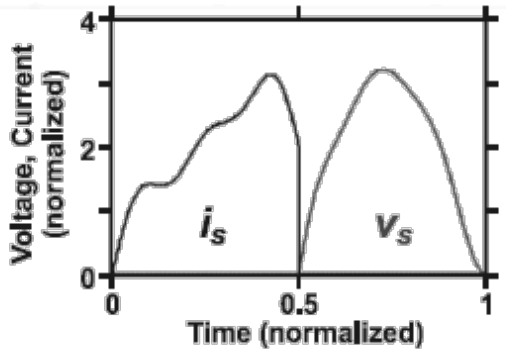
Class $E/F_{3,4}$



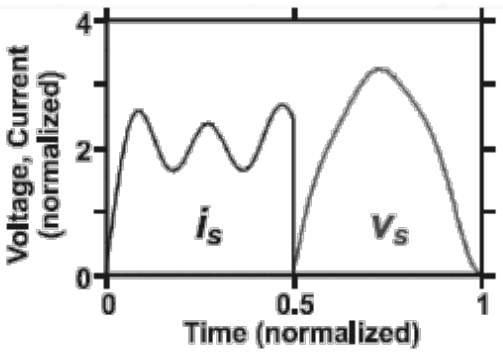
Class $E/F_{2,3,4}$



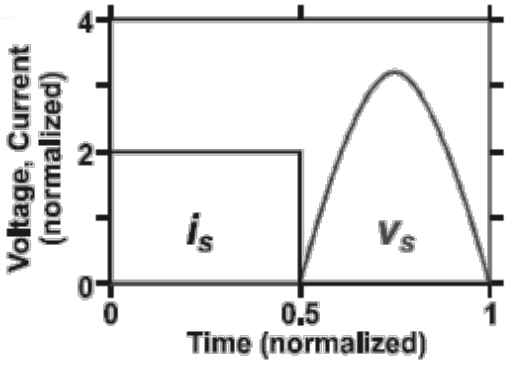
Class E/F_5



Class $E/F_{3,5}$

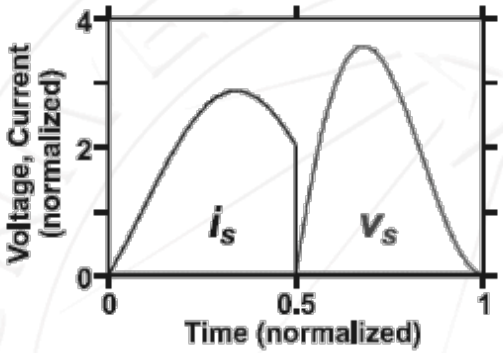


Class $E/F_{2,3,4,5}$

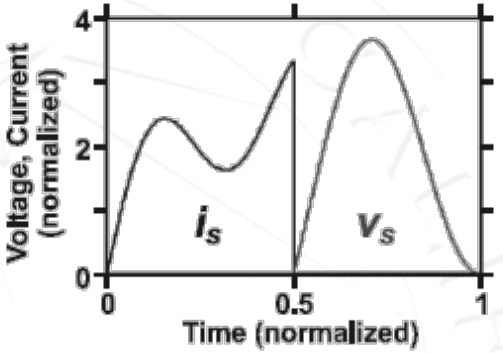


Class F^{-1}

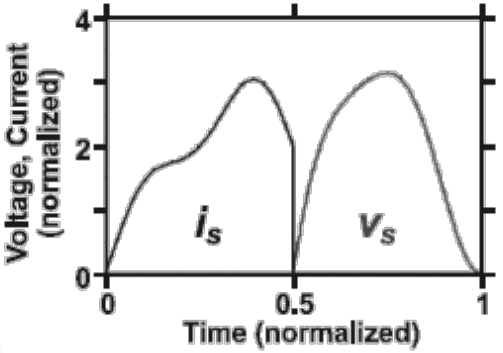
Single Harmonic Class E/F



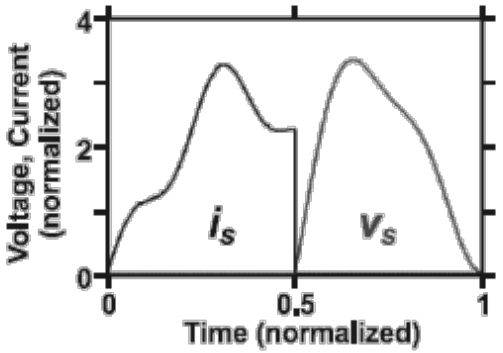
Class E



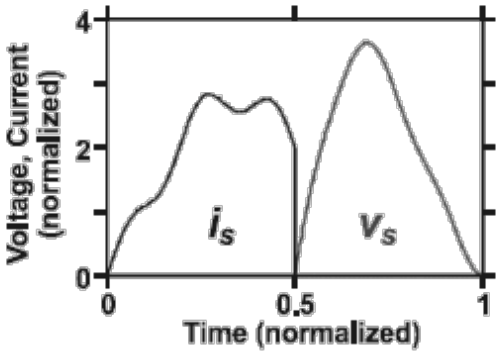
Class E/F_2



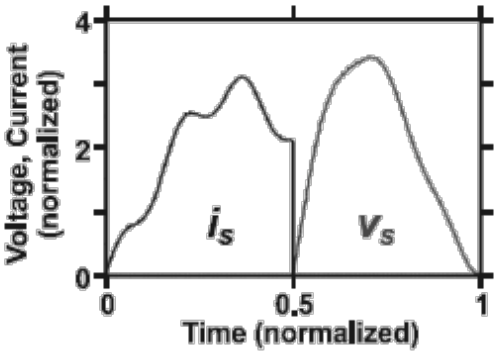
Class E/F_3



Class E/F_4

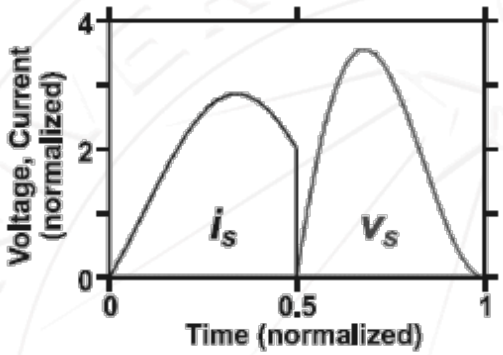


Class E/F_5

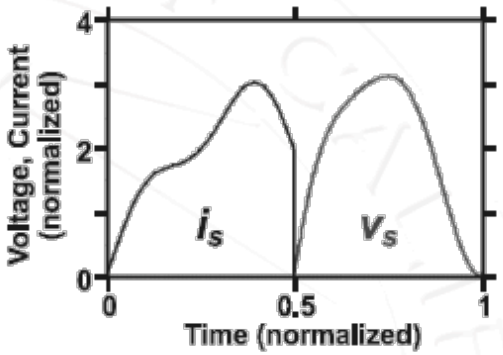


Class E/F_6

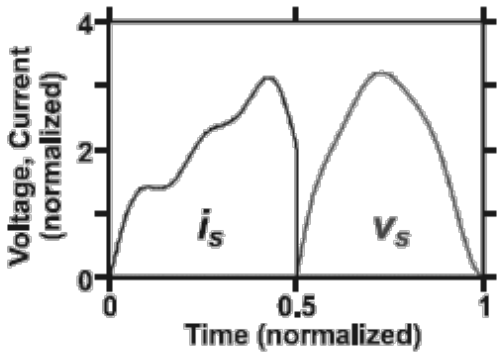
Odd Harmonic Class E/F



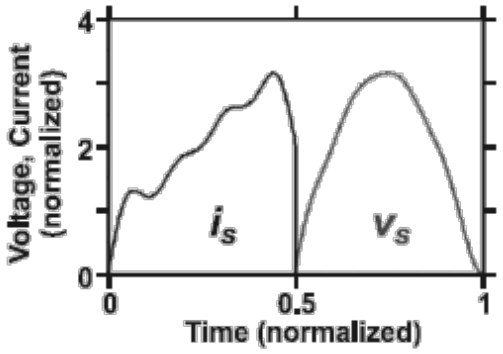
Class E



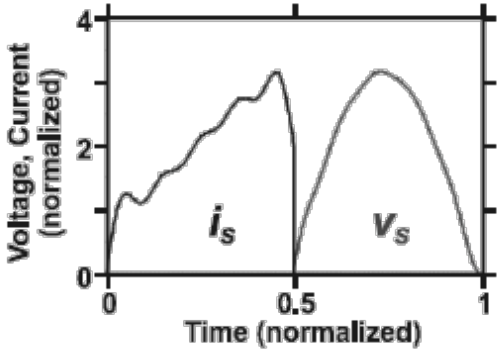
Class E/F_3



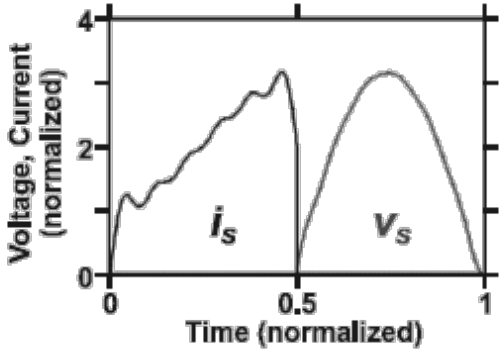
Class $E/F_{3,5}$



Class $E/F_{3,5,7}$

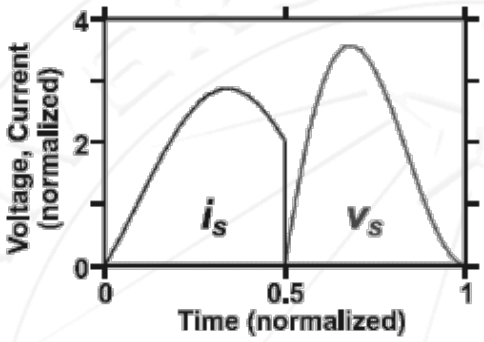


Class $E/F_{3,5,7,9}$

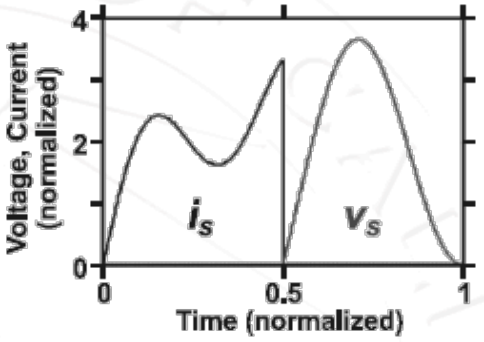


$E/F_{3,5,7,9,11}$

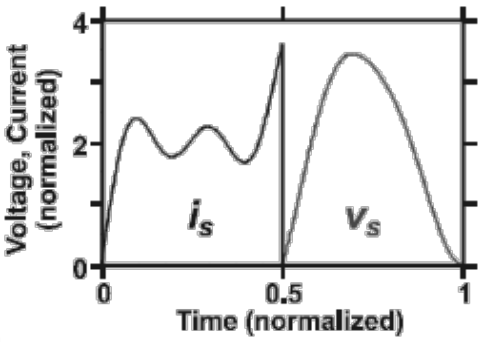
Even Harmonic Class E/F



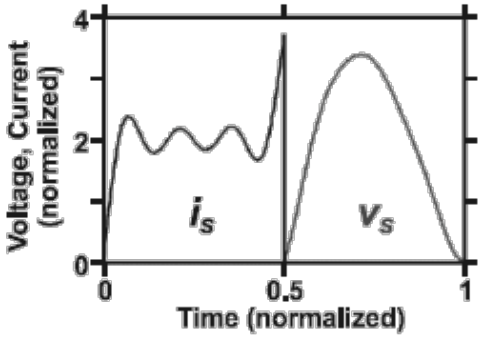
Class E



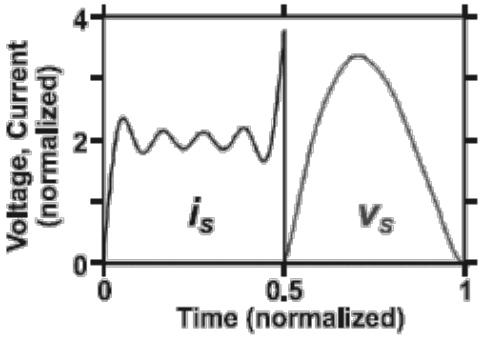
Class E/F_2



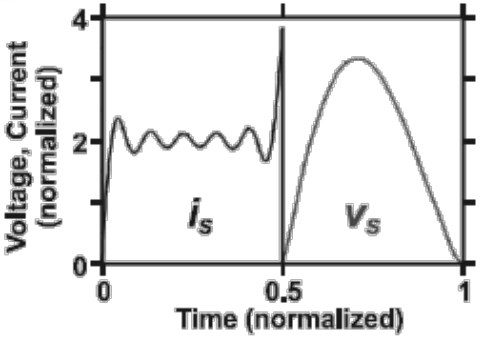
Class $E/F_{2,4}$



Class $E/F_{2,4,6}$

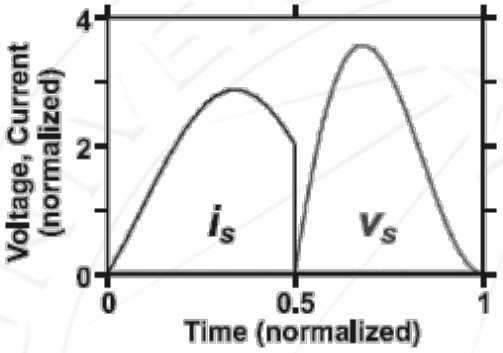


Class $E/F_{2,4,6,8}$

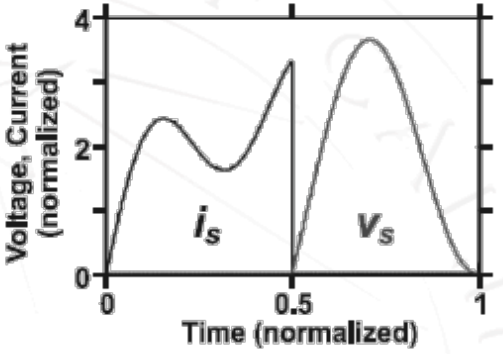


Class $E/F_{2,4,6,8,10}$

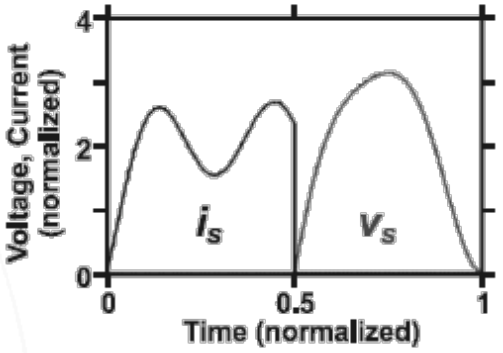
N-Harmonic Class E/F



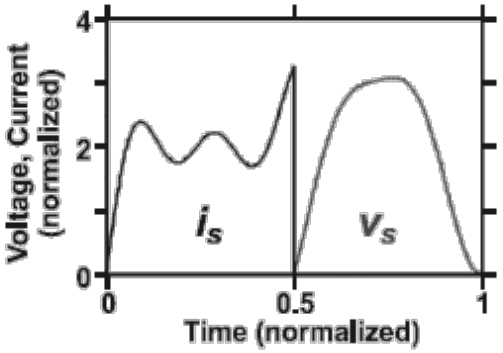
Class E



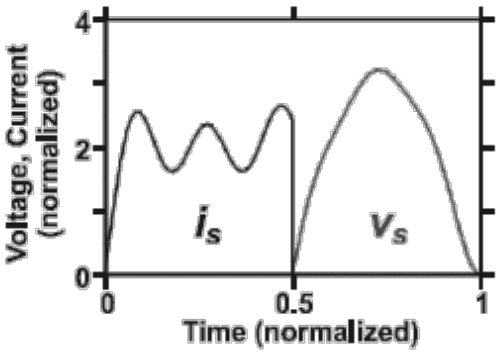
Class E/F_2



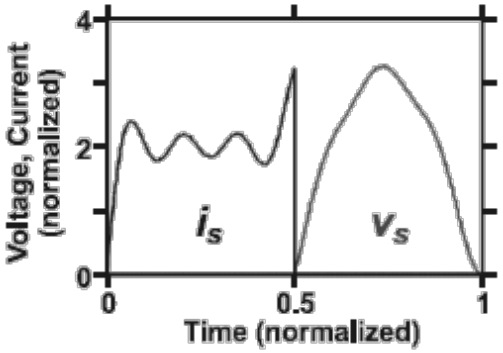
Class $E/F_{2,3}$



Class $E/F_{2,3,4}$



Class $E/F_{2,3,4,5}$

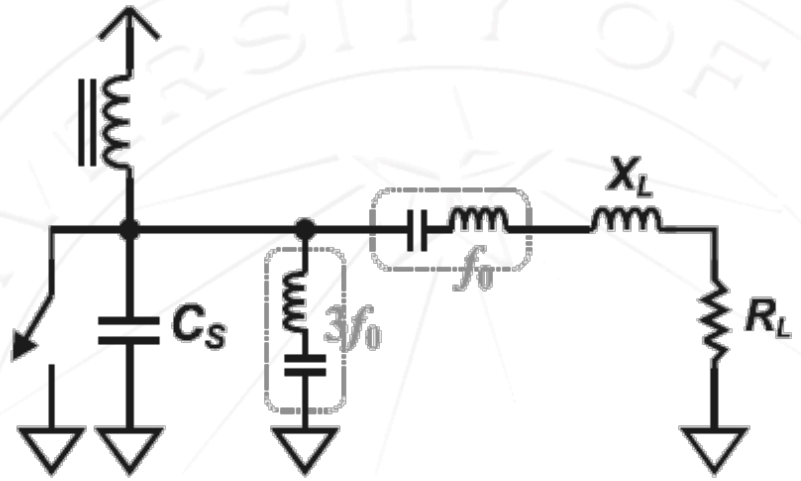


Class $E/F_{2,3,4,5,6}$

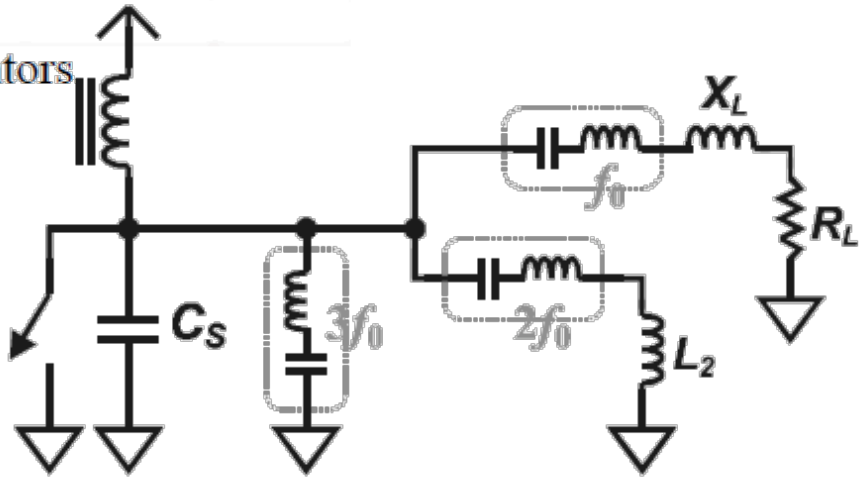
Overall Comparison

	Waveform Merit				Performance Merit (normalized to unity for Class E)				
Tuning	F_V	F_I	F_C	F_{PI}	$F_V^2F_I^2$	$F_I^2F_C$	F_V^2/F_C	$2F_VF_I$	F_VF_{PI}
E	3.56	1.54	3.14	2.86	1.00	1.00	1.00	1.00	1.00
E/F_2	3.67	1.48	**1.13**	3.33	0.98	**0.33**	2.94	0.99	1.20
E/F_3	**3.14**	1.52	3.14	3.06	**0.76**	0.97	**0.78**	0.87	0.94
$E/F_{2,3}$	**3.13**	1.47	2.31	2.67	**0.71**	**0.67**	1.05	**0.84**	**0.82**
E/F_4	3.34	1.55	2.45	3.27	0.89	0.79	1.13	0.94	1.07
$E/F_{2,4}$	3.43	1.46	**0.97**	3.60	0.84	**0.28**	3.00	0.91	1.21
$E/F_{3,4}$	**3.10**	1.62	1.93	3.45	0.84	0.68	1.23	0.91	1.05
$E/F_{2,3,4}$	**3.08**	1.45	**1.18**	3.26	**0.67**	**0.34**	1.99	**0.82**	0.99
E/F_5	3.65	1.53	3.14	2.84	1.04	0.99	1.05	1.02	1.02
$E/F_{3,5}$	3.20	1.51	3.14	3.12	0.78	0.97	**0.78**	0.87	0.94
$E/F_{2,3,4,5}$	3.20	1.45	2.11	2.65	**0.72**	0.60	1.20	**0.85**	**0.83**
F^{-1}	3.14	1.41	N/A	2.00	0.66	N/A	N/A	0.81	0.62

Direct Implementation

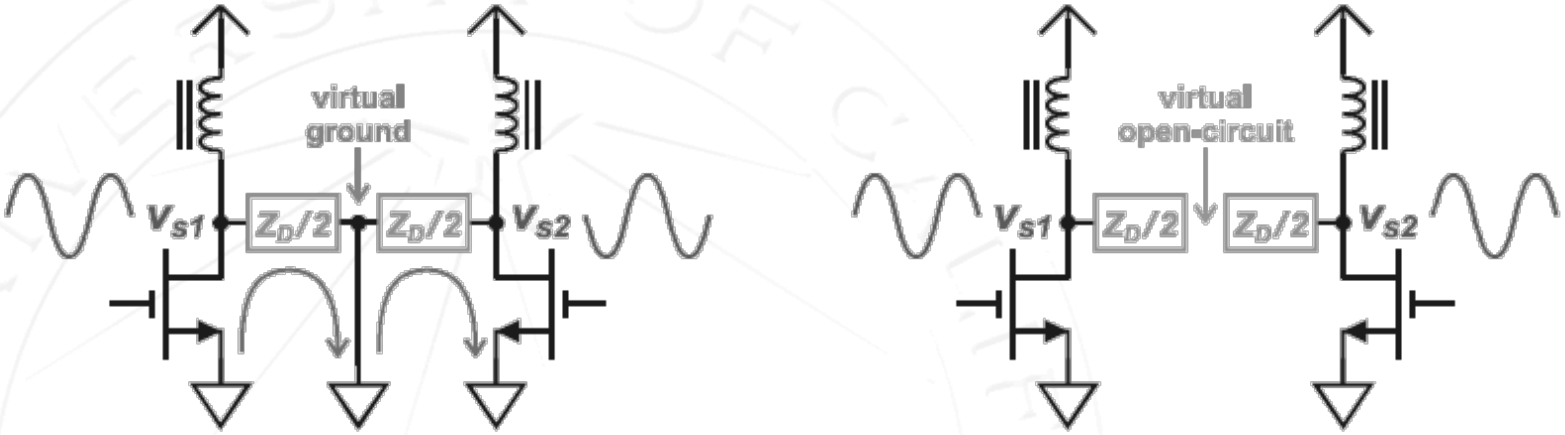


Direct E/F_3 implementation using high-Q resonators



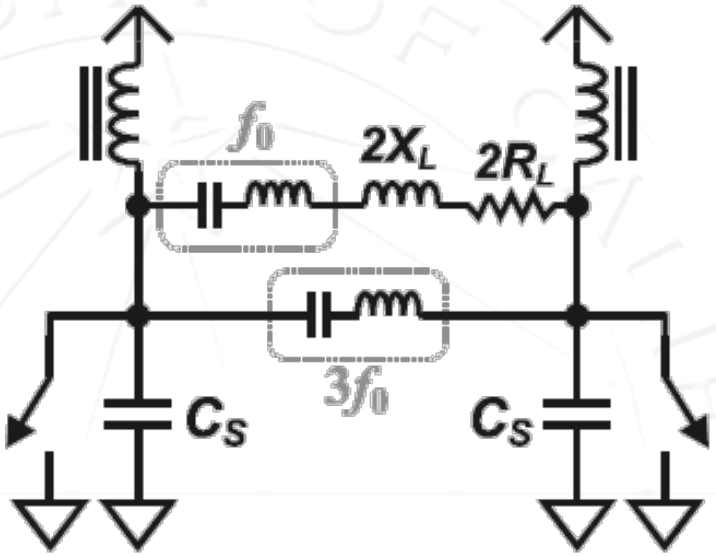
Direct $E/F_{2,3}$ implementation using high-Q resonators.

Push-Pull Amplifiers



- Creation of virtual grounds at odd harmonics and open circuits at even harmonics is very handy for designing class E/F amplifiers.

Class E/F_3 Push-Pull

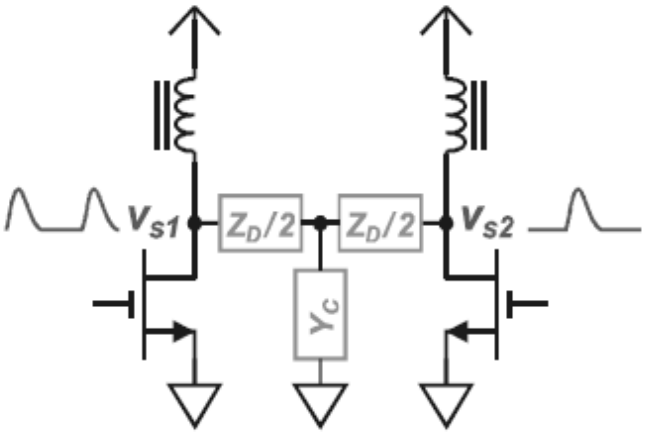


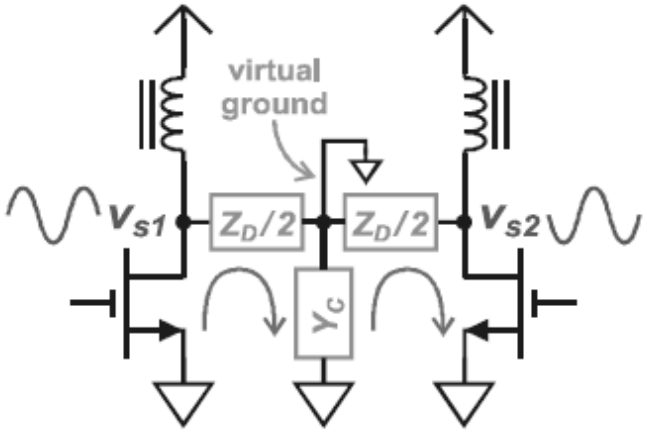
Class E/F_3 push/pull implementation allowing the use of low-Q resonators.

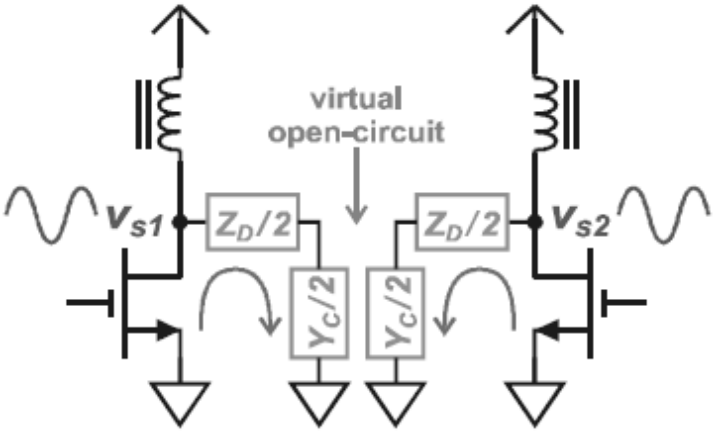
- Short at third harmonic. Does not need to be high Q since even harmonics don't "see it"

Even & Odd Harmonic Control

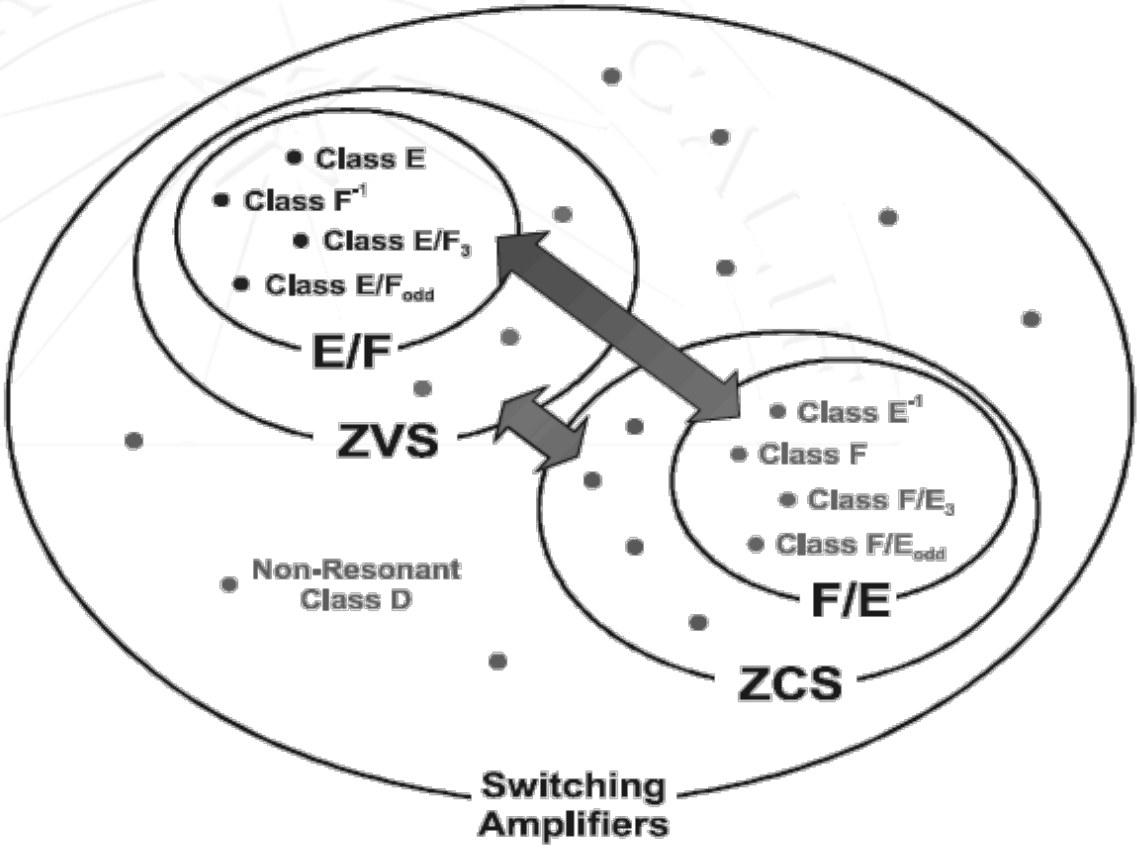
- Odd harmonics only see $Z_D/2$ since Y_C is shorted to ground.
- Even harmonics see Y_c to ground





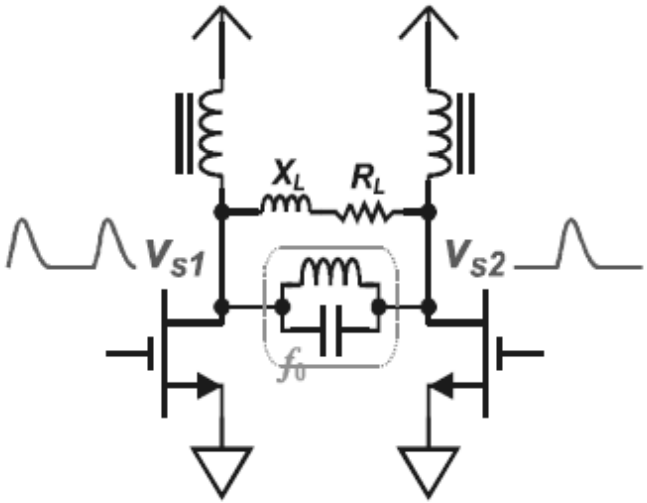


Switching Amplifier Landscape



Class E/F_{odd} Amplifier

- All odd harmonics see small impedance (ideally short) whereas even harmonics do not see shunt LC tank.



$$Y_1 = \frac{I_1}{V_1} = \frac{4I_{DC}}{\pi^2 V_{DC}} - j \cdot \frac{1}{Z_C}$$

$$= \frac{1}{R_L} - j \cdot \frac{1}{Z_C}$$

$$R_L \equiv \frac{\pi^2}{4} \cdot \frac{V_{DC}}{I_{DC}}$$