EECS 242:
The ABC's of Power Amplifiers

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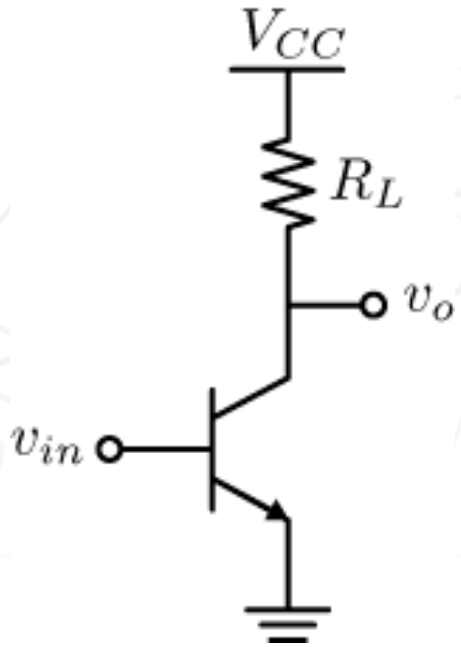
Class A Amplifiers

- Class A amplifiers have a collector current waveform with 100% duty cycle. In other words, the bias current $I_Q > i_{sw}$, where i_{sw} is the current swing.
- The advantage of Class A amplifiers is high linearity, clean sinusoidal waveforms (little harmonic filtering needed), and simple design (not relying too much on transistor non-linearity).
- The disadvantage of Class A is low efficiency and maximum power consumption at zero output power!
- Dynamic Class A (modulate bias current) is an attractive solution for some applications. Envelope following Class A combined with dynamic Class A is even better.

CE/CS Class A

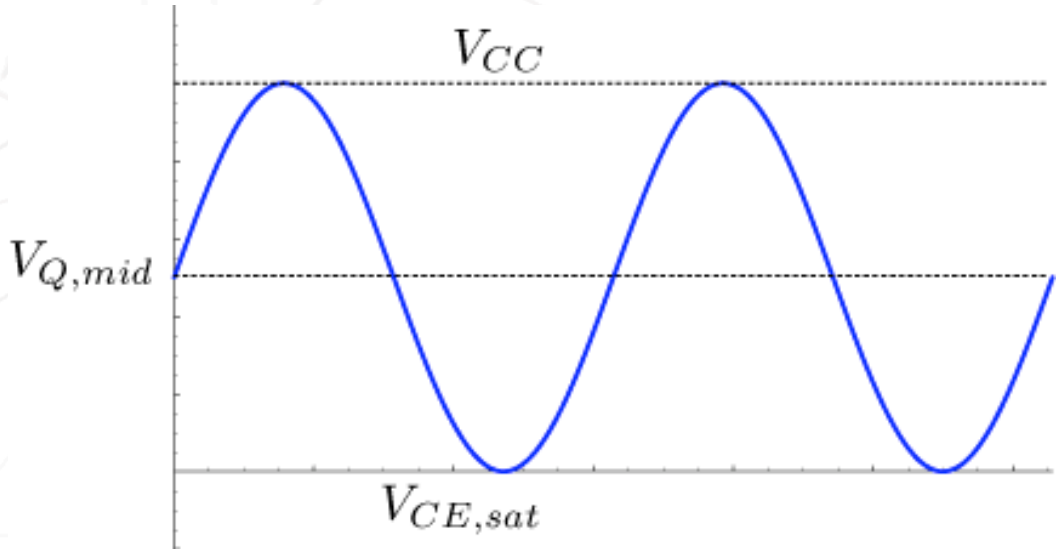


- The CE amplifier has the advantage of higher power gain (there is voltage gain and current gain).
- The collector effciency is given by

$$\eta_c = \frac{P_L}{P_{dc}} = \frac{\frac{1}{2} v_o i_o}{V_{CC} I_Q} = \frac{1}{2} \overline{v} \times \overline{i}$$

- The efficiency is maximized if we can set the voltage swing and current swing independently.

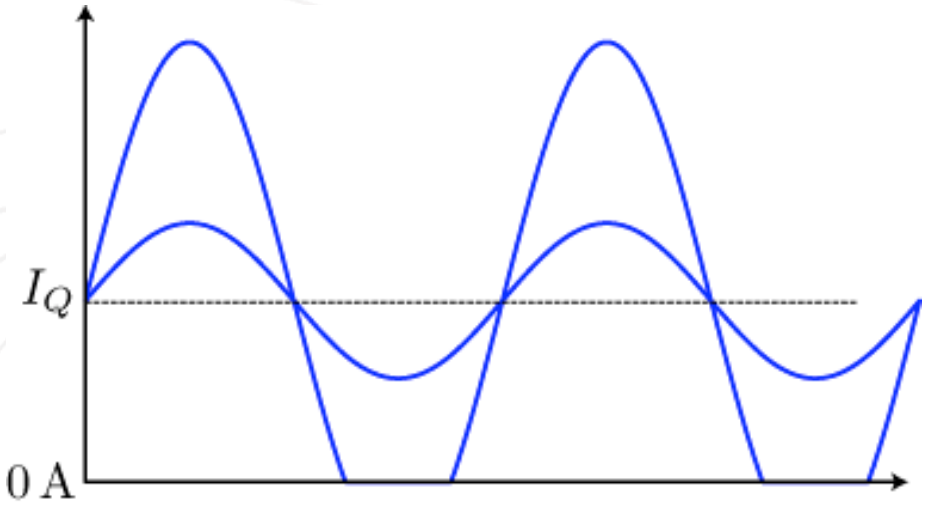
CE/CS Voltage Swing



- We see that to avoid clipping, we should bias the transistor at the midpoint between V_{CC} and V_{CEsat}.
- Thus

$$v_o \leq \frac{V_{CC}}{2}$$

CE/CS Current Swing



- The current in the transistor cannot go negative. Therefore, the maximum current is set by the bias current

$$i_o \leq I_Q$$

- The efficiency is therefore limited to 25%

$$\eta \leq \frac{1}{2} \times \frac{1}{2} = \frac{1}{4}$$

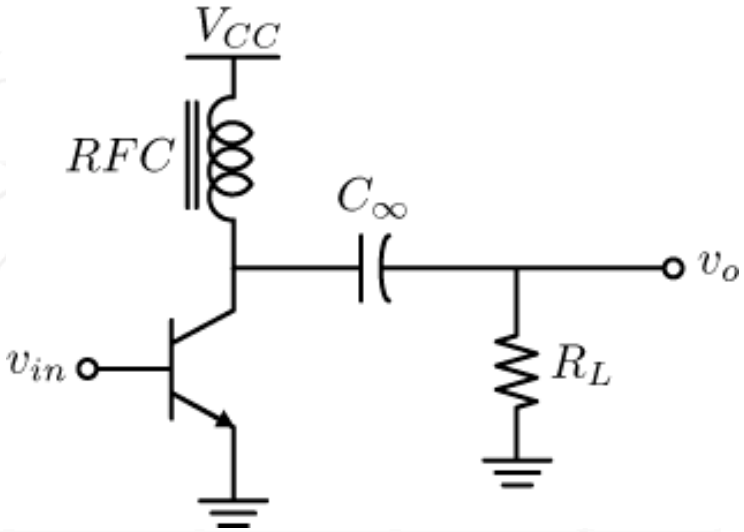
Optimum Load

- It's important to note that to achieve these optimum efficiencies, the value of the load resistance is constrained by the current and voltage swing

$$R_{opt} = \frac{v_o}{i_o} = \left(\frac{\overline{v}}{\overline{i}}\right)\left(\frac{V_{CC}}{I_Q}\right)$$

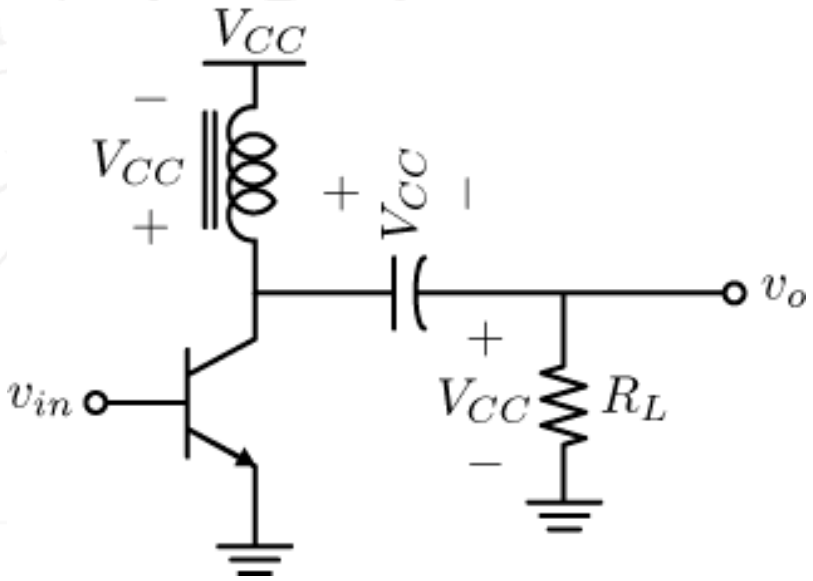
- Since the load resistance is usually fixed (e.g. antenna impedance), a matching network is required to present the optimum load to the amplifier.

Inductor Loaded CE/CS



- If we AC couple a load RL to the amplier, then the Q point of the amplifier collector voltage is set at V_{CC} through the choke inductor.
- The maximum swing is now nearly twice as large. Notice that the collector voltage can swing *above* the supply rail.

Swinging both ways …



- Recall that the voltage polarity across the inductor is given by dI/dt, which can go negative. Thus the collector voltage is equal to the supply minus or *plus* the absolute voltage across the inductor.

Improved Class A Efficiency

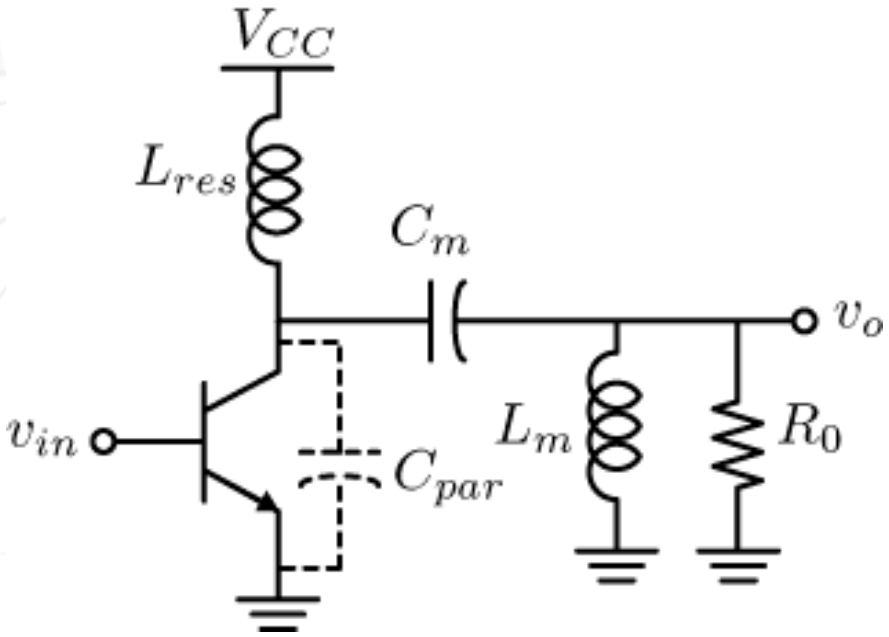
- Since the swing is almost double, the efficiency now approaches 50%

$$v_o \leq V_{CC}$$

$$\eta = \frac{1}{2}\frac{i_o v_o}{I_Q V_{CC}} \leq \frac{1}{2}$$

- In practice, due to losses in the components and back-off from maximum swing to minimize distortion, the actual efciency can be much lower.
- Package parasitics (see later slides) also limit the voltage swing.

Complete Class A Output Stage

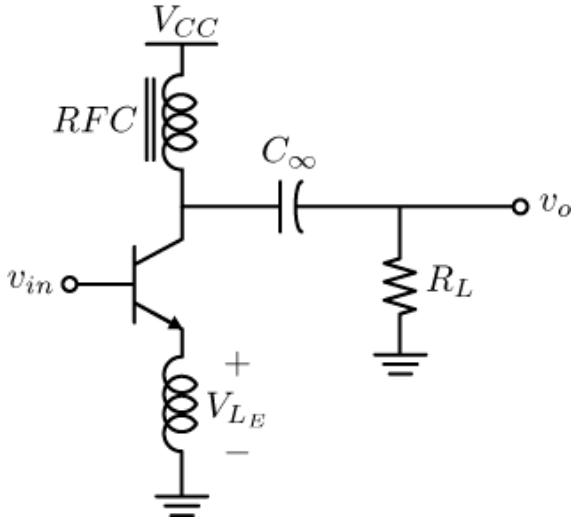


- In practice the collector inductor can double as a resonant element to tune out the collector parasitics.
- The coupling capacitor C_c can be replaced by a matching capacitor C_m.

Emitter Degeneration

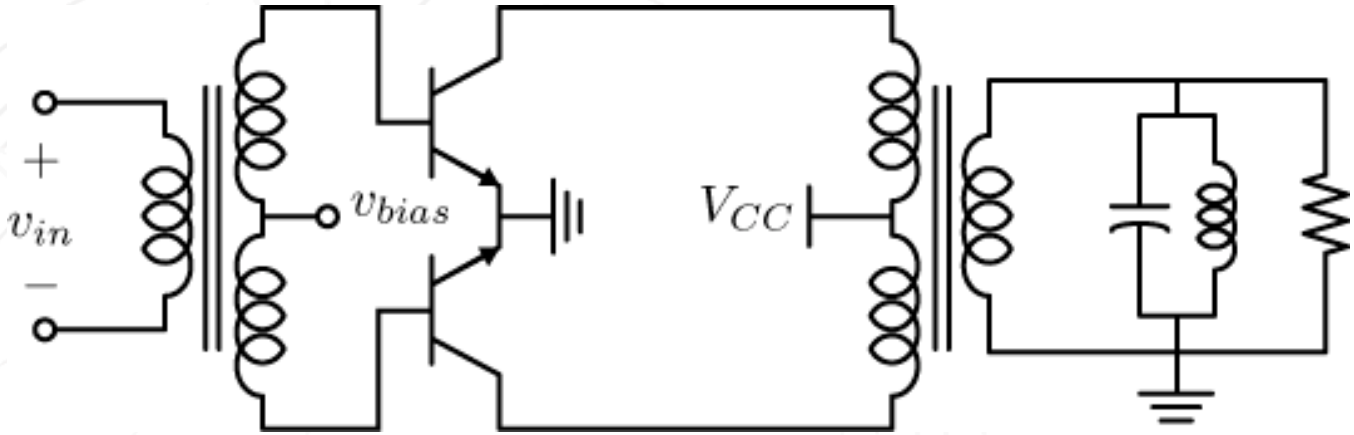
- Emitter inductance has a detrimental effect on PA efficiency since it reduces the swing. The voltage across the emitter is given by

$$V_E = j\omega L_E i_o$$



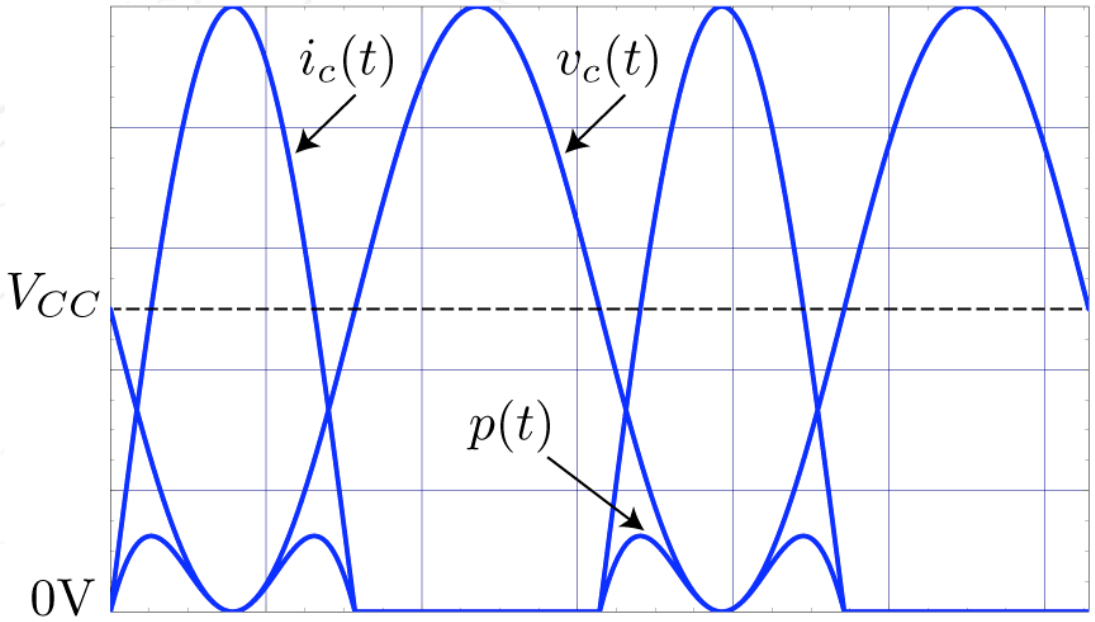
- For a current swing of 1A at 1 GHz, a typical parasitic inductance of 1 nH will "eat" up 6.28V of swing! We need to reduce L_E or to use a much higher V_{CC}.
- In practice both approaches are taken. We choose a technology with the highest breakdown voltage and the package with the lowest LE.

Class B



- The above circuit utilizes two transistors. Each device only delivers a half sinusoid pulse and the full sinusoid is recovered by phase inversion through the transformer.
- The base and collector bias voltages come from the transformer center tap. The base (or gate) is biased at the edge of conduction (threshold).

Class B Waveforms



- Since the voltage at the load is ideally a perfect sinusoid, the voltage on the collectors is likewise sinusoidal.
- The power dissipated by each transistor is thus the product of a sine and a half sine as shown above.

Class B Efficiency

- The average current drawn by each transistor is given by

$$I_Q = \frac{1}{T}\int_0^T i_c(t)dt = \frac{I_p}{T}\int_0^{T/2} \sin\omega t dt = \frac{I_p}{2\pi}\int_0^{\pi} \sin\theta d\theta = \frac{I_p}{\pi}$$

- Where I_p is the peak voltage drawn from the supply.
- The peak current drawn from the supply is just the load current swing reflected to the collector, $I_p = i_o \times n$.

$$\eta = \frac{1}{2}\left(\frac{I_p}{2I_Q}\right)\left(\frac{v_o}{V_{CC}}\right)$$

- Note that the total DC current draw is twice I_Q since both devices draw current from the supply.

Class B Efficiency (cont)

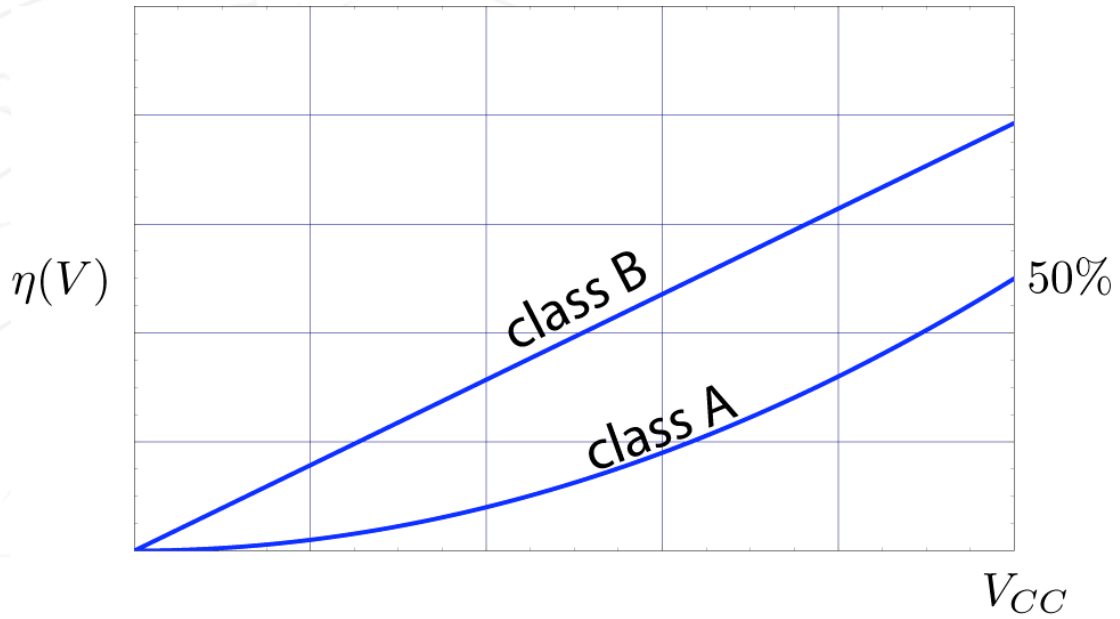
- Since the collector voltage swing can be as large as V_{CC} (similar to an inductively loaded Class A), the efficiency is bounded by

$$\eta \leq \frac{1}{2}\left(\frac{I_p}{2I_Q}\right) = \frac{1}{4}\left(\frac{I_p}{I_Q}\right)$$

$$\eta \leq \frac{\pi}{4} \approx 78\%$$

- This is a big improvement over the peak efficiency of Class A.
- Note that the average current naturally scales with output power, and so efficiency drops more gracefully as we back-off from peak power.

Efficiency versus Back-Off

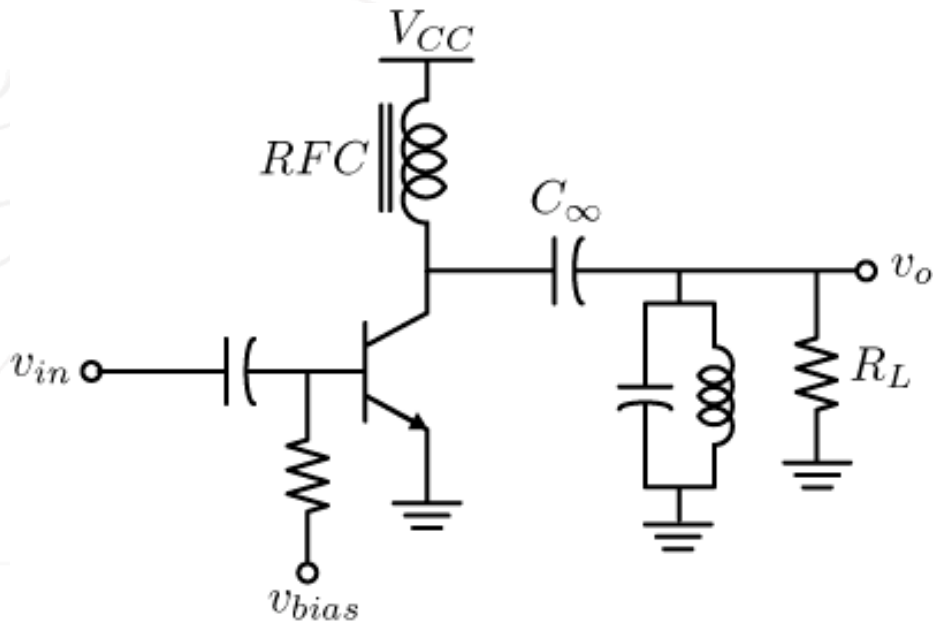


- The efficiency drops linearly as we back-off from the peak output voltage

$$\eta(v) = \frac{\pi}{4}\left(\frac{v_c}{V_{CC}}\right)$$

- where v_c is the collector voltage swing, which is just n times smaller than the load voltage, $v_c = v_o/n$.

Tuned Class B



- A tuned Class B amplifier works with a single devices by sending half sinusoid current pulses to the load. The device is biased at the edge of conduction.
- The load voltage is sinusoidal because a high Q RLC tank shunts harmonics to ground.

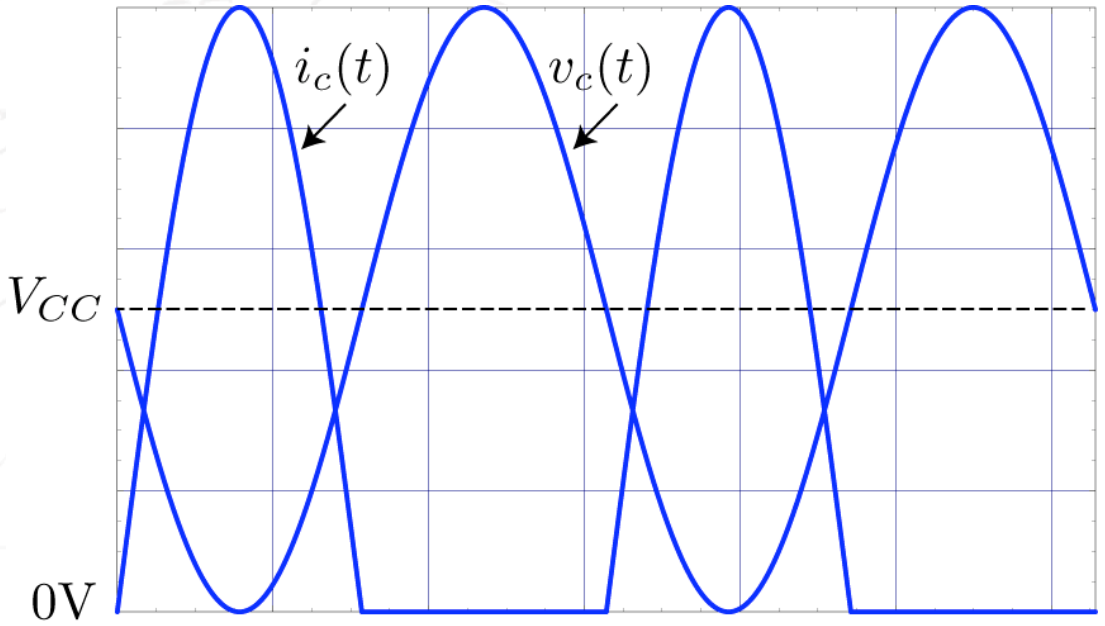
Class B Tank

- In a single transistor version, the "minus" pulse is in fact delivered by the RLC tank. The Q factor of the tank needs to be large enough to do this. This is analogous to pushing someone on a swing. You only need to push in one direction, and the reactive energy stored will swing the person back in the reverse direction.
- The average current drawn from the supply is the same as before, $I_Q = I_p/\pi$. The harmonic current delivered to the load is given by Fourier analysis of the half pulse

$$I_{\omega_1} = \frac{2}{2\pi} I_p \int_0^{\pi} \sin\theta sin\theta d\theta = \frac{1}{\pi} I_p \int_0^{\pi} \frac{1-\cos 2\theta}{2} d\theta$$

$$= \frac{1}{\pi}\frac{\pi}{2} I_p = \frac{I_p}{2}$$

Class B Waveforms



- We see that the transistor is cut-off when the collector voltage swings above V_{CC}. Thus, the power dissipated during this first half cycle is zero.
- During the second cycle, the peak current occurs when the collector voltage reaches zero.

Class B Efficiency (again)

- The efficiency is therefore the same

$$\eta = \frac{1}{2}\frac{I_{\omega_1}}{I_Q}\frac{v_c}{V_{CC}} =\leq \frac{1}{2}\frac{\pi}{2} = \frac{\pi}{4}$$

- The DC power drawn from the supply is proportional to the output voltage

$$P_{dc} = I_Q V_{CC} = \frac{V_{CC} I_p}{\pi} \qquad I_p = \frac{v_c}{R_{opt}} = \frac{n v_o}{R_{opt}}$$

- The power loss in the transistor is given by

$$p_t(t) = \frac{1}{2\pi}\int_0^{\pi} I_p \sin\theta (V_{CC} - v_c \sin\theta) d\theta$$

Transistor Power Loss

- Integrating the above expression

$$p_t(t) = \frac{V_{CC} I_p}{2\pi} \left(-\cos\theta \Big|_0^{\pi} - \frac{v_c}{I_p} 2\pi \right.$$

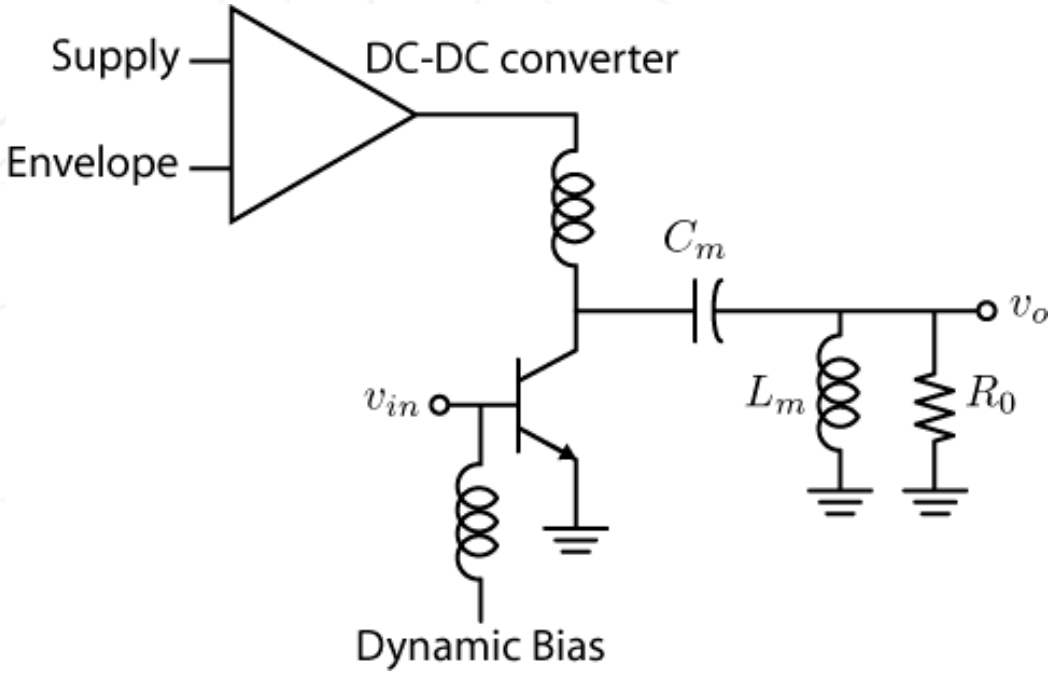
$$= \frac{1}{2\pi} \left(2V_{CC} I_p - \frac{v_c I_p}{2} \pi \right)$$

$$= \frac{I_p}{\pi} V_{CC} - \frac{v_c I_p}{4}$$

$$= I_Q \cdot V_{CC} - \frac{v_c I_{\omega_1}}{2}$$

$$= P_{dc} - P_L$$

Dynamic PA

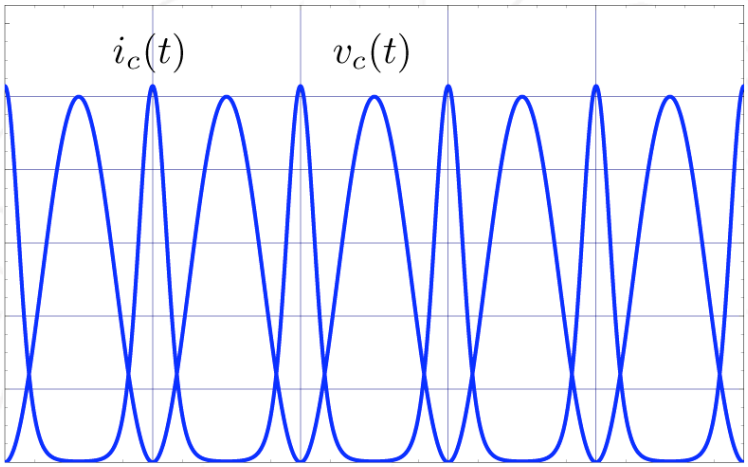


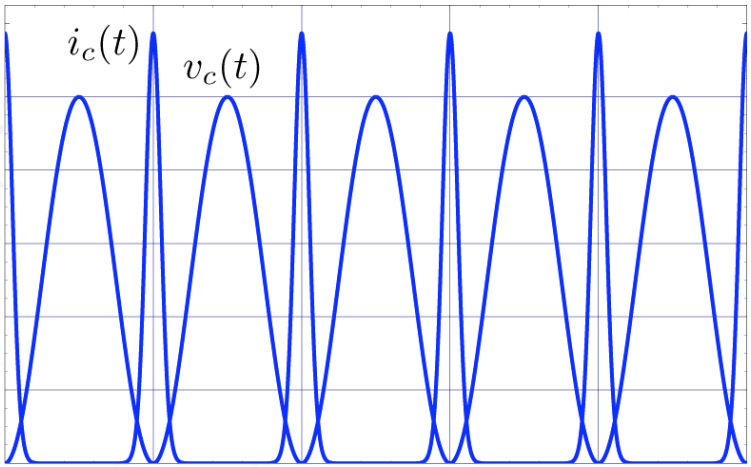
- Envelope tracking supply and dynamic class-A
- Efficiency always close to peak efficiency of amplifier (say 30%) regardless of PAR
- Need a very fast DC-DC converter

Conduction Angle

- Often amplifiers are characterized by their conduction angle, or the amount of time the collector current flows during a cycle.
- Class A amplifiers have 360° conduction angle, since the DC current is always flowing through the device.
- Class B amplifiers, though, have 180° conduction angle, since they conduct half sinusoidal pulses.
- In practice most Class B amplifiers are implemented as Class AB amplifiers, as a trickle current is allowed to flow through the main device to avoid cutting off the device during the amplifier operation.

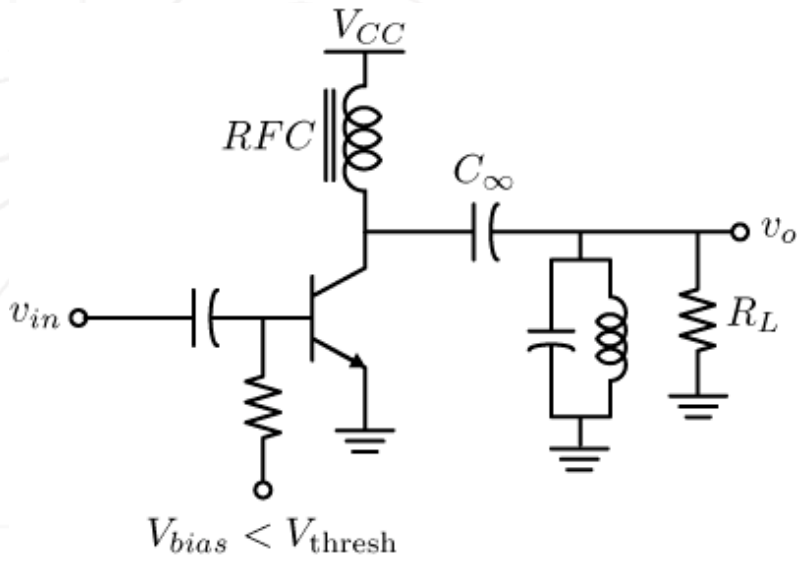
Reducing the Conduction Angle





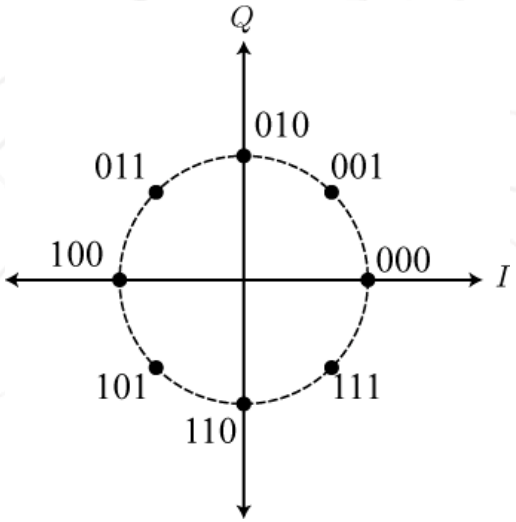
- The most optimal waveform is shown above, where a current pulse is delivered to the load during the collector voltage minimum (ideally zero)
- As the pulse is made sharper and sharper, the efficiency improves. To deliver the same power, though, the pulse must be taller and taller as it's made more narrow. In fact, in the limit the current spike approaches a delta function.

Class C



- Class C amplifiers are a wide family of amplifiers with conduction angle less than 180°. One way to achieve this is to bias a transistor below threshold and allow the input voltage to turn on the device for a small fraction of the cycle.

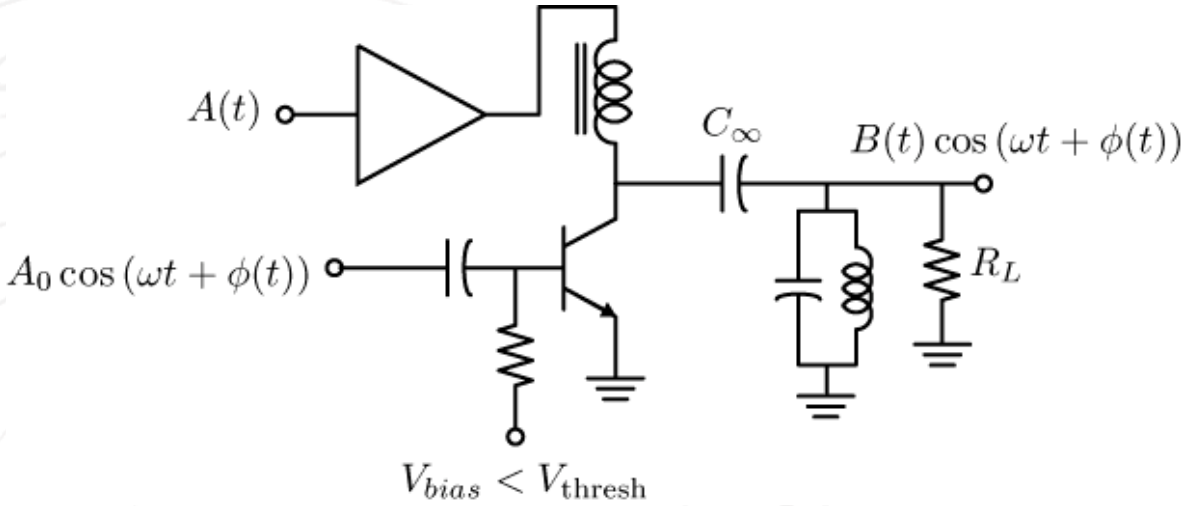
Class C Linearity



$$I^2 + Q^2 = A^2$$

- The Class C amplifier is very non-linear, and it is only appropriate for applications where the modulation is constant envelope. For instance, FM uses a constant amplitude carrier and only modulates the frequency to convey information. Likewise, any digital modulation scheme with a constellation in a circle is constant envelope

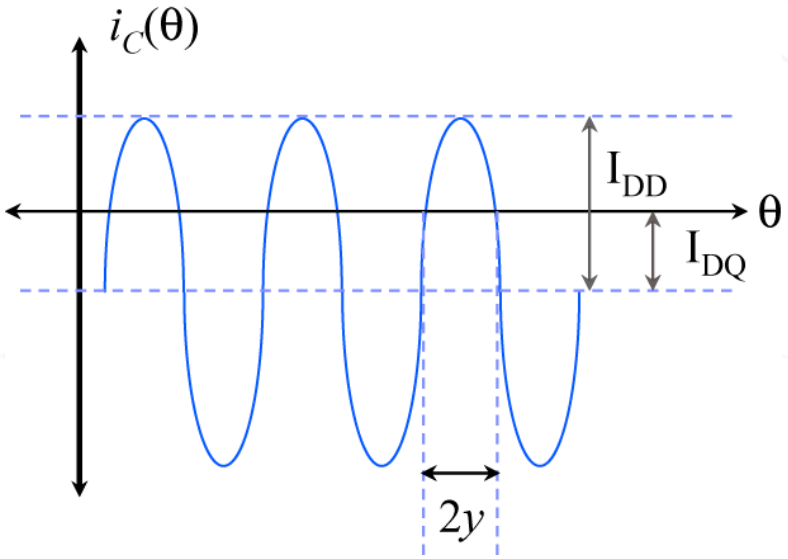
Polar Modulation



- While the amplifier is a non-linear function of the input amplitude, the Class C amplifier can be made to act fairly linearly to the collector voltage.
- By driving the amplifier into "saturation" in each cycle, e.g. with a large enough swing to rail the supplies, then the output power is related to the voltage supply. Collector modulation then uses the power supply to introduce amplitude modulation into the carrier.

Class C Approximate Analysis

- Assume current pulses are sine wave tips:



conduction angle is $2y$

$$I_{DD}\cos y = I_{DQ}, \qquad y = \cos^{-1}\left(\frac{I_{DQ}}{I_{DD}}\right)$$

$$i_D(\theta) = \begin{cases} -I_{DQ} + I_{DD}\sin\theta, & I_{DD}\sin\theta \geq I_{DQ} \\ 0, & \text{otherwise} \end{cases}$$

- I_{DC} from supply:

$$I_{DC} = \frac{1}{2\pi}\int_0^{2\pi} i_D(\theta)d\theta = \frac{1}{\pi}\int_0^{y}(I_{DD}\cos\theta - I_{DQ})d\theta$$

$$I_{DC} = \frac{1}{\pi}(I_{DD}\sin y - I_{DQ}y)$$

$$I_{DC} = \frac{I_{DD}}{\pi}(\sin y - y\cos y)$$

Class C Analysis (cont)

- Output voltage is: $V_{OM} = \text{Fund}\{-i_D(\theta)R_L\}$
- Since i_D is an odd function, the Fourier series will only yield sine terms

$$V_{OM} = \frac{-2R}{2\pi}\int_0^{2\pi} i_D(\theta)\sin\theta d\theta = \frac{2R}{\pi}\int_0^{y}(I_{DD}\cos\theta - I_{DQ})\cos\theta d\theta$$

$$V_{OM} = \frac{2R}{\pi}\left(\frac{I_{DD}y}{2} + \frac{I_{DD}\sin 2y}{4} - I_{DQ}\sin y\right)$$

$$V_{OM} = \frac{I_{DD}R}{2\pi}(2y - \sin 2y)$$

- DC power from prev page: $P_{DC} = I_{DC}V_{CC} = \frac{I_{DD}V_{CC}}{\pi}(\sin y - y\cos y)$
- Assuming that max swing ~ VCC:

$$V_{OM} \cong V_{CC} = \frac{I_{DD}R_L}{2\pi}(2y - \sin 2y)$$

$$P_{DC} \cong \frac{2V_{CC}^2}{R_L}\frac{\sin y - y\cos y}{2y - \sin 2y}$$

Class C Efficiency

- Power to load (assuming VCC swing): $P_L = \frac{V_{CC}^2}{2R_L}$
- Ideal Efficiency:

$$\eta = \frac{P_L}{P_{DC}} = \frac{1}{4}\frac{(2y - \sin 2y)}{(\sin y - y\cos y)}$$

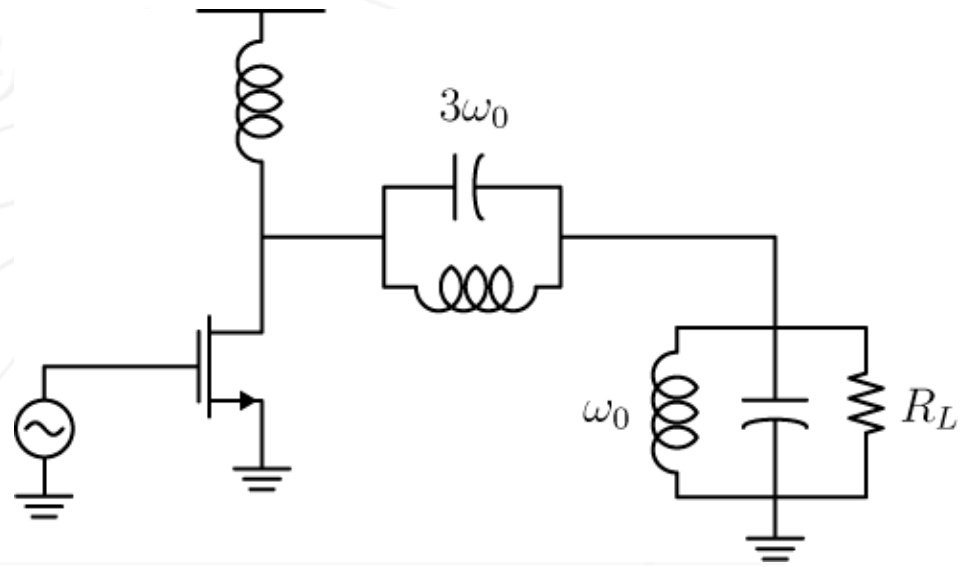
$$\lim_{y \to 0} \eta(y) = 100\% \qquad \text{(ideal class C)}$$

$$\eta(\pi) = 50\% \qquad \text{(tuned-circuit Class A)}$$

$$\eta(\tfrac{\pi}{2}) = 78.5\% \qquad \text{(single-ended Class B)}$$

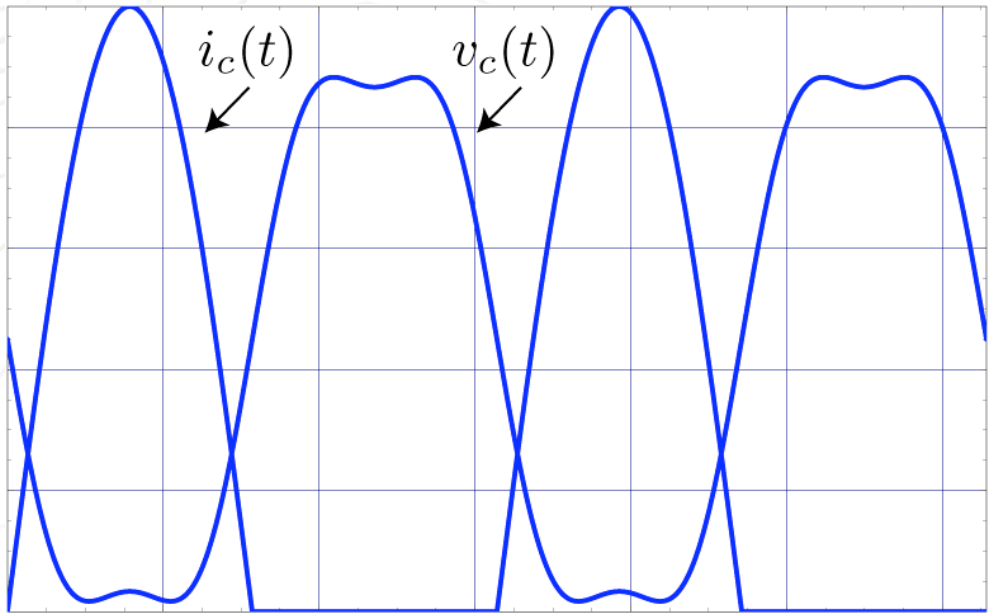
- For small conduction angle current pulses approach delta-function.
- Many practical issues make Class C difficult to design.

Class F Circuit



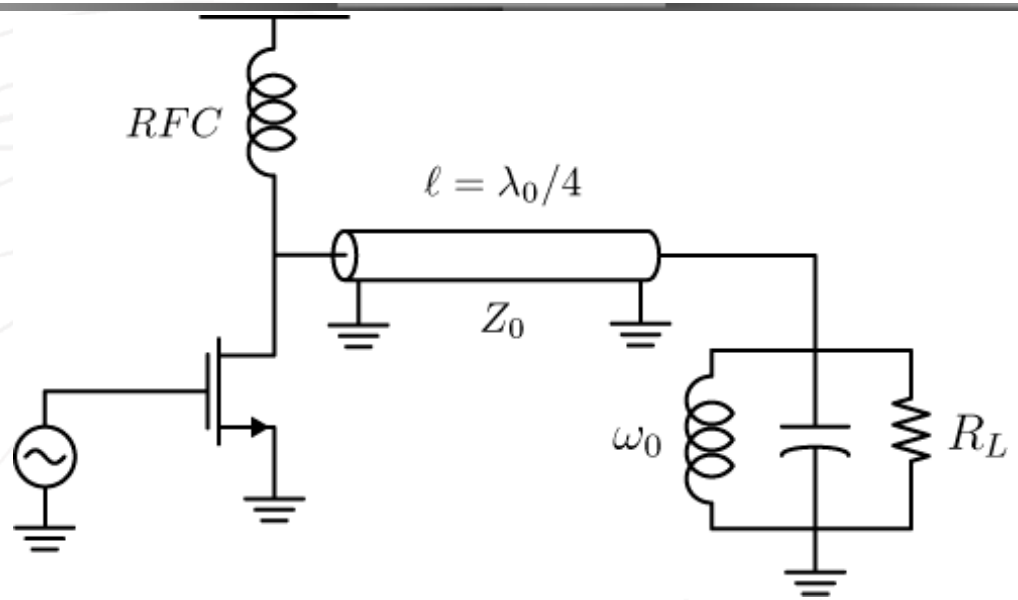
- The above circuit isolates the fundamental resonant load from the drain at the third harmonic, allowing the drain voltage to contain enough third harmonic to create a more square like waveform.
- It can be shown that just adding a third harmonic boost the efficiency from 78% (Class B) to 88%.

Class F



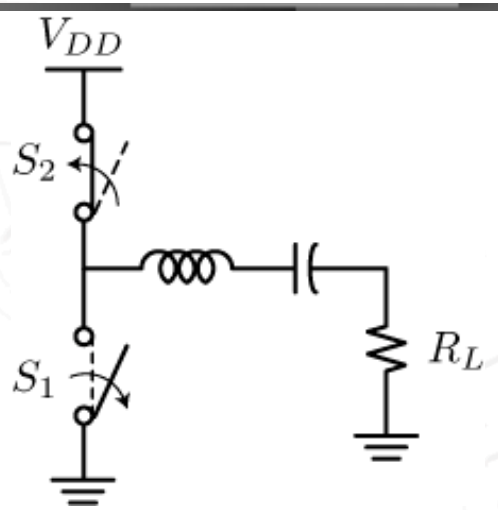
- Since it's difficult to create extremely narrow pulses at high frequency, we can take a different approach and attempt to square up the drain voltage.

Quarter Wave Class F



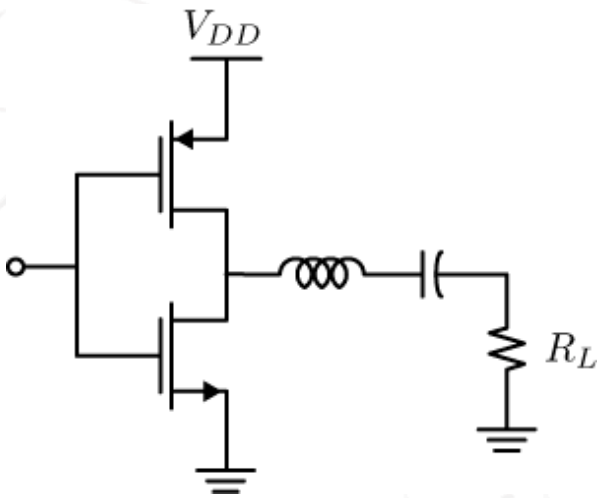
- In this circuit a quarter wave transformer converts the low impedance at the load (due to the capacitance) at harmonics of the fundamental to a high impedance for all odd harmonics. Even harmonics are unaltered as they see a λ/2 line.
- In theory then we can create a perfect square wave at the drain of the transistor and thus achieve 100% efficiency.

Ideal Class D Switching Amplifier



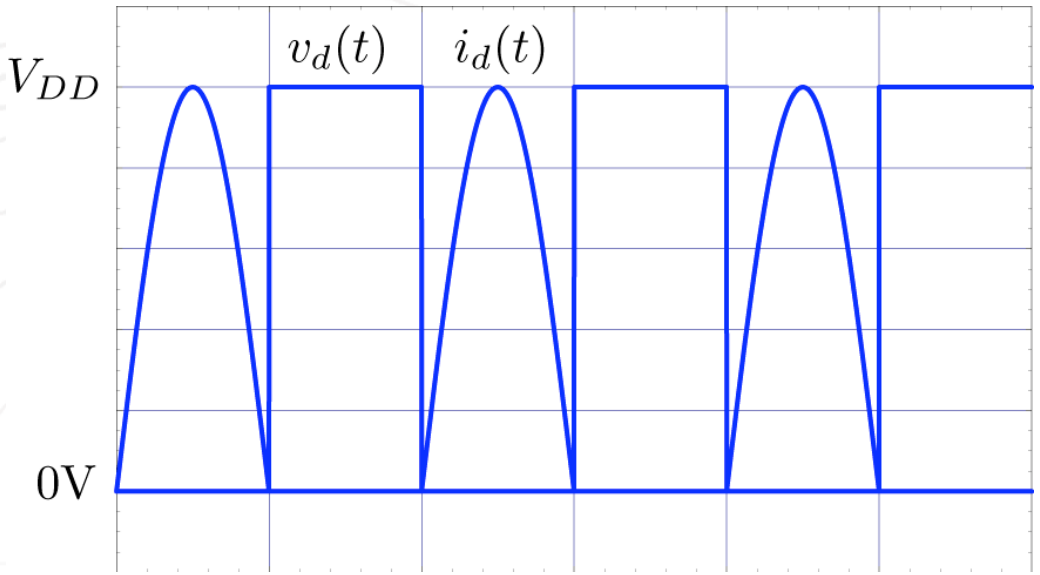
- If give up linearity, then we can create some intrinsically efficient amplifiers using switches. An ideal switch does not dissipate any power since either the voltage or current is zero.
- By varying the switching rate, we can impart frequency modulation onto the load.
- A real switch has on-resistance and parasitic off capacitance and conductance.

MOS Class D Inverter



- Switching amplifiers are realized with transistors operating as switches. MOS transistors make particularly good switches.
- The input voltage is large enough to quickly move the operating point from cut-off to triode region.

Class D Waveforms



- The MOS drain voltages switches from V_{SS} to V_{DD} at the rate of the input signal.
- A series LCR filter only allows the first harmonic of voltage to flow into the load. Since current only flows through a device when it's fully on (ideally $V_{ds} = 0$), little power dissipation occurs in the devices.

Class D Efficiency

- We can see that the efficiency has to be 100% for an ideal switch. That's because there is no where for the DC power to flow except to the load.
- The collector voltage can be decomposed into a Fourier series

$$v_d = \frac{V_{DD}}{2}\left(1 + s(\omega t)\right)$$

$$s(\theta) = \text{sign}(\sin(\theta)) = \frac{4}{\pi}\left(\sin\theta + \frac{1}{3}\sin 3\theta + \frac{1}{5}\sin 5\theta + \cdots\right)$$

- The load current is therefore

$$i_L = \frac{4}{\pi}\frac{V_{DD}}{2R}\sin\theta = \frac{2V_{DD}}{\pi R_L}\sin\theta$$

Class D Efficiency (cont)

- The load power is thus

$$P_L = \frac{i_L^2 R_L}{2} = \frac{2}{\pi^2}\frac{V_{DD}^2}{R_L} \approx 0.2\frac{V_{DD}^2}{R_L}$$

- The drain current are half-sinusoid pulses. The average current drawn from the supply is the average PMOS current

$$I_Q = \frac{I_p}{\pi} = \frac{2}{\pi^2}\frac{V_{DD}}{R_L}$$

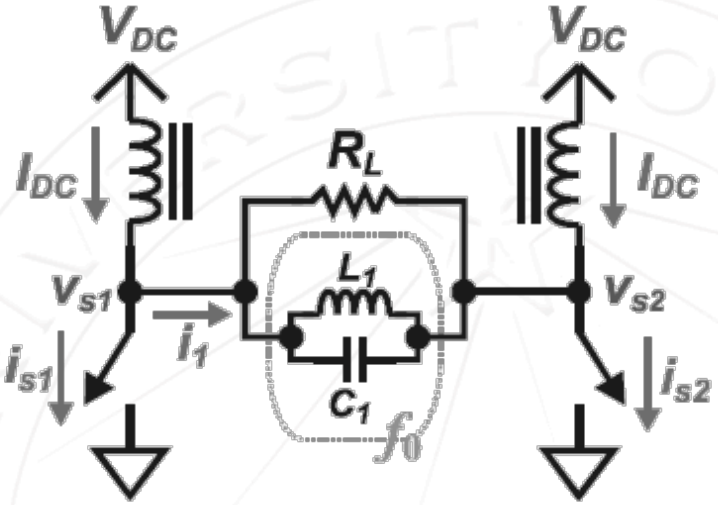
$$P_{DC} = I_Q \cdot V_{DD} = \frac{2V_{DD}^2}{\pi^2 R_L} = P_L$$

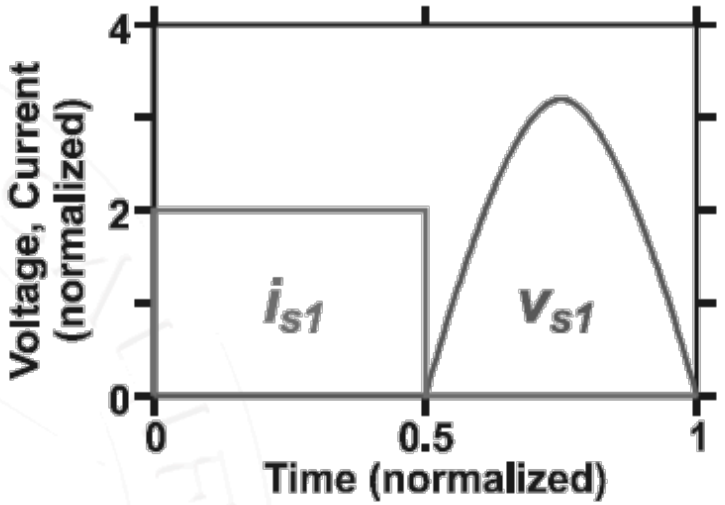
- As we expected, the ideal efficiency is $\eta = 100\%$

Class D Reality

- As previously noted, a real Class D amplifier efficiency is lowered due to the switch on-resistance. We can make our switches bigger to minimize the resistance, but this in turn increases the parasitic capacitance
- There are two forms of loss associated with the parasitic capacitance, the capacitor charging losses CV^2f and the parasitic substrate losses.
- The power required to drive the switches also increases proportional to C_{gs} since we have to burn CV^2f power to drive the inverter. A resonant drive can lower the drive power by the Q of the resonator.
- In practice a careful balance dictates the maximum switch size

Class D^{-1}





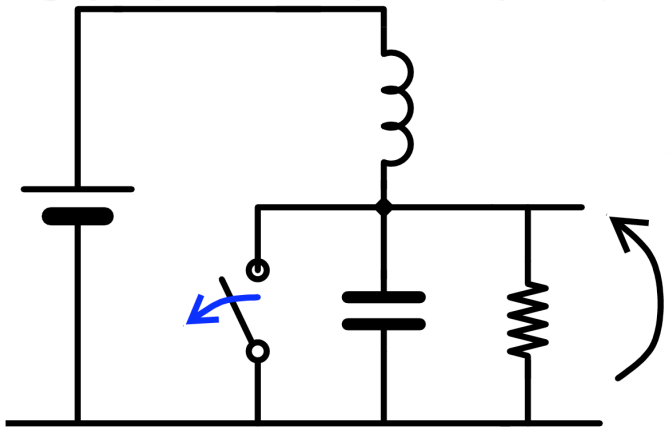
- The "Dual" Class D amplifier (interchange voltage/current → square wave current, sinusoidal voltage, parallel LCR filter)
- Chokes act like current sources. ZVS by "design" but only if there is no device capacitance to begin with.

$$v_{s1} = \begin{cases} 0 & 0 < \theta < \pi \\ -\frac{4}{\pi} I_{DC} R_L \sin(\theta) & \pi < \theta < 2\pi \end{cases}$$

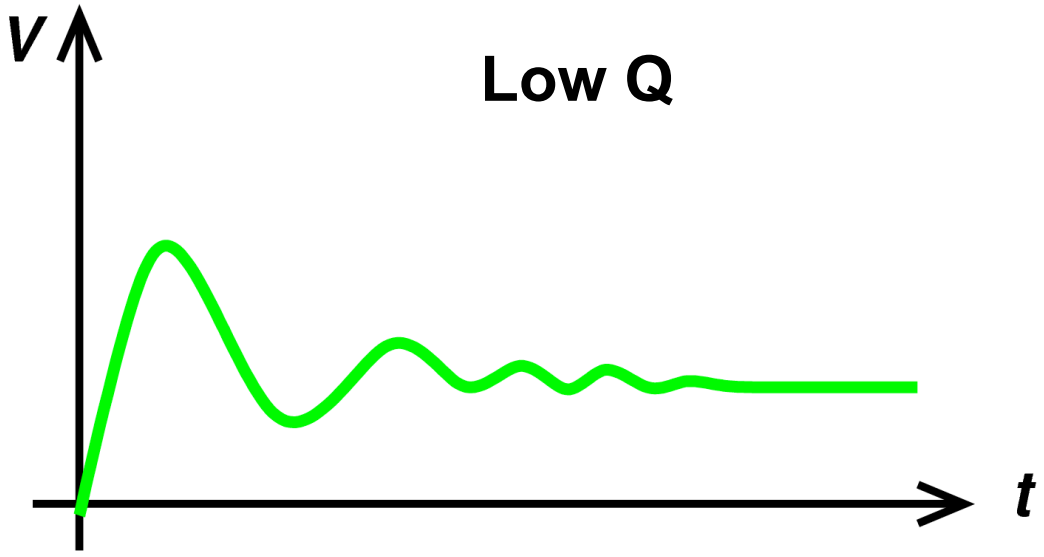
Switching RF Power Amplifier

Source: Patrick Reynaert and Michiel Steyaert

- switching amplifier = LC network and a switch



$$Q = R\sqrt{\frac{C}{L}}$$



Switching RF Power Amplifier

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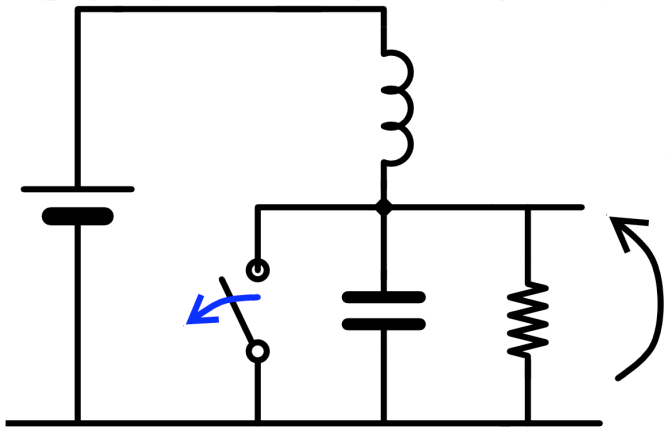

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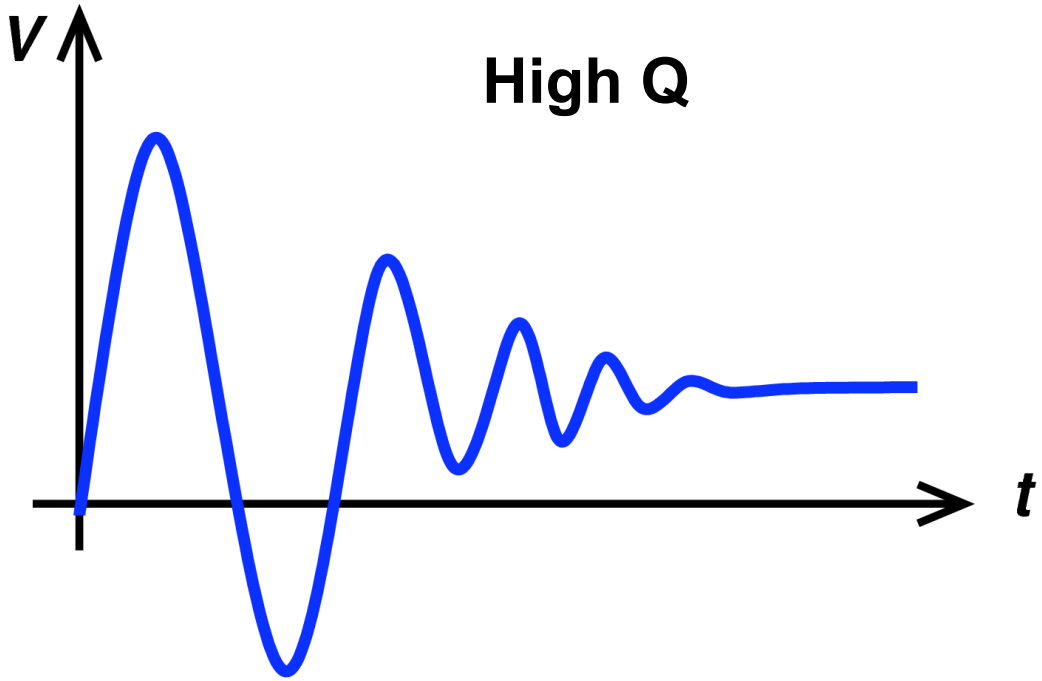

Switching RF Power Amplifier

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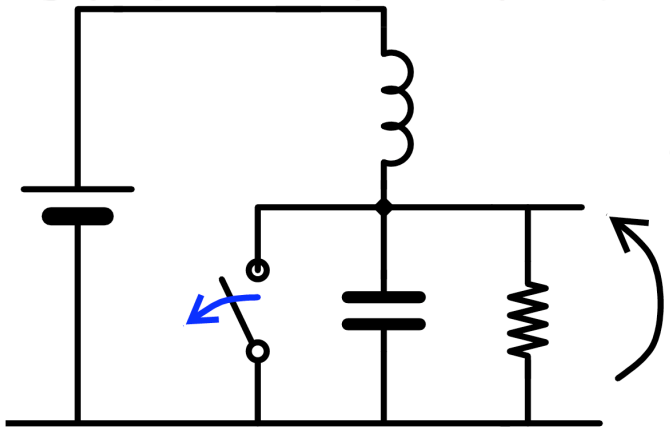
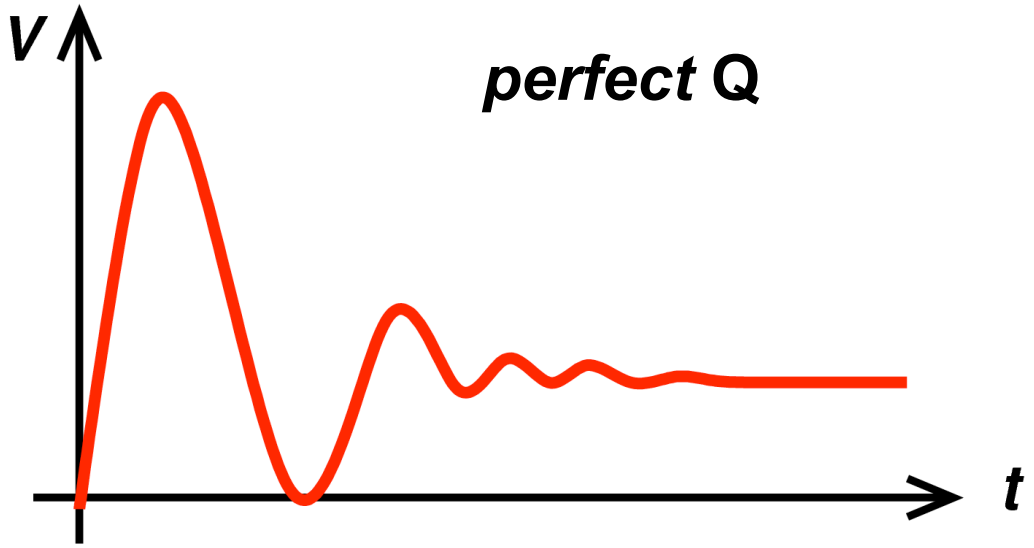


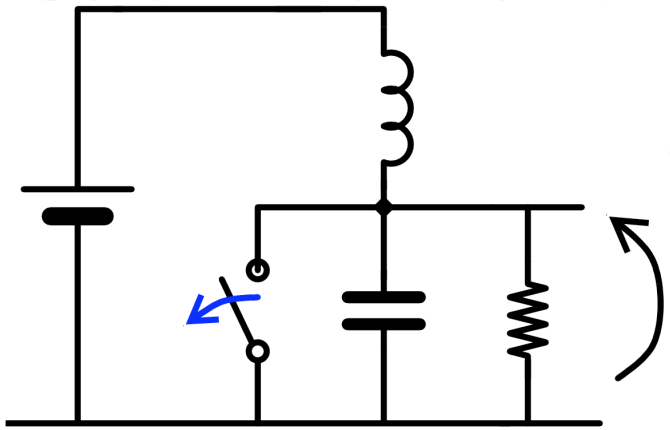
$$Q = R\sqrt{\frac{C}{L}}$$



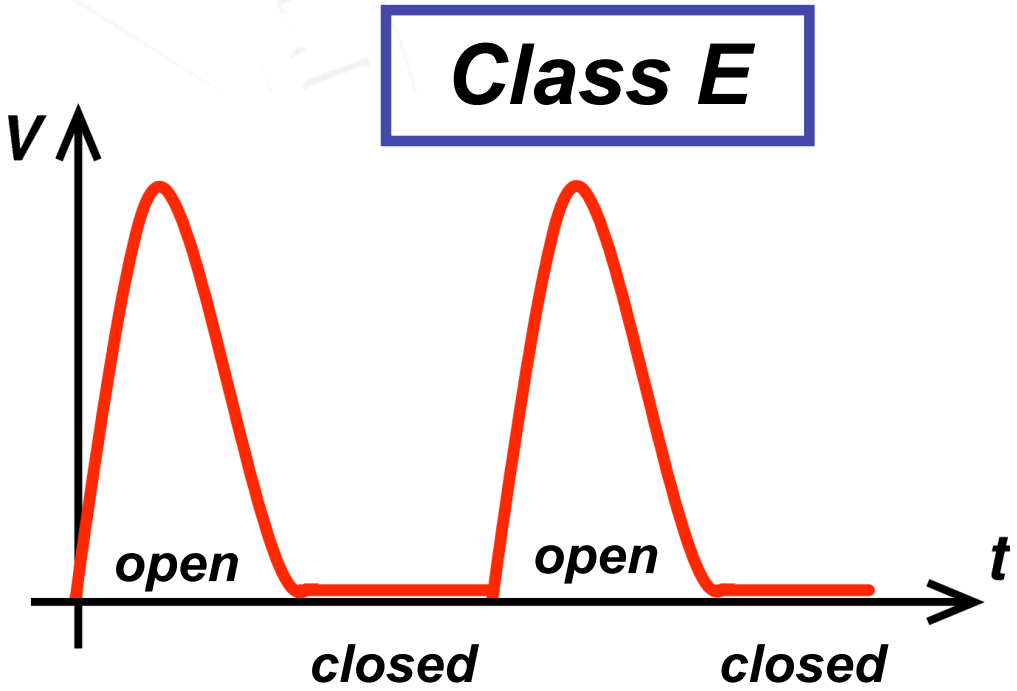
Switching RF Power Amplifier

Source: Patrick Reynaert and Michiel Steyaert

- switching amplifier = LC network and switch



$$Q = R\sqrt{\frac{C}{L}}$$



Switching RF Power Amplifier

Source: Patrick Reynaert and Michiel Steyaert

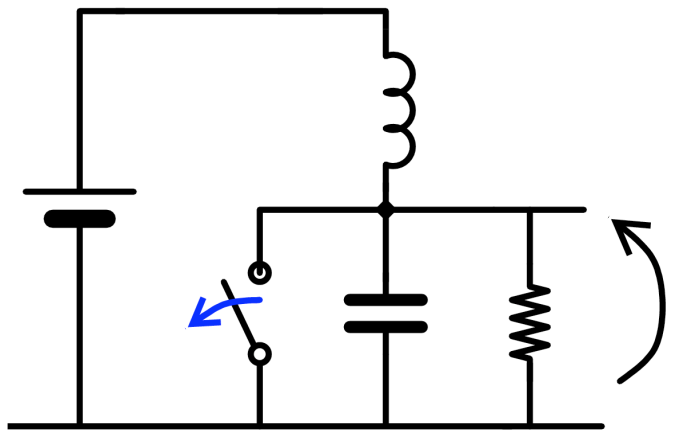
☹ **Output power of Class E is low**

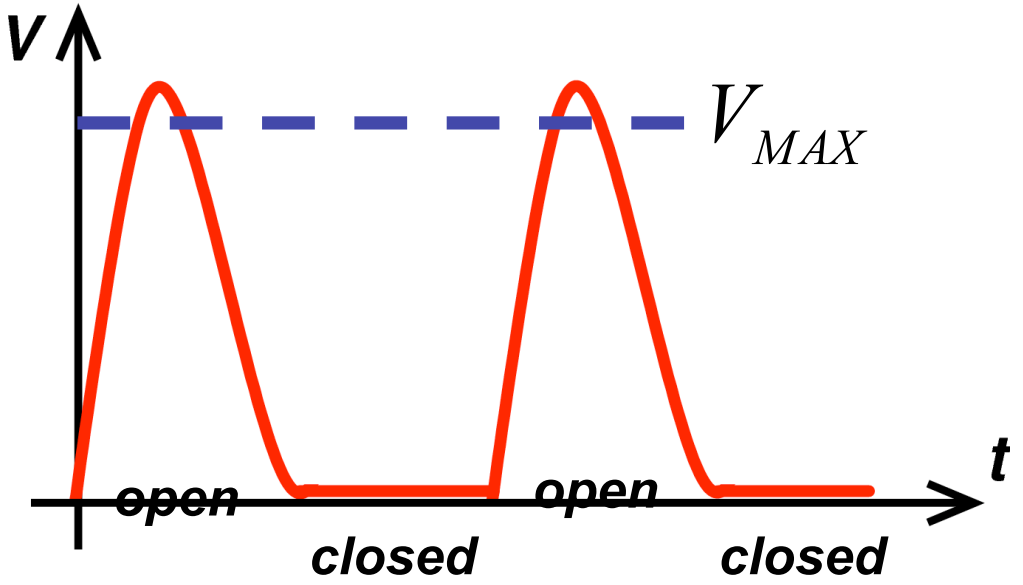
$$P_{OUT} < 0.045 \frac{V_{MAX}^2}{R_{LOAD}}$$

Class A: $P_{ClassA} = 0.125 \cdot \frac{V_{MAX}^2}{R_{LOAD}}$

0.35um technology (V_{MAX} = 8V)

→ P_{OUT} < 60mW @ 50 Ohm





Class E Amplifier

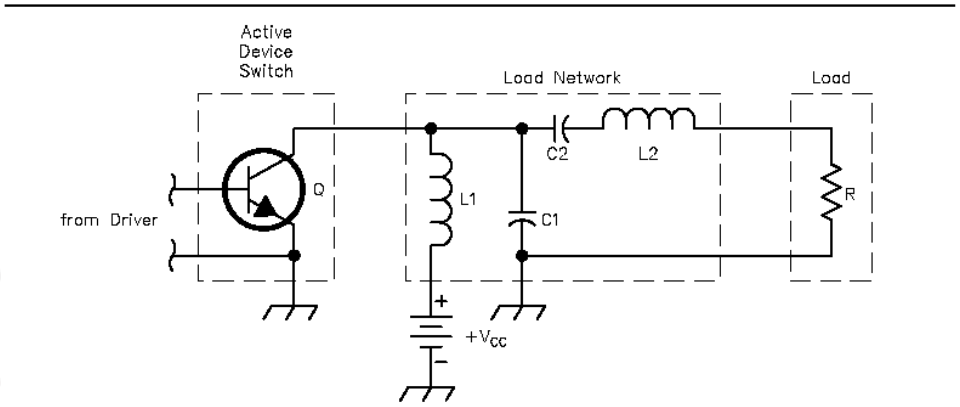
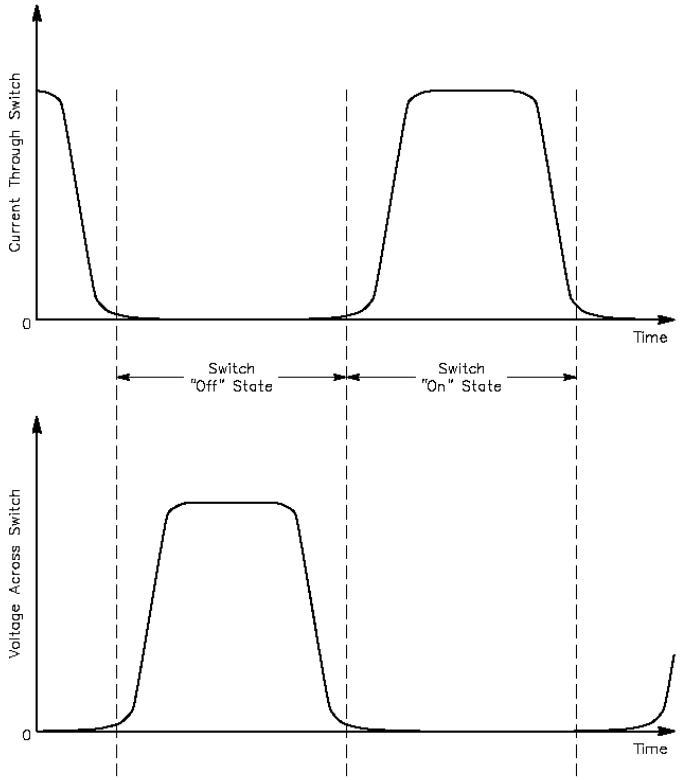


Fig 2—Schematic of a low-order Class-E amplifier.

- Switching PA like Class D but can absorb transistor parasitic capacitance into load network. This allows the switch to become very large (low on-resistance).
- The load network is design to ensure zero switching condition.



Figures: Class-E RF Power Amplifiers, By Nathan O. Sokal, Design Automation, Inc

Class E Waveforms

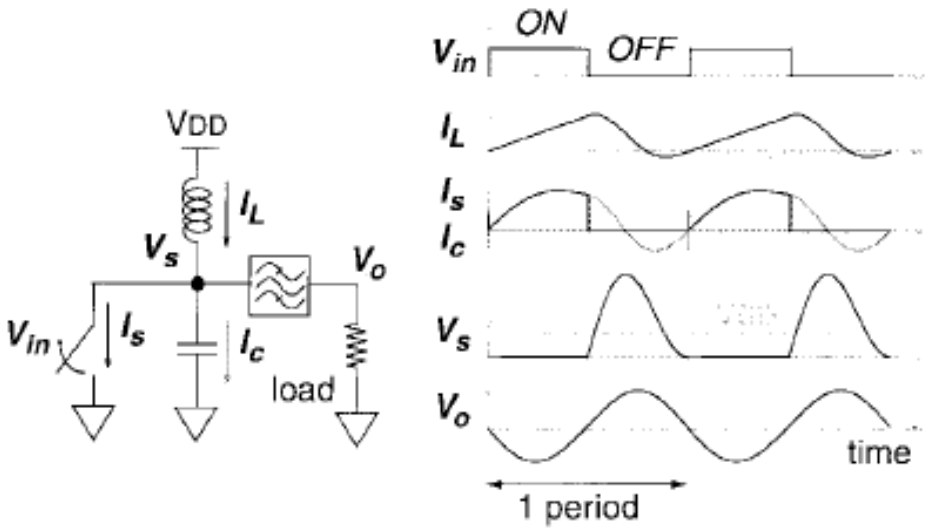


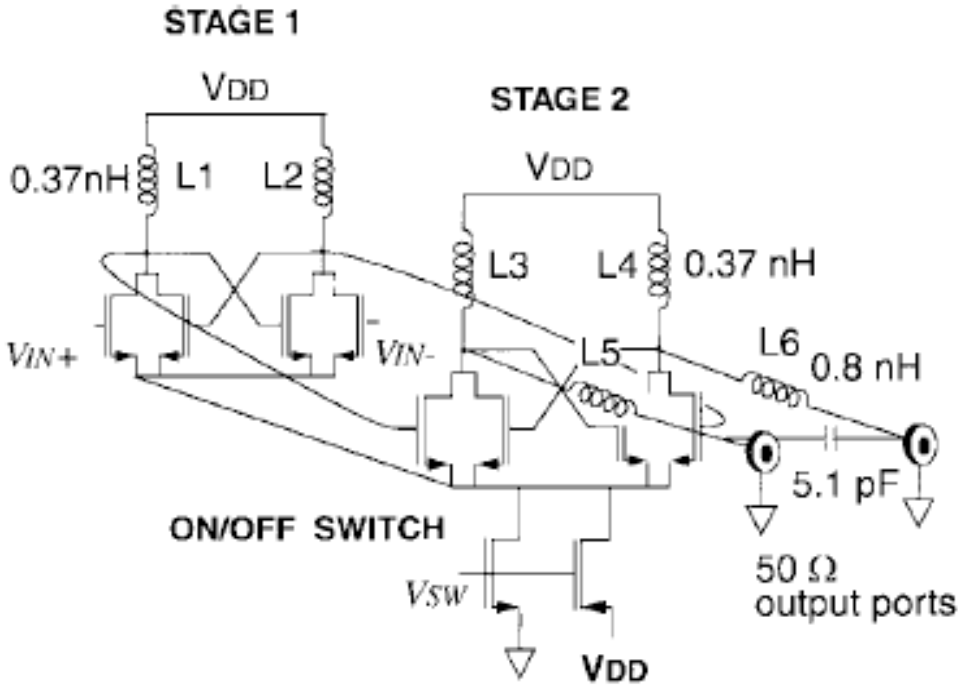
Figure: A 1.9-GHz, 1-W CMOS Class-E Power Amplifier for Wireless Communications, King-Chun Tsai and Paul R. Gray

- Problems with Class E include low power gain and large voltage swings. The drain waveform can swing to more than 3.5 times the supply voltage. This means the transistors have to be able to handle much larger voltages.
- Efficiency for this class of PA is extremely good.

First GSM CMOS Class E

Martin Tsai (UCB '99)

- Use standard CMOS to achi output power of 1W
- Measured efficiency > 50%
- Use cross-coupled devices t boost driver capability (requires injection locking)

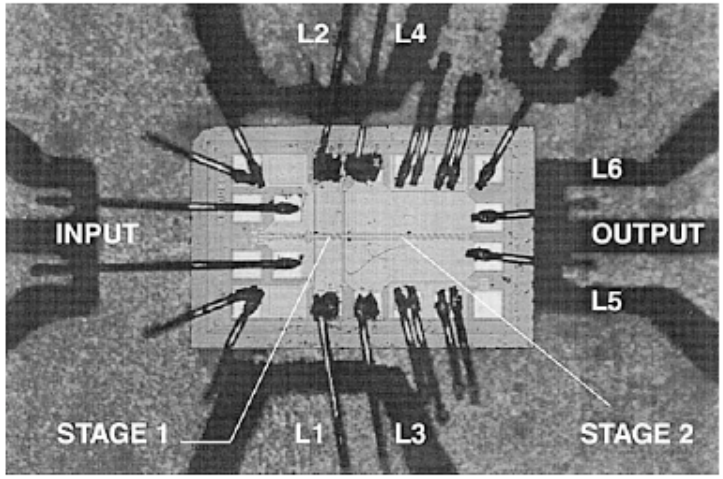


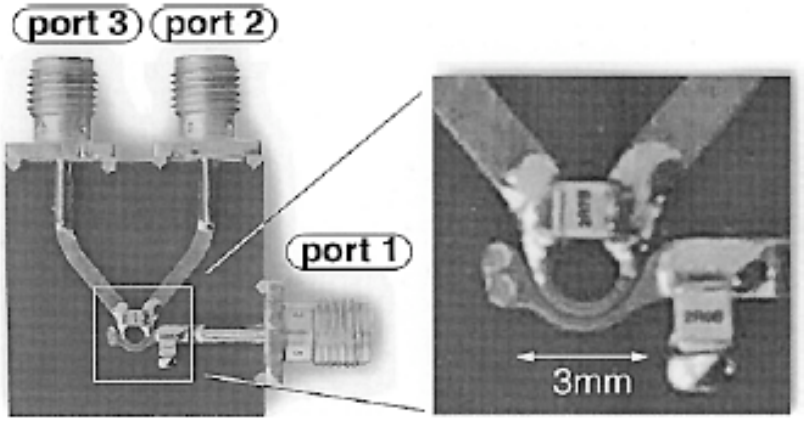
TRANSISTOR SIZING

STAGE 1	STAGE 2	ON/OFF SWITCH
Input: 980/0.35	Input: 3600/0.35	NMOS: 31580/0.35
Assist: 980/0.35	Assist: 4800/0.35	PMOS: 500/0.35

Source: A 1.9-GHz, 1-W CMOS Class-E Power Amplifier for Wireless Communications, King-Chun Tsai and Paul R. Gray

Output Matching





- Use chip-on-board testing (avoid lead inductance)
- Use a microstrip balun to convert from differential to single-ended to drive antenna

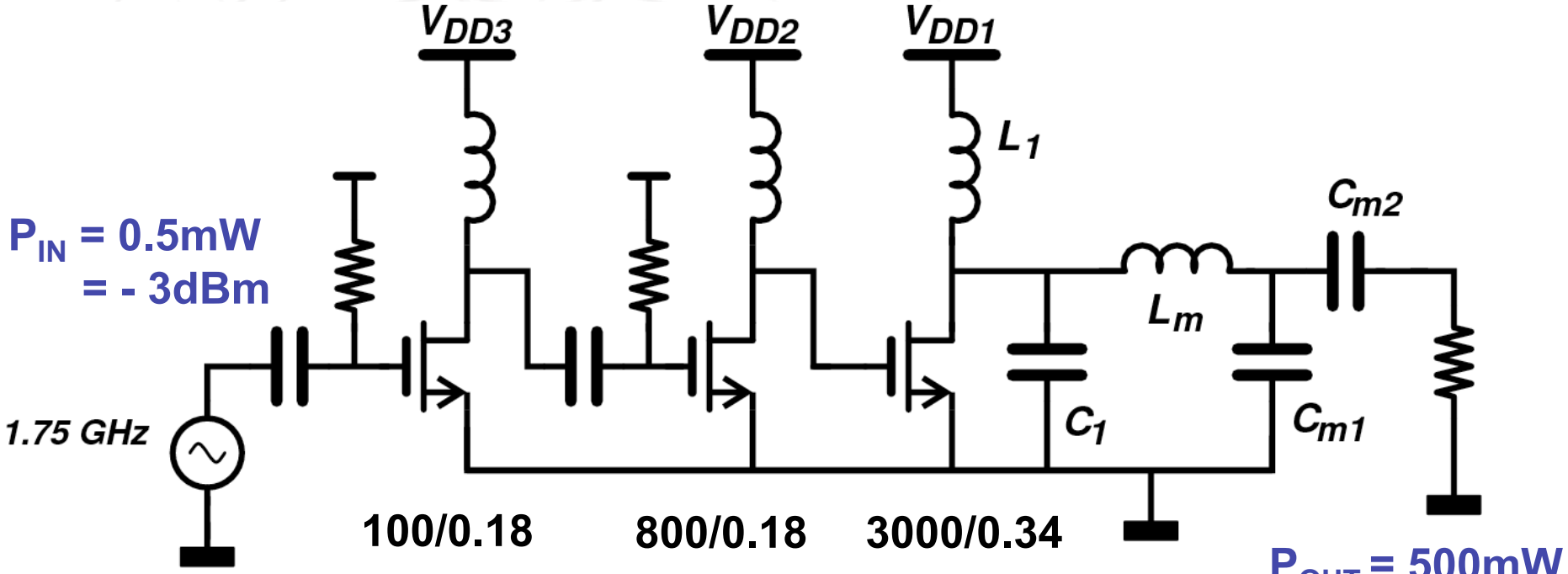
Source: A 1.9-GHz, 1-W CMOS Class-E Power Amplifier for Wireless Communications, King-Chun Tsai and Paul R. Gray

RF CMOS Class-E PA

Source: Patrick Reynaert and Michiel Steyaert

Implemented in a 0.18 um CMOS technology

P_3 = 66mW P_2 = 120mW P_1 = 1250mW

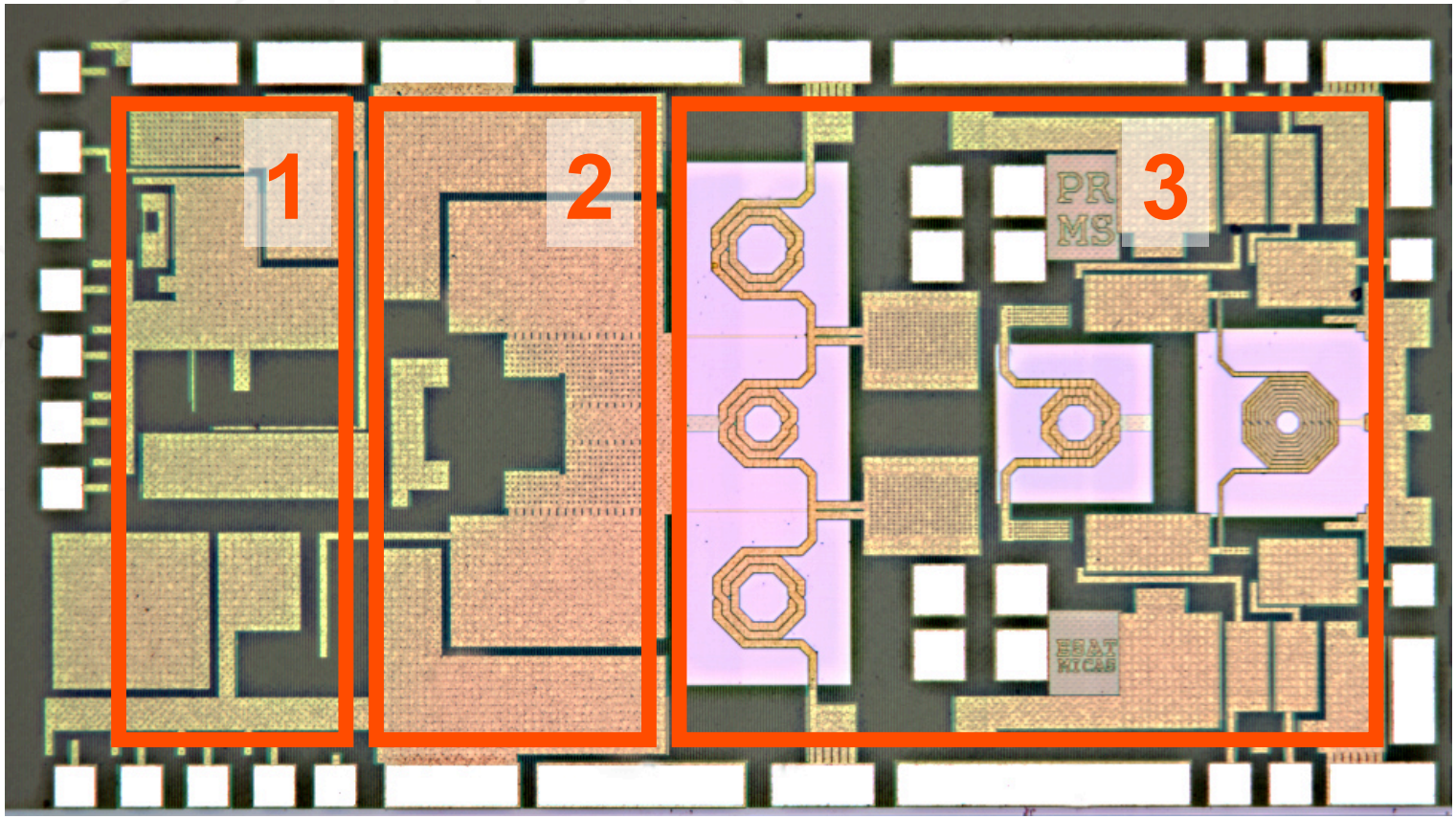


$$\eta_1 = \frac{P_{OUT}}{P_1} = 40\% \qquad \eta_{total} = \frac{P_{OUT}}{P_1 + P_2 + P_3} = 34\%$$

Gain = 30dB

Chip micrograph

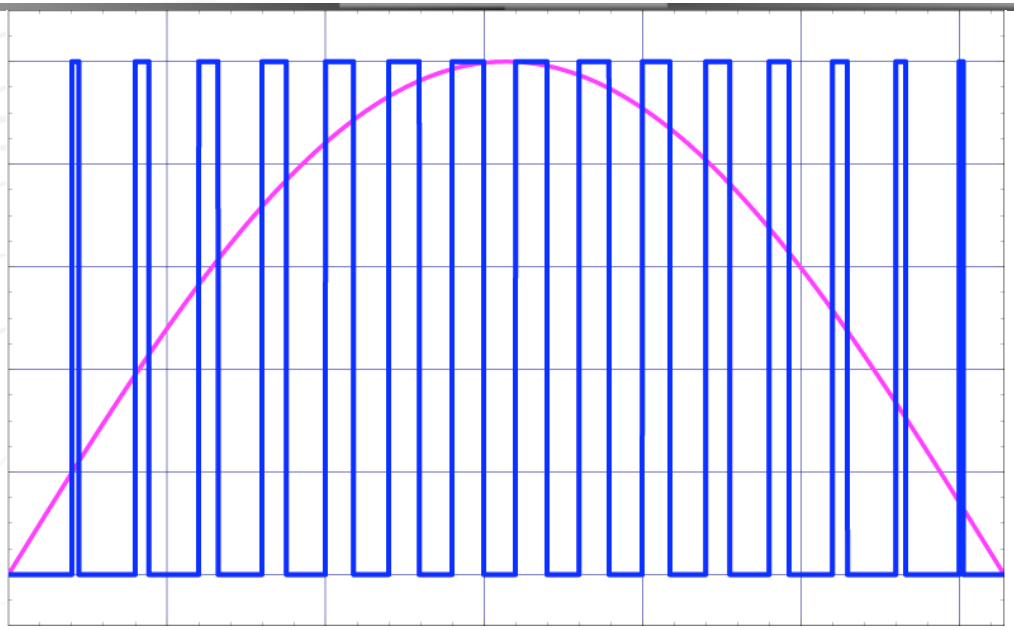
Source: Patrick Reynaert and Michiel Steyaert



1. Voltage regulator
2. Polar modulator
3. RF Power Amplifier

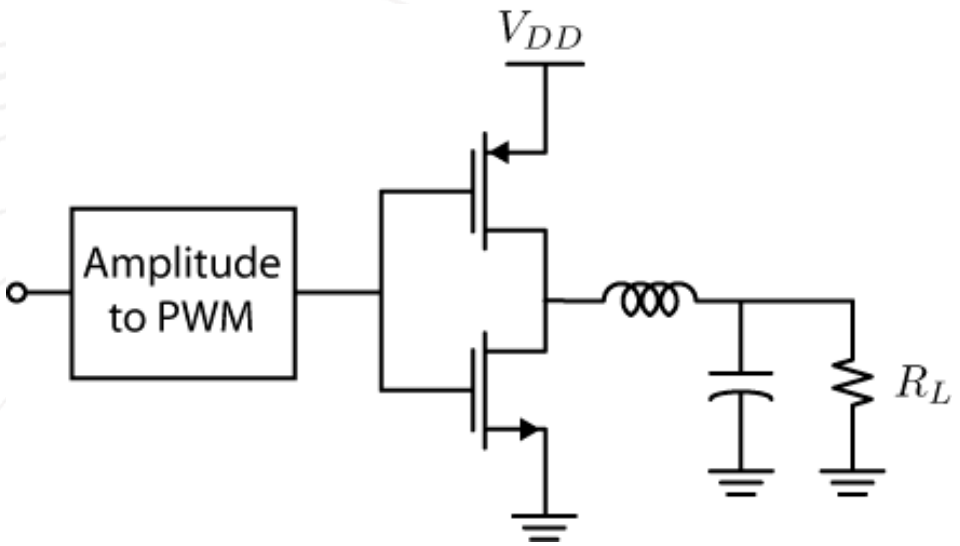
area = 1.8 x 3.6 mm^2

Class S



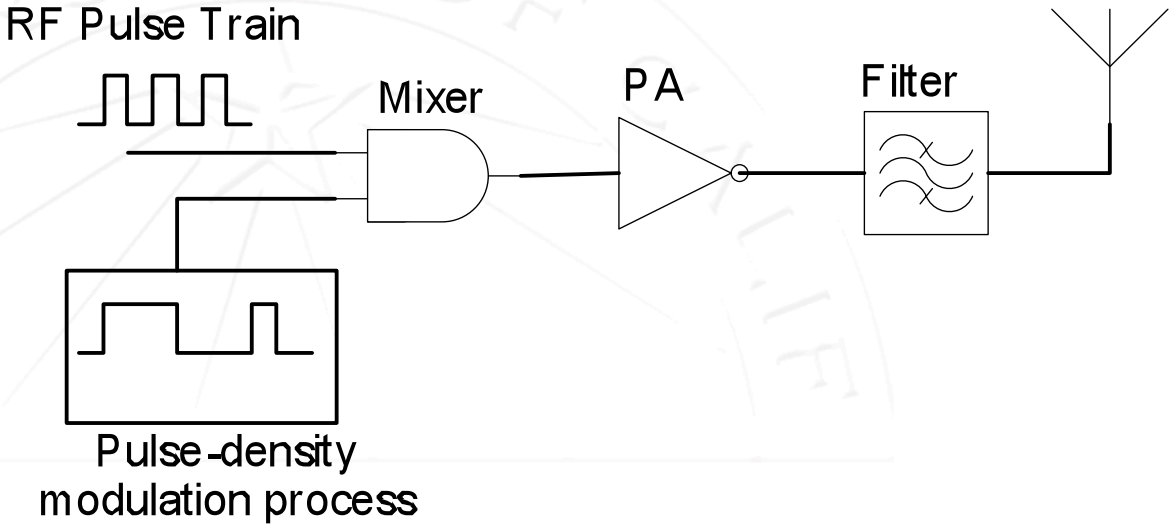
- If the switching rate is much higher than the fundamental, then amplitude modulation can be converted to pulse-width modulation.
- A low-pass filter at the output faithfully recreates the envelope of the signal.

Class S Amplifier



- Class S amplifiers are commonly used at low frequencies (audio) since the transistors can be switched at a much higher frequency than the fundamental.
- This allows efficiencies approaching 100% with good linearity.

Pulse Density Modulation



- Inherent linearity
- Improved efficiency in power backoff… but,

Pulse Density Modulation Process

- AM process → Extra harmonics
- Tradeoff between oversampling ratio & Q
  - Out of band spectrum
  - Efficiency
- Noise shaping: digital ΣΔ
- Conclusions
  - No major efficiency advantage with Q<~5-10
  - Linearity may be the compelling factor
  - (almost) pure digital implementation!
  - Need to run PDM process *as fast as possible*

