Complete MOS Small-Signal Model

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Announcements

- Welcome back!
- Pick up graded MT2 in lecture on Tuesday
- Check updated syllabus
- No lab this week
- HW8 due on Friday
Review: An MOS Amplifier

This type of amplifier is known as “Common Source (CS)”
Plot of Output Waveform (Gain!)
Total Small Signal Current

\[ i_{DS}(t) = I_{DS} + i_{ds} \]

\[ i_{ds} = \frac{\partial i_{DS}}{\partial v_{gs}} v_{gs} + \frac{\partial i_{DS}}{\partial v_{ds}} v_{ds} \]

\[ i_{ds} = g_m v_{gs} + \frac{1}{r_o} v_{ds} \]

Transconductance

Conductance
Changing One Variable at a Time

Assumption: \( V_{DS} > V_{DS,SAT} = V_{GS} - V_Tn \) (square law)
The **Transconductance** $g_m$

Defined as the change in drain current due to a change in the gate-source voltage, with *everything else constant*,

\[ I_{DS,\text{sat}} = \frac{W}{L} \frac{\mu C_{ox}}{2} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \]

\[ g_m = \frac{\Delta i_D}{\Delta v_{GS}} \bigg|_{v_{GS},v_{DS}} = \frac{\partial i_D}{\partial v_{GS}} \bigg|_{v_{GS},v_{DS}} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)(1 + \lambda V_{DS}) \]

\[ g_m \approx 0 \]

\[ g_m = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T) \]

\[ g_m = \mu C_{ox} \frac{W}{L} \left( \frac{2I_{DS}}{W} \right) = \sqrt{2\mu C_{ox} \frac{W}{L} I_{DS}} \]

\[ g_m = \frac{2I_{DS}}{(V_{GS} - V_T)} \]
Output Resistance $r_o$

Defined as the inverse of the change in drain current due to a change in the drain-source voltage, with everything else constant.

\[ \frac{\delta I_{DS}}{K} \]

Non-Zero Slope Caused by Channel-Length Modulation

\[ V_{DS}(V) \]
Evaluating $r_o$

$$i_D = \frac{W}{L} \frac{\mu C_{ox}}{2} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$r_o = \left( \frac{\partial i_D}{\partial v_{DS}} \right)^{-1}_{V_{GS}, V_{DS}}$$

$$r_o = \frac{1}{\frac{W}{L} \frac{\mu C_{ox}}{2} (V_{GS} - V_T)^2 \lambda}$$

$$r_o \approx \frac{1}{\lambda I_{DS}}$$
This is a simplified, 3-terminal small-signal model for a MOSFET.

In later lectures we will develop a more complete model.

- $g_m =$ transconductance
  - defined as $\frac{di_{ds}}{dv_{gs}}$, units [Ohms]$^{-1}$

- $r_o =$ output resistance
  - defined as $[\frac{di_{ds}}{dv_{ds}}]^{-1}$, units Ohms
Small-Signal PMOS Model

- This is a simplified, 3-terminal small-signal model for a MOSFET
- In later lectures we will develop a more complete model
- $g_m = \text{transconductance}$
  - defined as $\frac{\text{di}_{sd}}{\text{dv}_{sg}}$, units [Ohms]$^{-1}$
- $r_o = \text{output resistance}$
  - defined as $[\frac{\text{di}_{sd}}{\text{dv}_{sd}}]^{-1}$, units Ohms
What we’ve ignored…until now!

- The fourth terminal of the MOSFET is the body of the transistor… it can act like a second gate, or “back gate”
- The junctions of the transistor form pn-junction diodes with body, this introduces parasitic capacitance
MOSFET Capacitances in Saturation

MOSFETS have many parasitic capacitances. Let us analyze where each parasitic comes from.

- Note that gate-source capacitance: channel charge is mostly controlled by gate-source and not drain in saturation.
Gate-Source Capacitance $C_{gs}$

Wedge-shaped charge in saturation $\rightarrow$ effective area is $(2/3)WL$

$$C_{gs} = (2/3)WL C_{ox} + C_{ov}$$

Overlap capacitance along source edge of gate $\rightarrow$

$$C_{ov} = L_D WC_{ox}$$

(Underestimate due to fringing fields)
Not due to change in inversion charge in channel.

Overlap (and fringing) capacitance $C_{ov}$ between drain and source is $C_{gd}$

$$C_{gd} = C_{ov} = L_D W C_{ox}$$
Drain-Bulk Capacitance $C_{db}$

Drain-Bulk and Source-Bulk capacitance is caused by p-n junction depletion

source to bulk cap: $C_{jsb} = \frac{C_j(0)}{\sqrt{1 + V_{SB}/|\Phi_B|}} \text{WE} + \frac{C_{jsw}(0)}{\sqrt{1 + V_{SB}/|\Phi_B|}} (W + 2E)$

drain to bulk cap: $C_{jsd} = \frac{C_j(0)}{\sqrt{1 + V_{DB}/|\Phi_B|}} \text{WE} + \frac{C_{jsw}(0)}{\sqrt{1 + V_{DB}/|\Phi_B|}} (W - 2E)$
Summary of Capacitance Models

\[ C_{gs} = (2/3)WLC_{ox} + C_{ov} \]
\[ C_{gd} = C_{ov} \]
\[ C_{sb} = C_{jsb}(\text{area + perimeter})\text{ junction} \]
\[ C_{db} = C_{jdb}(\text{area + perimeter})\text{ junction} \]
Back-Gate Effect

- Transistor really has *four* terminals:
  - Source / Drain
  - Gate / Body
- There is a symmetry between the gate and the body. The body can act like a “back gate”
- In many instances the body terminal is simply tied to the source (ground or VSS for NMOS, supply or VDD for PMOS)
- What happens if there is a DC or AC voltage swing on the body?
Body Bias Affects $V_T$

- If there is a body bias $V_{SB}$, a depletion capacitance appears in parallel with $C_{ox}$ and affects the amount of channel charge:

$$Q_{inv} = -C_{ox} \left[ V_{GS} - V_T + \frac{C_{dep}}{C_{ox}} V_{SB} \right]$$

$$C_{dep} = \varepsilon_s / x_{dep,max}$$

$$Q_{inv} = -C_{ox} (V_{GS} - V_T) + C_{dep} V_{SB}$$

$$V_T (V_{SB}) = V_{T0} + \frac{C_{dep}}{C_{ox}} V_{SB}$$

- $C_{dep}$ changes with body bias, if we account for this:

$$V_{T0n} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}} \sqrt{2q\varepsilon_s N_a (-2\phi_p)}$$

$$\Delta V_T = \frac{1}{C_{ox}} \sqrt{2q\varepsilon_s N_a (\sqrt{-2\phi_p} + V_S) - \sqrt{-2\phi_p}}$$

$$V_T = V_{T0} + \gamma \left( \sqrt{V_{SB} - 2\phi_p} - \sqrt{-2\phi_p} \right)$$
Role of the Substrate Potential

Note: Need not be the source potential, but $V_B < V_S$

Effect: changes threshold voltage, which changes the drain current … substrate acts like a “backgate”

$$g_{mb} = \frac{\Delta i_D}{\Delta v_{BS}} \bigg|_Q = \frac{\partial i_D}{\partial v_{BS}} \bigg|_Q$$

$$Q = (V_{GS}, V_{DS}, V_{BS})$$

$$g_{mb} = \frac{\partial i_D}{\partial v_{BS}} \bigg|_Q = \frac{\partial i_D}{\partial V_{Tn}} \bigg|_Q \frac{\partial V_{Tn}}{\partial v_{BS}} \bigg|_Q$$
Backgate Transconductance

\[ V_T = V_{T0} + \gamma \left( \sqrt{V_{SB} - 2\phi_p} - \sqrt{-2\phi_p} \right) \]

Result:

\[ g_{mb} = \frac{\partial i_D}{\partial V_{BS}} \bigg|_Q = \frac{\partial i_D}{\partial V_{Tn}} \bigg|_Q \frac{\partial V_{Tn}}{\partial V_{BS}} \bigg|_Q = \frac{\gamma g_m}{2 \sqrt{V_{BS} - 2\phi_p}} \]
Four-Terminal Small-Signal Model

\[ i_{ds} = g_m v_{gs} + g_{mb} v_{bs} + \frac{1}{r_o} v_{ds} \]
Complete Small-Signal Model NMOS
Complete Small-Signal Model PMOS